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Details	
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Core Size	16-Bit
Speed	24MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	68
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2215rute24v

Section 8 Data Transfer Controller (DTC)

7.2 Register Configuration

The DMAC registers are listed below.

- Memory address register 0A (MAR0A)
- I/O address register 0A (IOAR0A)
- Transfer count register 0A (ETCR0A)
- Memory address register 0B (MAR0B)
- I/O address register 0B (IOAR0B)
- Transfer count register 0B (ETCR0B)
- Memory address register 1A (MAR1A)
- I/O address register 1A (IOAR1A)
- Transfer count register 1A (ETCR1A)
- Memory address register 1B (MAR1B)
- I/O address register 1B (IOAR1B)
- Transfer count register 1B (ETCR1B)
- DMA write enable register (DMAWER)
- DMA control register 0A (DMACR0A)
- DMA control register 0B (DMACR0B)
- DMA control register 1A (DMACR1A)
- DMA control register 1B (DMACR1B)
- DMA band control register (DMABCR)

The DMAC register functions differs depending on the address modes: short address mode and full address mode. The DMAC register functions are described in each address mode. Short address mode or full address mode can be selected for channels 1 and 0 independently by means of bits FAE1 and FAE0.

10.3.1 Timer Control Register (TCR)

The TCR registers control the TCNT operation for each channel. The TPU has a total of three TCR registers, one for each channel (channels 0 to 2). TCR register settings should be made only when TCNT operation is stopped.

Bit	Bit Name	Initial value	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	These bits select the TCNTcounter clearing source. See tables 10.3 and 10.4 for details.
5	CCLR0	0	R/W	
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge. When the internal clock is counted using both edges, the input clock frequency is halved (e.g., ϕ/4 both edges = ϕ/2 rising edge). If phase counting mode is used on channels 1, 2, 4, and 5, this setting is ignored and the phase counting mode setting has priority. Internal clock edge selection is valid when the input clock is ϕ/4 or slower. If ϕ/1 is selected as the input clock, this setting is ignored and count at falling edge of ϕ is selected. 00: Count at rising edge 01: Count at falling edge 1×: Count at both edges Legend: ×: Don't care
2	TPSC2	0	R/W	Time Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT counter clock. The clock source can be selected independently for each channel. See tables 10.5 to 10.10 for details.
0	TPSC0	0	R/W	

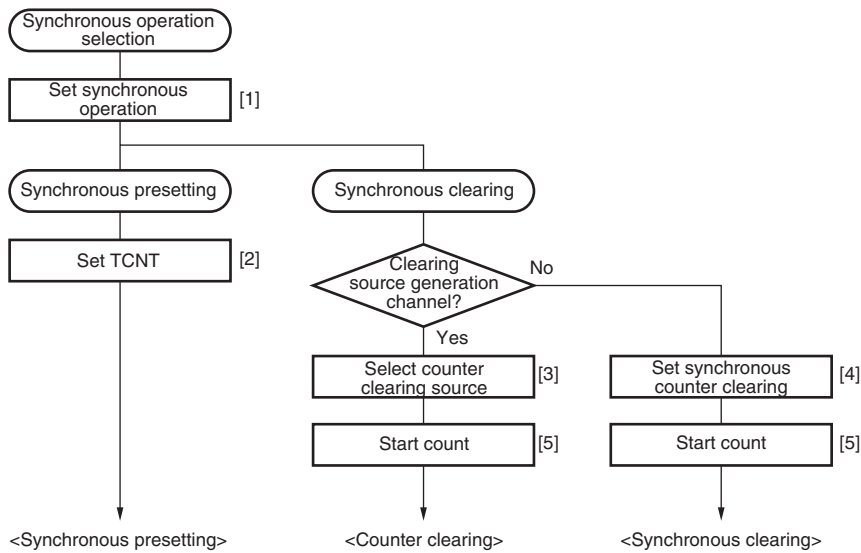
Bit	Bit Name	Initial value	R/W	Description
1	TGFB	0	R/(W)*	Input Capture/Output Compare Flag B Status flag that indicates the occurrence of TGRB input capture or compare match. The write value should always be 0 to clear this flag. [Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register [Clearing conditions] • When DTC is activated by TGIB interrupt, DISEL bit in MRB of DTC is cleared to 0, and transfer counter value is not 0 • When 0 is written to TGFB after reading TGFB = 1
0	TGFA	0	R/(W)*	Input Capture/Output Compare Flag A Status flag that indicates the occurrence of TGRA input capture or compare match. The write value should always be 0 to clear this flag. [Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register [Clearing conditions] • When DTC is activated by TGIA interrupt, DISEL bit in MRB of DTC is cleared to 0, and transfer counter value is not 0 • When 0 is written to TGFA after reading TGFA = 1

Note: * The write value should always be 0 to clear the flag.

10.5.2 Synchronous Operation

In synchronous operation, the values in a number of TCNT counters can be rewritten simultaneously (synchronous presetting). Also, a number of TCNT counters can be cleared simultaneously by making the appropriate setting in TCR (synchronous clearing). Synchronous operation enables TGR to be incremented with respect to a single time base. Channels 0 to 2 can all be designated for synchronous operation.

Example of Synchronous Operation Setting Procedure: Figure 10.14 shows an example of the synchronous operation setting procedure.



[1] Set to 1 the SYNC bits in TSYR corresponding to the channels to be designated for synchronous operation.
[2] When the TCNT counter of any of the channels designated for synchronous operation is written to, the same value is simultaneously written to the other TCNT counters.
[3] Use bits CCLR2 to CCLR0 in TCR to specify TCNT clearing by input capture/output compare, etc.
[4] Use bits CCLR2 to CCLR0 in TCR to designate synchronous clearing for the counter clearing source.
[5] Set to 1 the CST bits in TSTR for the relevant channels, to start the count operation.

Figure 10.14 Example of Synchronous Operation Setting Procedure

10.7.2 Interrupt Signal Timing

TGF Flag Setting Timing in Case of Compare Match: Figure 10.38 shows the timing for setting of the TGF flag in TSR by compare match occurrence, and TGI interrupt request signal timing.

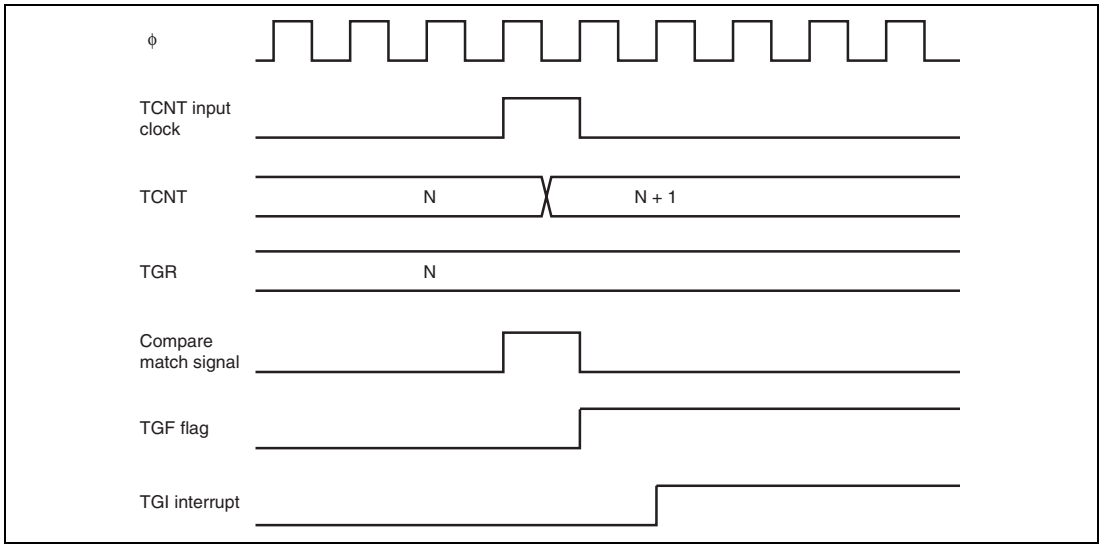


Figure 10.38 TGI Interrupt Timing (Compare Match)

TGF Flag Setting Timing in Case of Input Capture: Figure 10.39 shows the timing for setting of the TGF flag in TSR by input capture occurrence, and TGI interrupt request signal timing.

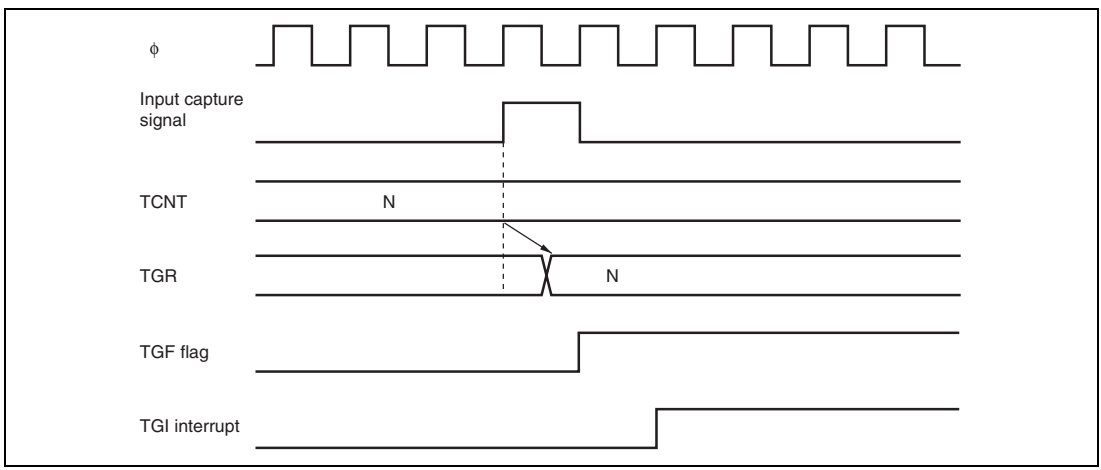


Figure 10.39 TGI Interrupt Timing (Input Capture)

11.5.2 Setting of Compare Match Flags CMFA and CMFB

The CMFA and CMFB flags in TCSR are set to 1 by a compare match signal generated when the TCOR and TCNT values match. The compare match signal is generated at the last state in which the match is true, just before the timer counter is updated. Therefore, when TCOR and TCNT match, the compare match signal is not generated until the next incrementation clock input. Figure 11.5 shows this timing.

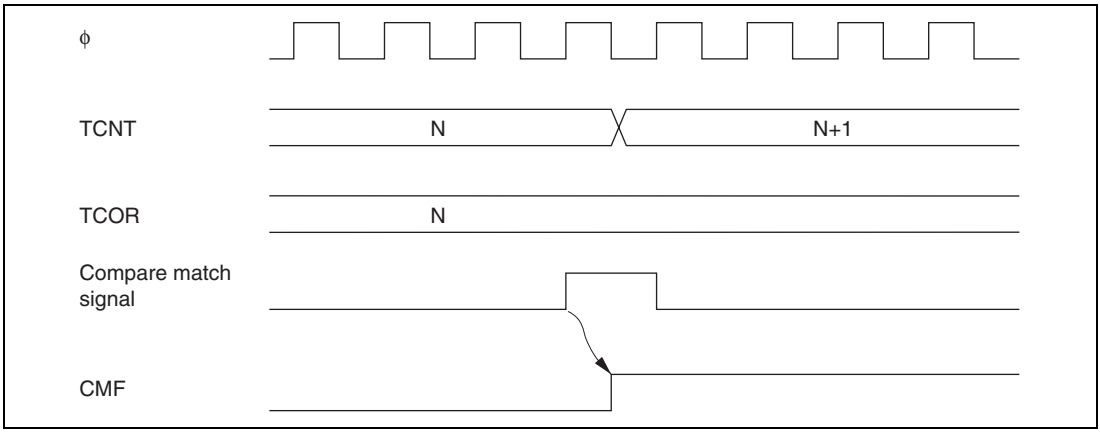


Figure 11.5 Timing of CMF Setting

11.5.3 Timer Output Timing

When compare match A or B occurs, the timer output changes as specified by bits OS3 to OS0 in TCSR. Figure 11.6 shows the timing when the output is set to toggle at compare match A.

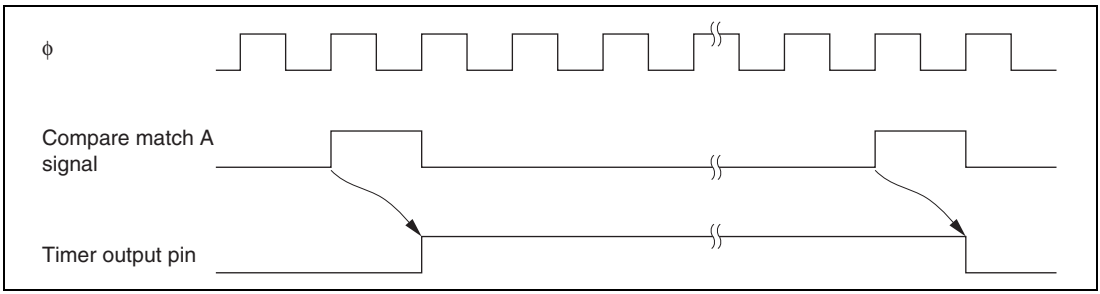


Figure 11.6 Timing of Timer Output

11.7 Interrupts

11.7.1 Interrupt Sources and DTC Activation

There are three 8-bit timer interrupt sources: CMIA, CMIB, and OVI. Their relative priorities are shown in table 11.3. Each interrupt source is set as enabled or disabled by the corresponding interrupt enable bit in TCR or TCSR, and independent interrupt requests are sent for each to the interrupt controller. It is also possible to activate the DTC by means of CMIA and CMIB interrupts.

Table 11.3 8-Bit Timer Interrupt Sources

Channel	Name	Interrupt Source	Interrupt Flag	DTC Activation	Priority*
0	CMIA0	TCORA_0 compare match	CMFA	Possible	High
	CMIB0	TCORB_0 compare match	CMFB	Possible	
	OVI0	TCNT_0 overflow	OVF	Not possible	
1	CMIA1	TCORA_1 compare match	CMFA	Possible	
	CMIB1	TCORB_1 compare match	CMFB	Possible	
	OVI1	TCNT_1 overflow	OVF	Not possible	Low

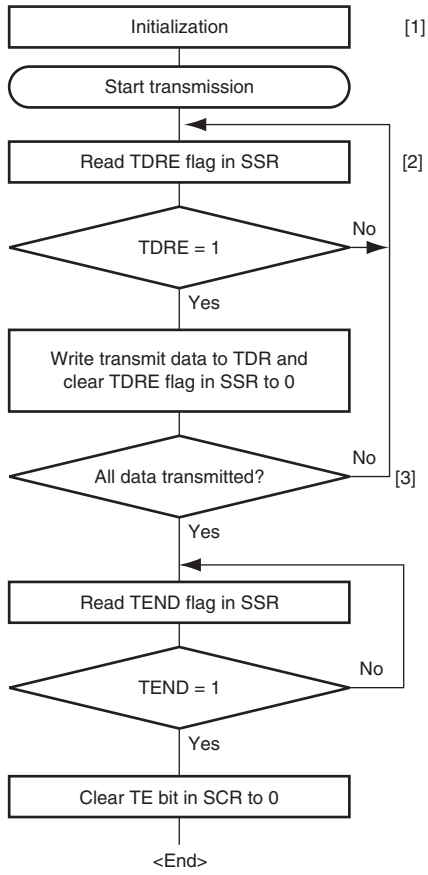
Note: * This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

12.2.3 Reset Control/Status Register (RSTCSR)

RSTCSR is an 8-bit readable/writable register that controls the generation of the internal reset signal when TCNT overflows, and selects the type of internal reset signal. RSTCSR is initialized to H'1F by a reset signal from the $\overline{\text{RES}}$ pin, and not by the WDT internal reset signal caused by overflows.

Bit	Bit Name	Initial Value	R/W	Description
7	WOVF	0	R/(W)*	Watchdog Overflow Flag This bit is set when TCNT overflows in watchdog timer mode. This bit cannot be set in interval timer mode, and the write value should always be 0. [Setting condition] • Set when TCNT overflows (changed from H'FF to H'00) in watchdog timer mode [Clearing condition] • Cleared by reading RSTCSR when WOVF = 1, and then writing 0 to WOVF
6	RSTE	0	R/W	Reset Enable Specifies whether or not a reset signal is generated in the chip if TCNT overflows during watchdog timer operation. 0: Reset signal is not generated even if TCNT overflows (Though this LSI is not reset, TCNT and TCSR in WDT are reset) 1: Reset signal is generated if TCNT overflows
5	RSTS	0	R/W	Reset Select Selects the type of internal reset generated if TCNT overflows during watchdog timer operation. 0: Power-on reset 1: Setting prohibited
4 to 0	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.

Note: * The write value should always be 0 to clear this flag.



[1] SCI initialization:
The TxD pin is automatically designated as the transmit data output pin.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:
To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and then clear the TDRE flag to 0.
Checking and clearing of the TDRE flag is automatic when the DMAC or the DTC* is activated by a transmit data empty interrupt (TXI) request and data is written to TDR.

Note: * Checking and clearing of the TDRE flag are performed automatically by the DTC when the DTC's DISEL bit is cleared to 0 and the transfer counter value is not 0. Consequently, it is necessary to use the CPU to clear the TDRE flag if DISEL is set to 1 or if the transfer counter value is 0.

Figure 13.21 Sample Serial Transmission Data Flowchart

13.7.6 Initialization

Before transmitting and receiving data, initialize the SCI as described below. Initialization is also necessary when switching from transmit mode to receive mode, or vice versa.

1. Clear the TE and RE bits in SCR to 0.
2. Clear the error flags ERS, PER, and ORER in SSR to 0.
3. Set the GM, BLK, O/$\overline{E}$, BCP0, BCP1, CKS0, CKS1 bits in SMR. Set the PE bit to 1.
4. Set the SMIF, SDIR, and SINV bits in SCMR.
   When the SMIF bit is set to 1, the TxD and RxD pins are both switched from ports to SCI pins, and are placed in the high-impedance state.
5. Set the value corresponding to the bit rate in BRR.
6. Set the CKE0 and CKE1 bits in SCR. Clear the TIE, RIE, TE, RE, MPIE, and TEIE bits to 0.
   If the CKE0 bit is set to 1, the clock is output from the SCK pin.
7. Wait at least one bit interval, then set the TIE, RIE, TE, and RE bits in SCR. Do not set the TE bit and RE bit at the same time, except for self-diagnosis.

To switch from receive mode to transmit mode, after checking that the SCI has finished reception, initialize the SCI, and set RE to 0 and TE to 1. Whether SCI has finished reception or not can be checked with the RDRF, PER, or ORER flags. To switch from transmit mode to receive mode, after checking that the SCI has finished transmission, initialize the SCI, and set TE to 0 and RE to 1. Whether SCI has finished transmission or not can be checked with the TEND flag.

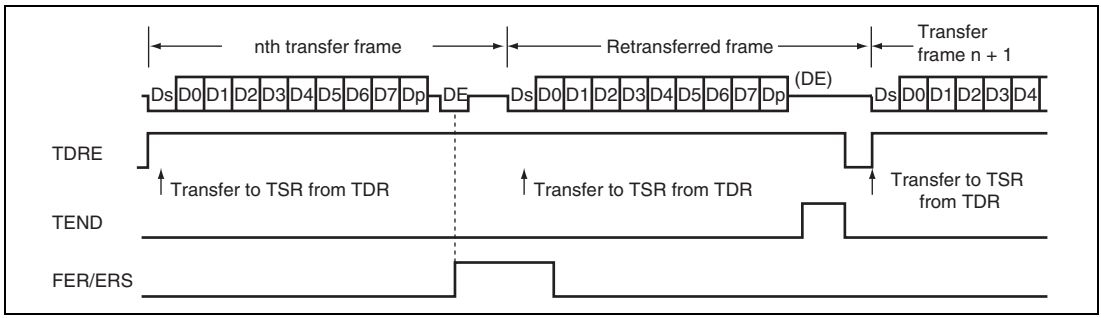


Figure 13.30 Retransfer Operation in SCI Transmit Mode

The timing for setting the TEND flag depends on the value of the GM bit in SMR. The TEND flag set timing is shown in figure 13.31.

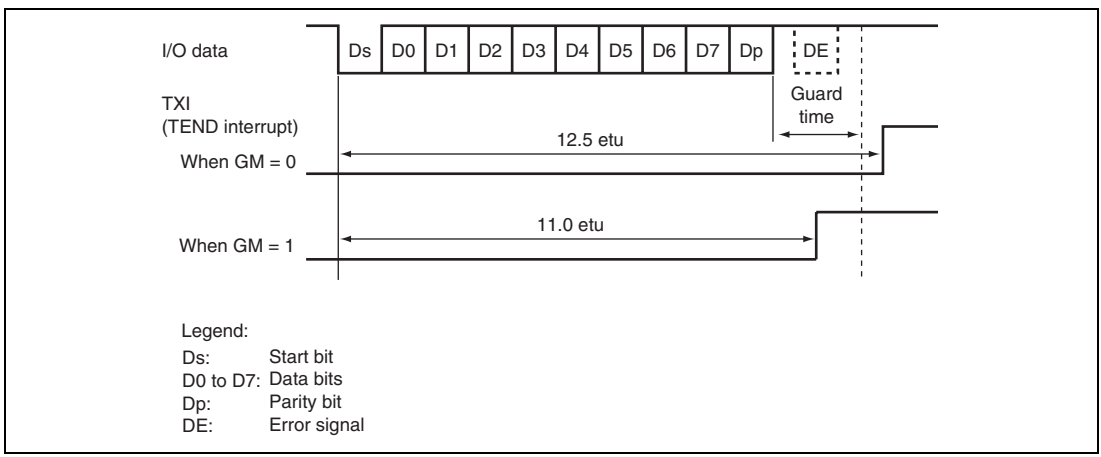


Figure 13.31 TEND Flag Generation Timing in Transmission Operation

Bit	Bit Name	Initial Value	R/W	Description
7	CK48READYE	1	R/W	Enables the CK48READY interrupt
6	SOFE	0	R/W	Enables the SOF interrupt
5	SETCE	0	R/W	Enables the SETC interrupt
4	SETIE	0	R/W	Enables the SETI interrupt
3	—	0	R	Reserved This bit is always read as 0.
2	SPRSiE	0	R/W	Enables the SPRSi interrupt (only for $\overline{\text{IRQ6}}$)
1	—	0	R	Reserved This bit is always read as 0.
0	VBUSiE	0	R/W	Enables the VBUSi interrupt

15.3.38 USB Interrupt Select Register 0 (UISR0)

UISR0 selects the $\overline{\text{EXIRQ}}$ pin to output interrupt request indicated in the interrupt flag register 0 (UIFR0). When a bit in UIER0 corresponding to the UISR0 bit is cleared to 0, an interrupt request is output to $\overline{\text{EXIRQ0}}$. When a bit in UIER0 corresponding to the UISR0 bit is set to 1, an interrupt request is output to $\overline{\text{EXIRQ1}}$.

Bit	Bit Name	Initial Value	R/W	Description
7	BRSTS	0	R/W	Selects the BRST interrupt
6	—	0	R	Reserved This bit is always read as 0.
5	EP1iTRS	0	R/W	Selects the EP1iTR interrupt
4	EP1iTSS	0	R/W	Selects the EP1iTS interrupt
3	EP0oTSS	0	R/W	Selects the EP0oTS interrupt
2	EP0iTRS	0	R/W	Selects the EP0iTR interrupt
1	EP0iTSS	0	R/W	Selects the EP0iTS interrupt
0	SetupTSS	0	R/W	Selects the SetupTS interrupt

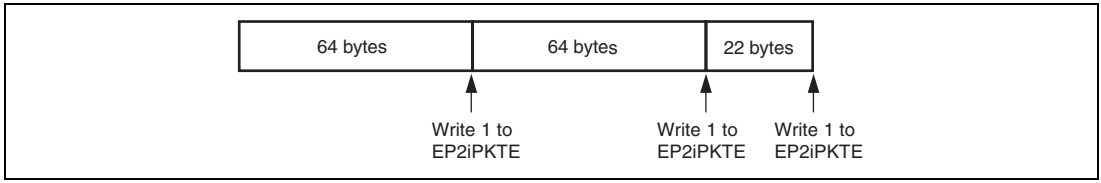


Figure 15.27 EP2iPKTE Operation in UTRG0 (Auto-Request)

(4) EPno DMA Transfer (n = 0, 2, 4)

(a) EPnoRDFN Bits of UTRG (n = 0, 2, 4)

Note that 1 is not automatically written to EPnoRDFN in case of auto-request transfer. Always write 1 to EPnoRDFN by the CPU. The following example shows when EP2o receives 150-byte data from the host. In this case, 1 should be written to EP2oRDFN three times as shown in figure 15.28.

(b) EP2o DMA Transfer Procedure

The DMAC transfer unit should be one packet. Therefore, set the number of transfers so that it is equal to or less than the maximum packet size of each endpoint.

1. Wait for the UIFR1/EP2oREADY flag to be set.
2. DMAC settings for EP2o data transfer (such as auto-request and address setting). Read value of UESZ2o and specify number of transfers to match size of received data (64 bytes or less).
3. Activate the DMAC (write 1 to DTE after reading DTE as 0).
4. DMA transfer (transfer of 64 bytes or less).
5. Write 1 to the UTRG0/EP2oRDFN bit after the DMA transfer is completed.
6. Repeat steps 1 to 5 above.

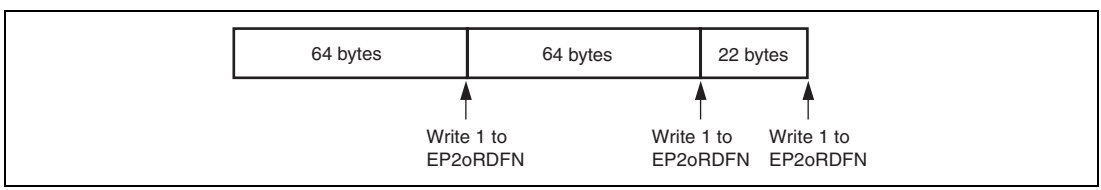


Figure 15.28 EP2oRDFN Operation in UTRG0 (Auto-Request)

Bit	Bit Name	Initial Value	R/W	Description
6	ADIE	0	R/W	A/D Interrupt Enable A/D conversion end interrupt (ADI) request enabled when 1 is set.
5	ADST	0	R/W	A/D Start Clearing this bit to 0 stops A/D conversion, and the A/D converter enters the unit state. Setting this bit to 1 starts A/D conversion. It can be set to 1 by software, the timer conversion start trigger, and the A/D external trigger ($\overline{\text{ADTRG}}$). In single mode, this bit is cleared to 0 automatically when conversion on the specified channel is complete. In scan mode, conversion continues sequentially on the specified channels until this bit is cleared to 0 by software, a reset, a transition to standby mode, or module stop mode.
4	SCAN	0	R/W	Scan Mode Selects single mode or scan mode as the A/D conversion operating mode. 0: Single mode 1: Scan mode
3	CH3	0	R/W	Channel Select 3 to 0 Select analog input channels.
2	CH2	0	R/W	
1	CH1	0	R/W	
0	CH0	0	R/W	

When SCAN = 0	When SCAN = 1
0000: AN0	0000: AN0
0001: AN1	0001: AN0 to AN1
0010: AN2	0010: AN0 to AN2
0011: AN3	0011: AN0 to AN3
01××: Setting prohibited	01××: Setting prohibited
10××: Setting prohibited	1×××: Setting prohibited
110×: Setting prohibited	
1110: AN14	
1111: AN15	

Legend:
×: Don't care

Note: * The write value should always be 0 to clear this flag.

19.14 Note on Switching from F-ZTAT Version to Masked ROM Version

The masked ROM version does not have the internal registers for flash memory control that are provided in the F-ZTAT version. Table 19.7 lists the registers that are present in the F-ZTAT version but not in the masked ROM version. If a register listed in table 19.7 is read in the masked ROM version, an undefined value will be returned. Therefore, if application software developed on the F-ZTAT version is switched to a masked ROM version product, it must be modified to ensure that the registers in table 19.9 have no effect.

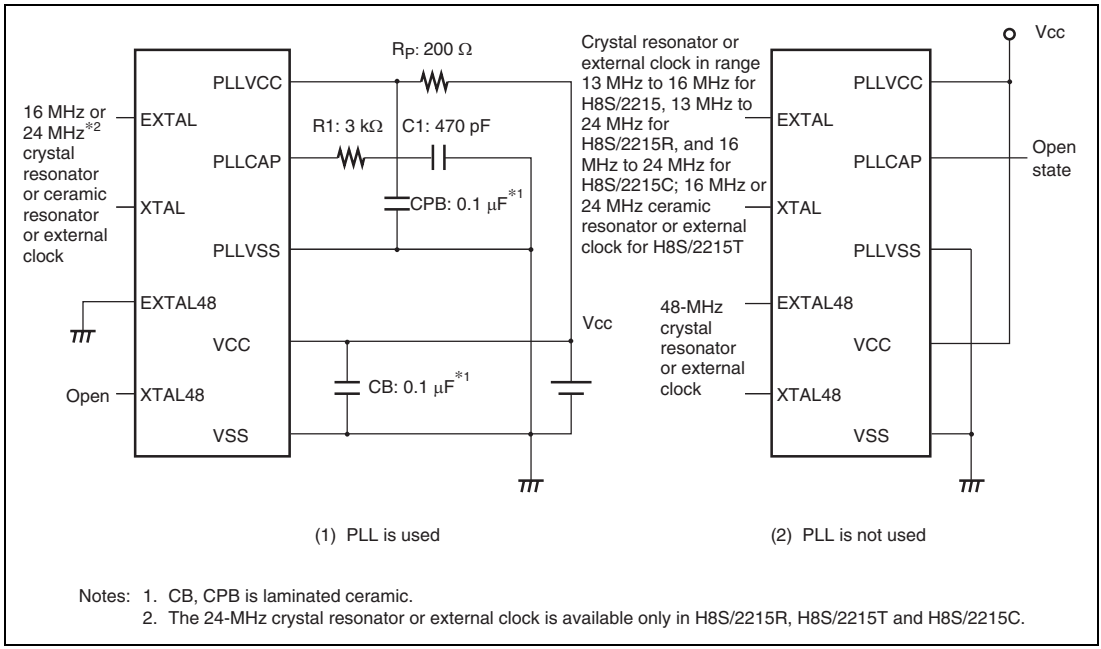
Table 19.9 Registers Present in F-ZTAT Version but Absent in Masked ROM Version

Register	Abbreviation	Address
Flash memory control register 1	FLMCR1	H'FFA8
Flash memory control register 2	FLMCR2	H'FFA9
Erase block register 1	EBR1	H'FFAA
Erase block register 2	EBR2	H'FFAB
RAM emulation register	RAMER	H'FEDB
Serial control register x	SCRX	H'FDB4

21.7 PLL Circuit for USB

The PLL circuit has the function of tripling or doubling* the 16- or 24-MHz* clock from the system oscillator to generate the 48-MHz USB operating clock. When the PLL circuit is used, set the UCKS3 to UCKS0 bits of UCTLR. For details, refer to section 15, Universal Serial Bus Interface (USB). When the PLL circuit is not used, connect the PLLVCC pin to VCC, and leave the PLLCAP pin open as shown in figure 21.11.

Note: * Available only in H8S/2215R, H8S/2215T and H8S/2215C.



Notes: 1. CB, CPB is laminated ceramic.
2. The 24-MHz crystal resonator or external clock is available only in H8S/2215R, H8S/2215T and H8S/2215C.

Figure 21.11 Example of PLL Circuit

When designing the board, place the capacitor C1 and resistor R1 as close as possible to the PLLCAP pin. Other signal lines should be routed away from the oscillator circuit to prevent induction from interfering with correct oscillation. C1 must be grounded to PLLVSS. In addition, PLLVCC and PLLVSS must be separated from the VCC and VSS pins. Bypass capacitors CPB and CB must be connected between VCC and VSS and between PLVCC and PLVSS, respectively.

22.6 Module Stop Mode

Module stop mode can be set for individual on-chip supporting modules.

When the corresponding MSTP bit in MSTPCR is set to 1, module operation stops at the end of the bus cycle and a transition is made to module stop mode. The CPU continues operating independently.

When the corresponding MSTP bit is cleared to 0, module stop mode is cleared and the module starts operating at the end of the bus cycle. In module stop mode, the internal states of modules other than the A/D converter are retained.

After reset clearance, all modules other than DTC and DMAC are in module stop mode.

When an on-chip supporting module is in module stop mode, read/write access to its registers is disabled.

When a transition is made to sleep mode with all modules stopped, the bus controller and I/O ports also stop operating, enabling current dissipation to be further reduced.

22.7 φ Clock Output Disabling Function

Output of the φ clock can be controlled by means of the PSTOP bit in SCKCR, and DDR for the corresponding port. When the PSTOP bit is set to 1, the φ clock stops at the end of the bus cycle, and φ output goes high. φ clock output is enabled when the PSTOP bit is cleared to 0. When DDR for the corresponding port is cleared to 0, φ clock output is disabled and input port mode is set. Table 22.4 shows the state of the φ pin in each processing state.

Table 22.4 φ Pin State in Each Processing State

Register Settings					
DDR	**PSTOP**	**Normal Mode**	**Sleep Mode**	**Software Standby Mode**	**Hardware Standby Mode**
0	×	High impedance	High impedance	High impedance	High impedance
1	0	φ output	φ output	Fixed high	High impedance
1	1	Fixed high	Fixed high	Fixed high	High impedance

Legend:
×: Don't care

22.8 Usage Notes

22.8.1 I/O Port Status

In software standby mode, I/O port states are retained. In addition, if the OPE bit is set to 1, the address bus and bus control signal output are retained. Therefore, there is no reduction in current dissipation for the output current when a high-level signal is output.

22.8.2 Current Dissipation during Oscillation Stabilization Wait Period

Current dissipation increases during the oscillation stabilization wait period.

22.8.3 DMAC and DTC Module Stop

Depending on the operating status of the DMAC and DTC, the MSTPA7 and MSTPA6 bits may not be set to 1. Setting of the DTC module stop mode should be carried out only when the DTC is not activated.

For details, section 7, DMA Controller (DMAC) and section 8, Data Transfer Controller (DTC).

22.8.4 On-Chip Peripheral Module Interrupts

Module interrupts do not function when in module stop mode. Consequently, it is not possible to clear CPU interrupt sources or DMAC or DTC activation sources if interrupt requests occur while in module stop mode.

For this reason, module interrupts should be disabled before entering module stop mode.

22.8.5 Writing to MSTPCR

MSTPCR should only be written to by the CPU.

Section 27 Electrical Characteristics (H8S/2215C)

27.1 Absolute Maximum Ratings

Table 27.1 lists the absolute maximum ratings.

Table 27.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}, $PLLV_{CC}$, DrV_{CC}	–0.3 to +4.3	V
Input voltage (except ports 4 and 9)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (ports 4 and 9)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85*	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Note: * The operating temperature ranges for flash memory programming/erasing are T_a = –20°C to +75°C.