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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	16MHz
Connectivity	SCI, SmartCard, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	68
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2215te16wv

2.8 Processing States

The H8S/2000 CPU has five main processing states: the reset state, exception handling state, program execution state, bus-released state, and power-down state. Figure 2.13 indicates the state transitions.

- Reset State

  In this state the CPU and internal peripheral modules are all initialized and stop. When the $\overline{\text{RES}}$ input goes low all current processing stops and the CPU enters the reset state. All interrupts are masked in the reset state. Reset exception handling starts when the $\overline{\text{RES}}$ signal changes from low to high. For details, refer to section 4, Exception Handling.

  The reset state can also be entered by a watchdog timer overflow.

- Exception-Handling State

  The exception-handling state is a transient state that occurs when the CPU alters the normal processing flow due to an exception source, such as, a reset, trace, interrupt, or trap instruction. The CPU fetches a start address (vector) from the exception vector table and branches to that address. For further details, refer to section 4, Exception Handling.

- Program Execution State

  In this state the CPU executes program instructions in sequence.

- Bus-Released State

  In a product which has a bus master other than the CPU, such as a direct memory access controller (DMAC) and a data transfer controller (DTC), the bus-released state occurs when the bus has been released in response to a bus request from a bus master other than the CPU. While the bus is released, the CPU halts operations.

- Power-Down State

  This is a power-down state in which the CPU stops operating. The program stop state occurs when a SLEEP instruction is executed or the CPU enters hardware standby mode. For details, refer to section 22, Power-Down Modes.

Section 3 MCU Operating Modes

3.1 Operating Mode Selection

This LSI supports four operating modes (modes 7 to 4). These modes are depending on the setting of mode pins (MD2 to MD0). Modes 6 to 4 are extended modes in which external memory and external peripheral devices can be accessed. In extended modes, each area can be used as 8-bit or 16-bit address space according to the bus controller settings after program execution. In this case, if an area is specified as 16-bit access space, 16-bit bus mode is employed for all areas; while if an area is specified as 8-bit access space, 8-bit bus mode is employed for all areas. In mode 7, external addresses cannot be used. Do not change the mode pin settings during operation.

Table 3.1 MCU Operating Mode Selection

MCU Operating Mode	MD2	MD1	MD0	CPU Operating Mode	Description	On-Chip ROM	External Data Bus	
							Initial Value	Maximum Value
4	1	0	0	Advanced mode	On-chip ROM disabled, extended mode	Disabled	16 bits	16 bits
5	1	0	1	Advanced mode	On-chip ROM disabled, extended mode	Disabled	8 bits	16 bits
6	1	1	0	Advanced mode	On-chip ROM enabled, extended mode	Enabled	8 bits	16 bits
7*	1	1	1	Advanced mode	Single-chip mode	Enabled	—	—

Note: * The following applies to the use of mode 7.
(1) H8S/2215
The USB cannot be used in mode 7.
(2) H8S/2215R, H8S/2215T or H8S/2215C
Development work using the E6000 emulator:
The USB cannot be used in mode 7.
Development work using the on-chip (E10A-USB) emulator:
The USB can be used in mode 7.
See section 3.3.4, Mode 7, for details.

Table 4.2 Exception Handling Vector Table

Exception Source		Vector Number	Vector Address[*1]	
			Normal Mode[*2]	Advanced Mode
Power-on reset		0	H'0000 to H'0001	H'0000 to H'0003
Manual reset		1	H'0002 to H'0003	H'0004 to H'0007
Reserved for system use		2	H'0004 to H'0005	H'0008 to H'000B
		3	H'0006 to H'0007	H'000C to H'000F
		4	H'0008 to H'0019	H'0010 to H'0013
Trace		5	H'000A to H000B	H'0014 to H0017
Direct transitions[*2]		6	H'000C to H000D	H'0018 to H001B
External interrupt (NMI)		7	H'000E to H'000F	H'001C to H'001F
Trap instruction	#0	8	H'0010 to H'0011	H'0020 to H'0023
	#1	9	H'0012 to H'0013	H'0024 to H'0027
	#2	10	H'0014 to H'0015	H'0028 to H'002B
	#3	11	H'0016 to H'0017	H'002C to H'002F
Reserved for system use		12	H'0018 to H'0019	H'0030 to H'0033
		13	H'001A to H'001B	H'0034 to H'0037
		14	H'001C to H'001D	H'0038 to H'003B
		15	H'001E to H'001F	H'003C to H'003F
External interrupt	IRQ0	16	H'0020 to H'0021	H'0040 to H'0043
External interrupt	IRQ1	17	H'0022 to H'0023	H'0044 to H'0047
External interrupt	IRQ2	18	H'0024 to H'0025	H'0048 to H'004B
External interrupt	IRQ3	19	H'0026 to H'0027	H'004C to H'004F
External interrupt	IRQ4	20	H'0028 to H'0029	H'0050 to H'0053
External interrupt	IRQ5	21	H'002A to H'002B	H'0054 to H'0057
USB interrupt	IRQ6	22	H'002C to H'002D	H'0058 to H'005B
External interrupt	IRQ7	23	H'002E to H'002F	H'005C to H'005F
Internal interrupt[*3]		24	H'0030 to H'0031	H'0060 to H'0063
		⎪	⎪	⎪
		127	H'00FE to H'00FF	H'01FC to H'01FF

Notes: 1. Lower 16 bits of the address.
2. Not available in this LSI.
3. For details of internal interrupt vectors, see section 5.5, Interrupt Exception Handling Vector Table.

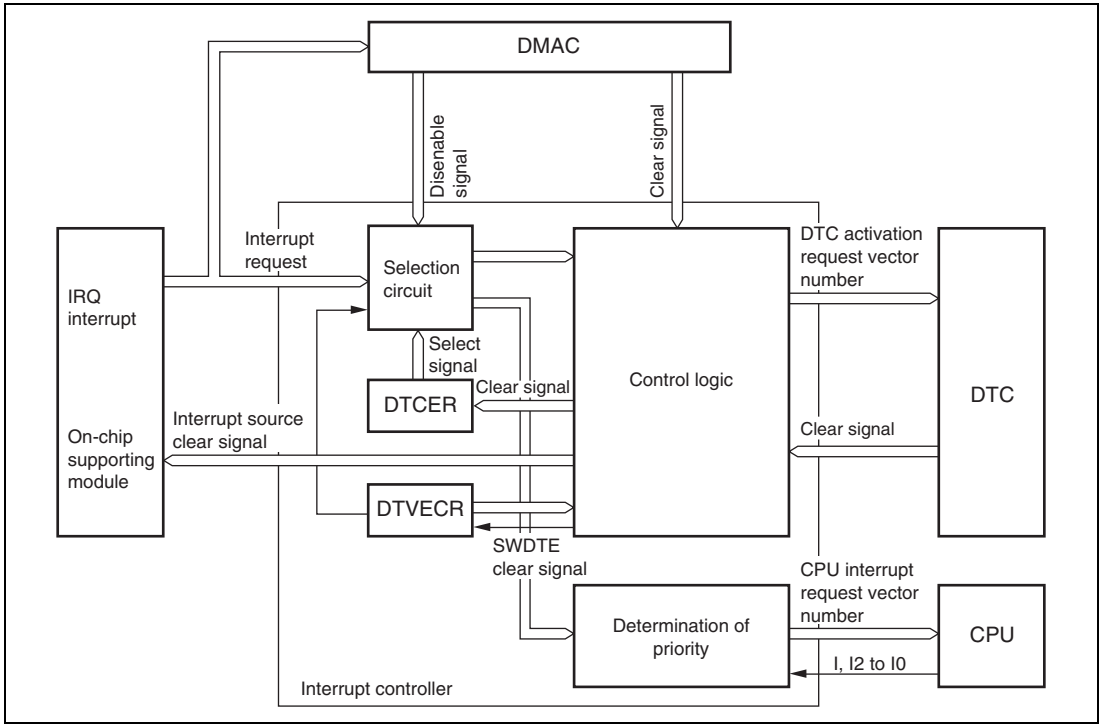


Figure 5.7 Interrupt Control for DTC and DMAC

Selection of Interrupt Source: An activation factor is directly input to each channel of the DMAC. The activation factors for each channel of the DMAC are selected by the DTF3 to DTF0 bits of DMACR. The DTA bit of DMABCR can be used to select whether the selected activation factors are managed by the DMAC. By setting the DTA bit to 1, the interrupt factor which was the activation factor for that DMAC cannot act as the DTC activation factor or the CPU interrupt factor.

Interrupt factors other than the interrupts managed by the DMAC are selected as DTC activation request or CPU interrupt request by the DTCERA to DTCERF of DTC and the DTCE bit of DTCERI.

By specifying the DISEL bit of the DTC's MRB, it is possible to clear the DTCE bit to 0 after DTC data transfer, and request a CPU interrupt.

If DTC carries out the designate number of data transfers and the transfer counter reads 0, after DTC data transfer, the DTCE bit is also cleared to 0, CPU interrupt requested.

6.3.1 Bus Width Control Register (ABWCR)

ABWCR designates each area for either 8-bit access or 16-bit access.

ABWCR sets the data bus width for the external memory space. The bus width for on-chip memory and internal I/O registers except for the on-chip USB is fixed regardless of the settings in ABWCR.

Bit	Bit Name	Initial Value	R/W	Description
7	ABW7	1/0*1	R/W	Area 7 to 0 Bus Width Controls
6	ABW6*2	1/0*1	R/W	These bits select whether the corresponding area is to be designated for 8-bit access or 16-bit access.
5	ABW5	1/0*1	R/W	0: Area n is designated for 16-bit access
4	ABW4	1/0*1	R/W	1: Area n is designated for 8-bit access
3	ABW3	1/0*1	R/W	Note: n = 7 to 0
2	ABW2	1/0*1	R/W	
1	ABW1	1/0*1	R/W	
0	ABW0	1/0*1	R/W	

Notes: 1. In modes 5 to 7, initial value of each bit is 1. In mode 4, initial value of each bit is 0.
2. The on-chip USB is allocated to area 6. Therefore this bit should be set to 1.

Table 7.1 Short Address Mode and Full Address Mode (For 1 Channel: Example of Channel 0)

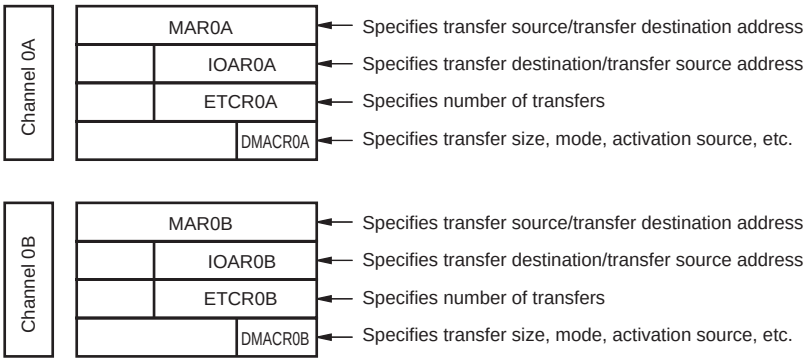
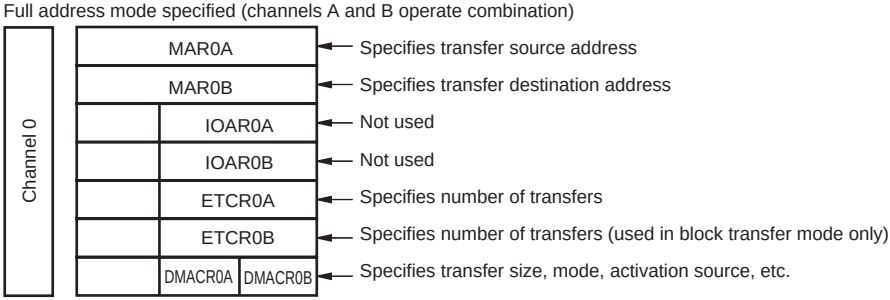
FAE0	Description
0	Short address mode specified (channels A and B operate independently) 
1	Full address mode specified (channels A and B operate combination) 

Table 9.41 PC2 Pin Function

Operating Mode	Modes 4 and 5	Mode 6*		Mode 7	
PC2DDR	—	0	1	0	1
Pin Function	A2 output	PC2 input	A2 output	PC2 input	PC2 output

Table 9.42 PC1 Pin Function

Operating Mode	Modes 4 and 5	Mode 6*		Mode 7	
PC1DDR	—	0	1	0	1
Pin Function	A1 output	PC1 input	A1 output	PC1 input	PC1 output

Table 9.43 PC0 Pin Function

Operating Mode	Modes 4 and 5	Mode 6*		Mode 7	
PC0DDR	—	0	1	0	1
Pin Function	A0 output	PC0 input	A0 output	PC0 input	PC0 output

Note: * When on-chip USB is used in mode 6, bits PC7DDR to PC0DDR should be set to H'FF so that the pins output A7 to A0.

2. Phase counting mode 2

Figure 10.27 shows an example of phase counting mode 2 operation, and table 10.21 summarizes the TCNT up/down-count conditions.

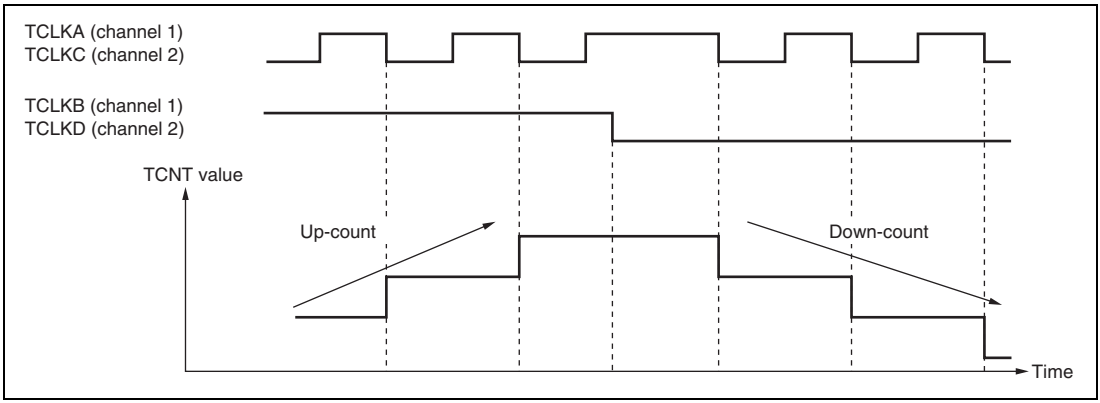


Figure 10.27 Example of Phase Counting Mode 2 Operation

Table 10.21 Up/Down-Count Conditions in Phase Counting Mode 2

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Don't care
Low level	↓	
↑	Low level	
↓	High level	Up-count
High level	↓	Don't care
Low level	↑	
↑	High level	
↓	Low level	Down-count

Legend:
↑ : Rising edge
↓ : Falling edge

10.6 Interrupts

10.6.1 Interrupt Source and Priority

There are three kinds of TPU interrupt source: TGR input capture/compare match, TCNT overflow, and TCNT underflow. Each interrupt source has its own status flag and enable/disabled bit, allowing generation of interrupt request signals to be enabled or disabled individually. When an interrupt request is generated, the corresponding status flag in TSR is set to 1. If the corresponding enable/disable bit in TIER is set to 1 at this time, an interrupt is requested. The interrupt request is cleared by clearing the status flag to 0. Relative channel priorities can be changed by the interrupt controller, but the priority order within a channel is fixed. For details, see section 5, Interrupt Controller. Table 10.24 lists the TPU interrupt sources.

Table 10.24 TPU Interrupts

Channel	Name	Interrupt Source	Interrupt Flag	DTC Activation	DMAC Activation	Priority*
0	TGI0A	TGRA_0 input capture/compare match	TGFA	Possible	Possible	High
	TGI0B	TGRB_0 input capture/compare match	TGFB	Possible	Not possible	
	TGI0C	TGRC_0 input capture/compare match	TGFC	Possible	Not possible	
	TGI0D	TGRD_0 input capture/compare match	TGFD	Possible	Not possible	
	TCI0V	TCNT_0 overflow	TCFV	Not possible	Not possible	
1	TGI1A	TGRA_1 input capture/compare match	TGFA	Possible	Possible	
	TGI1B	TGRB_1 input capture/compare match	TGFB	Possible	Not possible	
	TCI1V	TCNT_1 overflow	TCFV	Not possible	Not possible	
	TCI1U	TCNT_1 underflow	TCFU	Not possible	Not possible	
2	TGI2A	TGRA_2 input capture/compare match	TGFA	Possible	Possible	
	TGI2B	TGRB_2 input capture/compare match	TGFB	Possible	Not possible	
	TCI2V	TCNT_2 overflow	TCFV	Not possible	Not possible	
	TCI2U	TCNT_2 underflow	TCFU	Not possible	Not possible	Low

Note: * This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

Writing to RSTCSR: RSTCSR must be written to by a word transfer to address H'FF76. It cannot be written to with byte instructions. Figure 12.7 shows the format of data written to RSTCSR. The method of writing 0 to the WOVF bit differs from that for writing to the RSTE and RSTS bits.

To write 0 to the WOVF bit, the upper byte of the written word must contain H'A5 and the lower byte must contain H'00. This clears the WOVF bit to 0, but has no effect on the RSTE and RSTS bits. To write to the RSTE and RSTS bits, the upper byte must contain H'5A and the lower byte must contain the write data. This writes the values in bits 6 and 5 of the lower byte into the RSTE and RSTS bits, but has no effect on the WOVF bit.

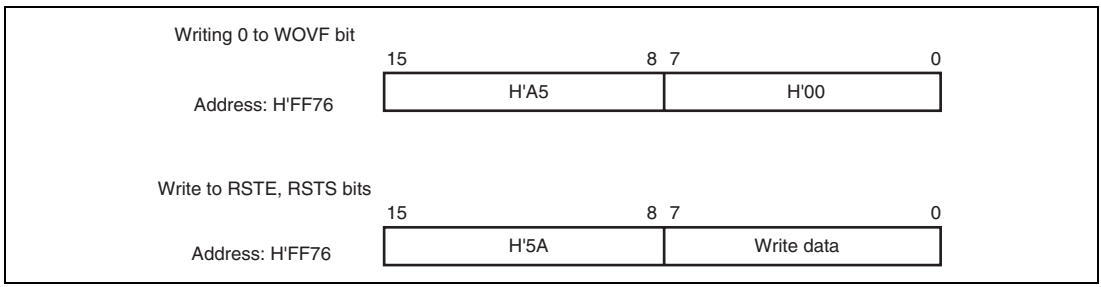
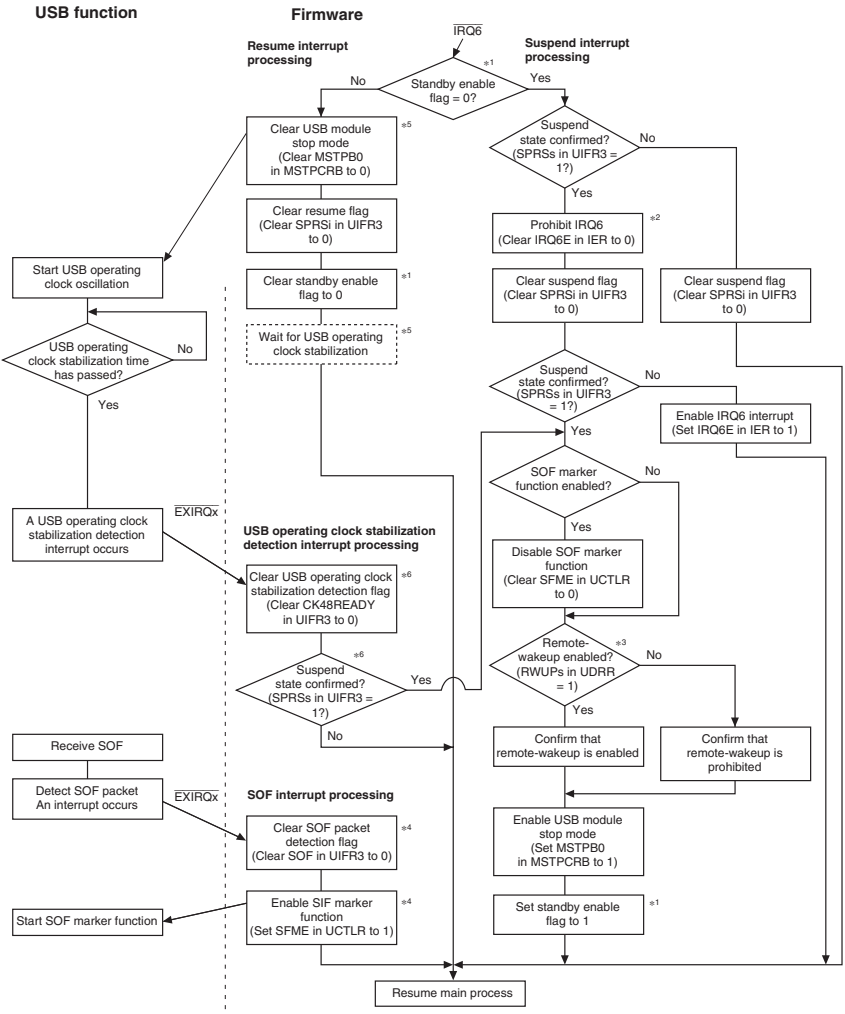


Figure 12.7 Format of Data Written to RSTCSR (Example of WDT0)

Reading from TCNT, TCSR, and RSTCSR: TCNT, TCSR, and RSTCSR are read by using the same method as for the general registers. TCSR, TCNT, and RSTCSR are allocated in addresses H'FF74, H'FF75, and H'FF77 respectively.

(2) Suspend and Resume Interrupt Processing

Figure 15.9 is a flowchart of suspend and resume interrupt processing.



Notes: 1. The standby enable flag is a software flag for controlling transition to the standby state. There is no such hardware flag.
2. Interrupts should be masked from when the IRQ6 interrupt is received until the SLEEP instruction is executed. Finally, unmask the interrupts using the LDC instruction or the like and execute the SLEEP instruction immediately afterward.
3. The remote-wakeup function cannot be used unless it is enabled by the host. Accordingly, the remote-wakeup function cannot be used unless it is enabled by the host. Accordingly, make sure to check RWUPs in UDRR before using the remote-wakeup function. However, it is not necessary to confirm that the remote-wakeup function is enabled by the host if the application does not make use of this function.
4. Make this setting only if the SOF marker function will be used.
5. When resuming by means of remote-wakeup the USB operating clock has already stabilized, so this step is not necessary.
6. Return to the main process and wait for the USB operating clock stabilization detection interrupt. When resuming by means of remote-wakeup the USB operating clock has already stabilized, so this step is not necessary.

Figure 15.9 Example Flowchart of Suspend and Resume Interrupt Processing

(2) Data Stage (Control-In)

The firmware first analyzes command data from the host in the setup stage, and determines the subsequent data stage direction. If the result of command data analysis is that the data stage is in-transfer, one packet of data to be sent to the host is written to the FIFO. If there is more data to be sent, this data is written to the FIFO after the data written first has been sent to the host (EP0iTS of UIFR0 is set to 1).

The end of the data stage is identified when the host transmits an OUT token and the status stage is entered.

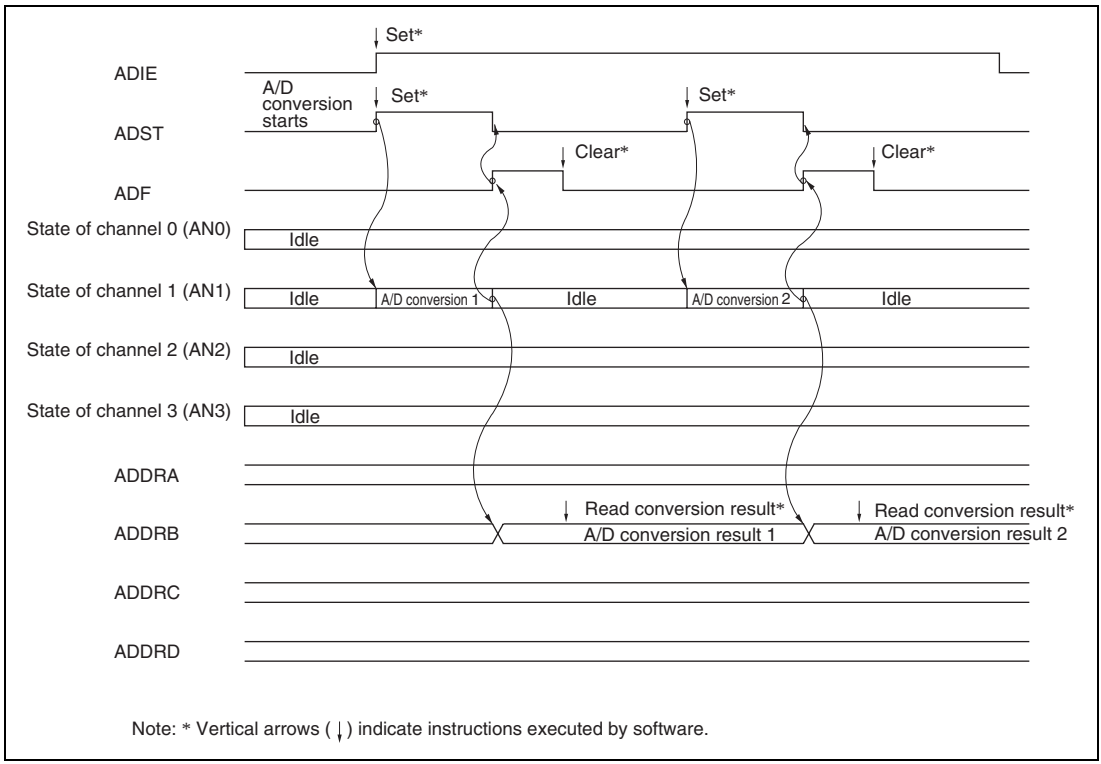


Figure 16.3 A/D Conversion Timing (Single-Chip Mode, Channel 1 Selected)

16.5.2 Scan Mode

In scan mode, A/D conversion is to be performed sequentially on the specified channels (four channels maximum). The operations are as follows.

1. When the ADST bit is set to 1 by software, TPU, or external trigger input, A/D conversion starts on the first channel in the group (AN0 when CH3 and CH2 = 00, AN4 when CH3 and CH2 = 01, or AN8 when CH3 and CH2 = 10).
2. When A/D conversion for each channel is completed, the result is sequentially transferred to the A/D data register corresponding to each channel.
3. When conversion of all the selected channels is completed, the ADF flag is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt is requested after A/D conversion ends. Conversion of the first channel in the group starts again.
4. Steps 2 to 3 are repeated as long as the ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops.

performed normally, initiate boot mode again by a reset. Depending on the host's transfer bit rate and system clock frequency of this LSI, there will be a discrepancy between the bit rates of the host and the chip. To operate the SCI properly, set the host's transfer bit rate and system clock frequency of this LSI within the ranges listed in table 19.5.

5. In boot mode, a part of the on-chip RAM area (4 kbytes) is used by the boot program. Addresses H'FFE000 to H'FFEFBF is the area to which the programming control program is transferred from the host. The boot program area cannot be used until the execution state in boot mode switches to the programming control program.
6. Before branching to the programming control program, the chip terminates transfer operations by the SCI_2 (by clearing the RE and TE bits in SCR to 0), but the adjusted bit rate value remains set in BRR. Therefore, the programming control program can still use it for transfer of write data or verify data with the host. The TxD pin is high. The contents of the CPU general registers are undefined immediately after branching to the programming control program. These registers must be initialized at the beginning of the programming control program, since the stack pointer (SP), in particular, is used implicitly in subroutine calls, etc.
7. Boot mode can be cleared by a reset. End the reset* after driving the reset pin low, waiting at least 20 states, and then setting the FWE pin and the mode (MD) pins. Boot mode is also cleared when a WDT overflow occurs.
8. Do not change the MD pin input levels in boot mode. If the mode pin input levels are changed (for example, from low to high) during a reset, the state of ports with multiplexed address functions and bus control output pins ($\overline{AS}$, $\overline{RD}$, $\overline{WR}$) will change according to the change in the microcomputer's operating mode . Therefore, care must be taken to make pin settings to prevent these pins from becoming output signal pins during a reset, or to prevent collision with signals outside the microcomputer.
9. All interrupts are disabled during programming or erasing of the flash memory.

Note: * Mode pin and FWE pin input must satisfy the mode programming setup time (t_{MDS} = 200 ns) with respect to the reset release timing.

22.6 Module Stop Mode

Module stop mode can be set for individual on-chip supporting modules.

When the corresponding MSTP bit in MSTPCR is set to 1, module operation stops at the end of the bus cycle and a transition is made to module stop mode. The CPU continues operating independently.

When the corresponding MSTP bit is cleared to 0, module stop mode is cleared and the module starts operating at the end of the bus cycle. In module stop mode, the internal states of modules other than the A/D converter are retained.

After reset clearance, all modules other than DTC and DMAC are in module stop mode.

When an on-chip supporting module is in module stop mode, read/write access to its registers is disabled.

When a transition is made to sleep mode with all modules stopped, the bus controller and I/O ports also stop operating, enabling current dissipation to be further reduced.

22.7 φ Clock Output Disabling Function

Output of the φ clock can be controlled by means of the PSTOP bit in SCKCR, and DDR for the corresponding port. When the PSTOP bit is set to 1, the φ clock stops at the end of the bus cycle, and φ output goes high. φ clock output is enabled when the PSTOP bit is cleared to 0. When DDR for the corresponding port is cleared to 0, φ clock output is disabled and input port mode is set. Table 22.4 shows the state of the φ pin in each processing state.

Table 22.4 φ Pin State in Each Processing State

Register Settings					
DDR	**PSTOP**	**Normal Mode**	**Sleep Mode**	**Software Standby Mode**	**Hardware Standby Mode**
0	×	High impedance	High impedance	High impedance	High impedance
1	0	φ output	φ output	Fixed high	High impedance
1	1	Fixed high	Fixed high	Fixed high	High impedance

Legend:
×: Don't care

24.3 DC Characteristics

Table 24.2 lists the DC characteristics. Table 24.3 lists the permissible output currents.

Table 24.2 DC Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = DrV_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = DrV_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)*1

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	$\overline{IRQ0}$ to $\overline{IRQ5}$, $\overline{IRQ7}$	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.8$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.05$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0, $\overline{TRST}$, TCK, TMS, TDI, VBUS, $\overline{UBPM}$, FWE*5	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL, EXTAL48, Ports 1, 3, 7, and A to G		$V_{CC} \times 0.8$	—	V_{CC} + 0.3	V	
	Ports 4*6 and 9		$V_{CC} \times 0.8$	—	AV_{CC} + 0.3*6	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0, $\overline{TRST}$, TCK, TMS, TDI, VBUS, $\overline{UBPM}$, FWE*5	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	EXTAL, EXTAL48, NMI, Ports 1, 3, 4, 7, 9, and A to G		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA

24.4.2 Control Signal Timing

Table 24.5 lists the control signal timing.

Table 24.5 Control Signal Timing

Conditions: V_{CC} = $PLLV_{CC}$ = DrV_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = DrV_{SS} = AV_{SS} = 0 V, φ = 13 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{RES}$ setup time	t_{RESS}	250	—	ns	Figure 24.5
$\overline{RES}$ pulse width	t_{RESW}	20	—	t_{cyc}	
$\overline{MRES}$ setup time	t_{MRESS}	250	—	ns	
$\overline{MRES}$ pulse width	t_{MRESW}	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	250	—	ns	Figure 24.6
NMI hold time	t_{NMIH}	10	—	ns	
NMI pulse width (exiting software standby mode)	t_{NMIW}	200	—	ns	
$\overline{IRQ}$ setup time	t_{IRQS}	250	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	ns	
$\overline{IRQ}$ pulse width (exiting software standby mode)	t_{IRQW}	200	—	ns	

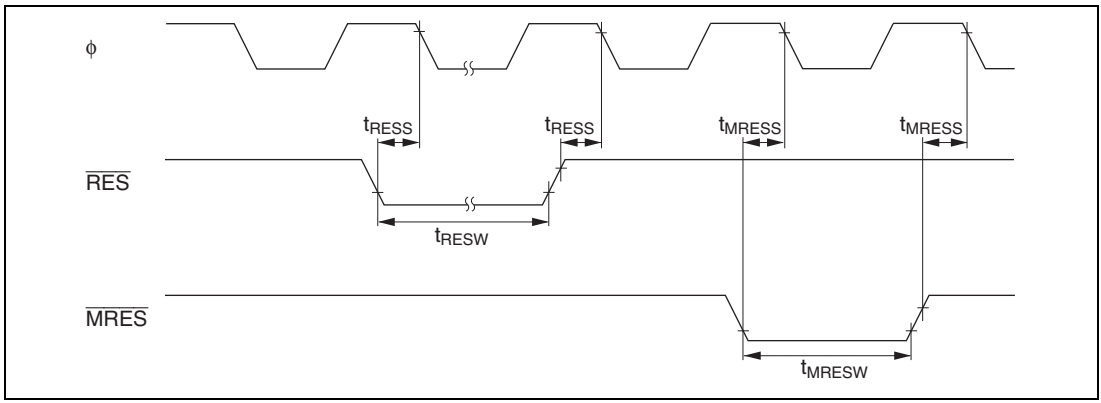


Figure 24.5 Reset Input Timing

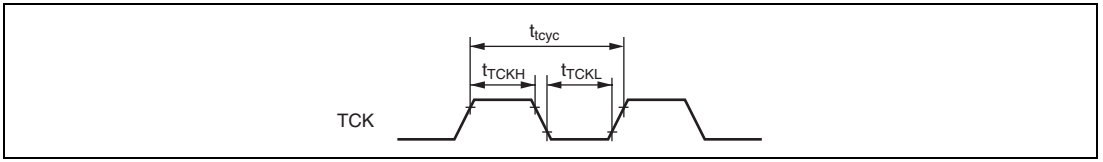


Figure 26.21 Boundary Scan TCK Input Timing

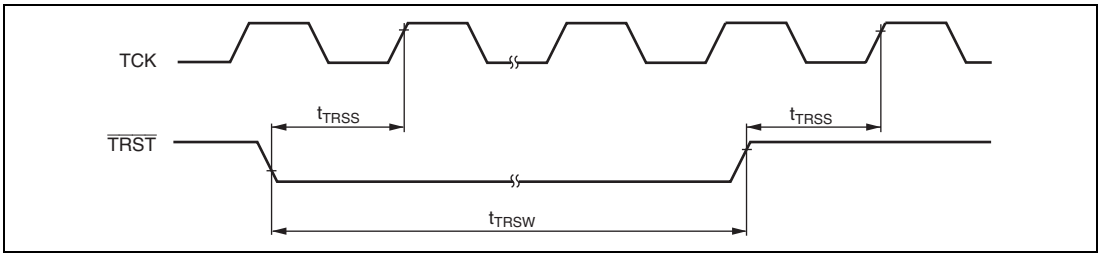


Figure 26.22 Boundary Scan $\overline{TRST}$ Input Timing (At Reset Hold)

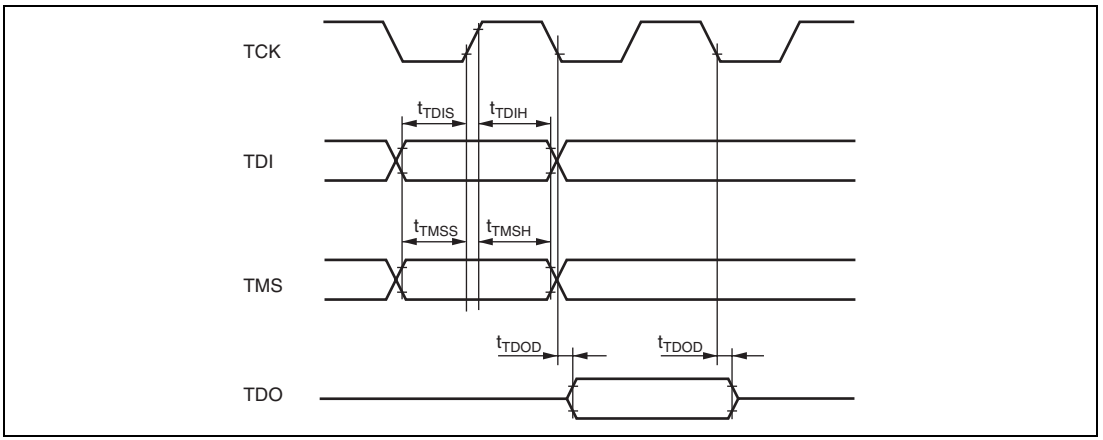


Figure 26.23 Boundary Scan Data Transmission Timing

Section 27 Electrical Characteristics (H8S/2215C)

27.1 Absolute Maximum Ratings

Table 27.1 lists the absolute maximum ratings.

Table 27.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}, $PLLV_{CC}$, DrV_{CC}	–0.3 to +4.3	V
Input voltage (except ports 4 and 9)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (ports 4 and 9)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.3	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85*	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Note: * The operating temperature ranges for flash memory programming/erasing are T_a = –20°C to +75°C.