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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf871t-i-l

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# FIGURE 1-2: PIC16F871 BLOCK DIAGRAM



NOTES:

# 4.3 PORTC and the TRISC Register

PORTC is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin).

PORTC is multiplexed with several peripheral functions (Table 4-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (BSF, BCF, XORWF) with TRISC as the destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

#### FIGURE 4-5:

#### PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)



Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI	bit1	ST	Input/output port pin or Timer1 oscillator input.
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/ PWM1 output.
RC3	bit3	ST	Input/output port pin.
RC4	bit4	ST	Input/output port pin.
RC5	bit5	ST	Input/output port pin.
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive or Synchronous Data.

### TABLE 4-5:PORTC FUNCTIONS

Legend: ST = Schmitt Trigger input

### TABLE 4-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	PORTC	Data Dire	ection Re		1111 1111	1111 1111				

Legend: x = unknown, u = unchanged

# 4.4 PORTD and TRISD Registers

This section is not applicable to the PIC16F870.

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

#### FIGURE 4-6: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL <sup>(1)</sup>	Input/output port pin or parallel slave port bit0.
RD1/PSP1	bit1	ST/TTL <sup>(1)</sup>	Input/output port pin or parallel slave port bit1.
RD2/PSP2	bit2	ST/TTL <sup>(1)</sup>	Input/output port pin or parallel slave port bit2.
RD3/PSP3	bit3	ST/TTL <sup>(1)</sup>	Input/output port pin or parallel slave port bit3.
RD4/PSP4	bit4	ST/TTL <sup>(1)</sup>	Input/output port pin or parallel slave port bit4.
RD5/PSP5	bit5	ST/TTL <sup>(1)</sup>	Input/output port pin or parallel slave port bit5.
RD6/PSP6	bit6	ST/TTL <sup>(1)</sup>	Input/output port pin or parallel slave port bit6.
RD7/PSP7	bit7	ST/TTL <sup>(1)</sup>	Input/output port pin or parallel slave port bit7.

# TABLE 4-7: PORTD FUNCTIONS

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

#### TABLE 4-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	PORTE	) Data D	irection l	Register			1111 1111	1111 1111		
89h	TRISE	IBF	OBF	IBOV	PSPMODE		PORTE Da	ata Directio	n Bits	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PORTD.

# 5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 5-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

Additional information on the Timer0 module is available in the PIC® Mid-Range MCU Family Reference Manual (DS33023).

Timer mode is selected by clearing bit TOCS (OPTION\_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register. Counter mode is selected by setting bit T0CS (OPTION\_REG<5>). In Counter mode, Timer0 will increment either on every rising, or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE (OPTION\_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 5.2.

The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler is not readable or writable. Section 5.3 details the operation of the prescaler.

# 5.1 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP, since the timer is shut-off during SLEEP.

FIGURE 5-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



# 6.7 Resetting of Timer1 Register Pair (TMR1H, TMR1L)

TMR1H and TMR1L registers are not reset to 00h on a POR, or any other RESET, except by the CCP1 special event trigger.

T1CON register is reset to 00h on a Power-on Reset, or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescale. In all other RESETS, the register is unaffected.

# 6.8 Timer1 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

# TABLE 6-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value POR,	e on: BOR	Valu all c RES	e on other ETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	0000	-000	0000	-000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	0000	-000	0000	-000
0Eh	TMR1L	Holding R	egister fo	r the Least	Significant	Byte of the	16-bit TM	R1 Registe	er	xxxx	xxxx	uuuu	uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx	xxxx	uuuu	uuuu
10h	T1CON	_	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F870; always maintain these bits clear.

# 7.0 TIMER2 MODULE

Timer2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time base for the PWM mode of the CCP module(s). The TMR2 register is readable and writable, and is cleared on any device RESET.

The input clock (Fosc/4) has a prescale option of 1:1, 1:4, or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon RESET.

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF (PIR1<1>)).

Timer2 can be shut-off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

Register 7-1 shows the Timer2 control register.

Additional information on timer modules is available in the PIC<sup>®</sup> Mid-Range MCU Family Reference Manual (DS33023).

### FIGURE 7-1: TIMER2 BLOCK DIAGRAM



#### REGISTER 7-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

bit 7	Unimplemented: Read	d as '0'		
bit 6-3	TOUTPS3:TOUTPS0:	Timer2 Output Postscale	e Select bits	
	0000 = 1:1 Postscale			
	0001 = 1:2 Postscale			
	0010 = 1:3 Postscale			
	•			
	•			
	• 1111 = 1:16 Postscale			
bit 2	TMR2ON: Timer2 On b	bit		
	1 = Timer2 is on			
	0 = Timer2 is off			
bit 1-0	T2CKPS1:T2CKPS0: 1	Fimer2 Clock Prescale S	elect bits	
	00 = Prescaler is 1			
	01 = Prescaler is 4			
	1x = Prescaler is 16			
	Legend:			
	R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	

'1' = Bit is set

'0' = Bit is cleared

- n = Value at POR

x = Bit is unknown

When setting up an Asynchronous Transmission, follow these steps:

- 1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH (Section 9.1).
- 2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- 3. If interrupts are desired, then set enable bit TXIE.
- 4. If 9-bit transmission is desired, then set transmit bit TX9.

- 5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Load data to the TXREG register (starts transmission).
- 8. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

### FIGURE 9-2: ASYNCHRONOUS MASTER TRANSMISSION



#### FIGURE 9-3: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)



#### TABLE 9-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	R0IF	x000 0000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	0000 -000	0000 -000
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Tra	nsmit Re	gister						0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	0000 -000	0000 -000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Generato	r Register		0000 0000	0000 0000				

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F870; always maintain these bits clear.

#### 9.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 9-4. The data is received on the RC7/RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter, operating at x16 times the baud rate; whereas, the main receive serial shifter operates at the bit rate or at Fosc.

Once Asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the Receive (Serial) Shift register (RSR). After sampling the STOP bit, the received data in the RSR is transferred to the RCREG register (if it is empty). If the transfer is complete, flag bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read only bit, which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty. The RCREG is a double-buffered register (i.e., it is a two-deep FIFO). It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting to the RSR register. On the detection of the STOP bit of the third byte, if the RCREG register is still full, the overrun error bit OERR (RCSTA<1>) will be set. The word in the RSR will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun bit OERR has to be cleared in software. This is done by resetting the receive logic (CREN is cleared and then set). If bit OERR is set, transfers from the RSR register to the RCREG register are inhibited, and no further data will be received. It is therefore, essential to clear error bit OERR if it is set. Framing error bit FERR (RCSTA<2>) is set if a STOP bit is detected as clear. Bit FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG will load bits RX9D and FERR with new values, therefore, it is essential for the user to read the RCSTA register before reading the RCREG register in order not to lose the old FERR and RX9D information.

Data Bus



Interrupt

#### FIGURE 9-5:

#### **ASYNCHRONOUS RECEPTION**



RCIF

RCIE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	R0IF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	_	CCP1IF	TMR2IF	TMR1IF	0000 -000	0000 -000
18h	RCSTA	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	x00- 0000
1Ah	RCREG	USART R	eceive Re	gister						0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	_	CCP1IE	TMR2IE	TMR1IE	0000 -000	0000 -000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	e Generat		0000 0000	0000 0000					

 TABLE 9-9:
 REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous master reception.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F870; always maintain these bits clear.





#### REGISTER 10-2: ADCON1 REGISTER (ADDRESS: 9Fh)

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	—		PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 ADFM: A/D Result Format Select bit

1 = Right justified. 6 Most Significant bits of ADRESH are read as '0'.
0 = Left justified. 6 Least Significant bits of ADRESL are read as '0'.

bit 6-4 Unimplemented: Read as '0'

bit 3-0 **PCFG3:PCFG0**: A/D Port Configuration Control bits:

PCFG3: PCFG0	AN7 <sup>(1)</sup> RE2	AN6 <sup>(1)</sup> RE1	AN5 <sup>(1)</sup> RE0	AN4 RA5	AN3 RA3	AN2 RA2	AN1 RA1	AN0 RA0	VREF+	VREF-	CHAN/ Refs <sup>(2)</sup>
0000	А	А	А	А	A	А	Α	Α	Vdd	Vss	8/0
0001	А	Α	А	А	VREF+	А	А	А	RA3	Vss	7/1
0010	D	D	D	А	Α	А	А	А	Vdd	Vss	5/0
0011	D	D	D	А	VREF+	А	А	А	RA3	Vss	4/1
0100	D	D	D	D	Α	D	А	А	Vdd	Vss	3/0
0101	D	D	D	D	VREF+	D	А	А	RA3	Vss	2/1
011x	D	D	D	D	D	D	D	D	Vdd	Vss	0/0
1000	А	А	А	А	VREF+	VREF-	А	А	RA3	RA2	6/2
1001	D	D	А	А	А	А	А	А	Vdd	Vss	6/0
1010	D	D	А	А	VREF+	А	А	А	RA3	Vss	5/1
1011	D	D	А	А	VREF+	VREF-	А	А	RA3	RA2	4/2
1100	D	D	D	А	VREF+	VREF-	А	А	RA3	RA2	3/2
1101	D	D	D	D	VREF+	VREF-	А	А	RA3	RA2	2/2
1110	D	D	D	D	D	D	D	А	Vdd	Vss	1/0
1111	D	D	D	D	VREF+	VREF-	D	А	RA3	RA2	1/2

A = Analog input D = Digital I/O

Note 1: These channels are not available on the PIC16F870 device.

**2:** This column indicates the number of analog channels available as A/D inputs and the number of analog channels used as voltage reference inputs.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented b	oit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D result register pair, the GO/DONE bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 10-1.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs. To determine sample time, see Section 10.1. After this acquisition time has elapsed, the A/D conversion can be started.

# 11.3 **RESET**

The PIC16F870/871 differentiates between various kinds of RESET:

- Power-on Reset (POR)
- MCLR Reset during normal operation
- MCLR Reset during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)
- Brown-out Reset (BOR)

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset (POR), on the MCLR and WDT Reset, on MCLR Reset during SLEEP, and Brown-out Reset (BOR). They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation. The  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits are set or cleared differently in different RESET situations, as indicated in Table 11-4. These bits are used in software to determine the nature of the RESET. See Table 11-6 for a full description of RESET states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 11-4.

These devices have a  $\overline{\text{MCLR}}$  noise filter in the  $\overline{\text{MCLR}}$  Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive  $\overline{\text{MCLR}}$  pin low.







FIGURE 11-6: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1



FIGURE 11-7: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



# 11.17 In-Circuit Serial Programming

PIC16F870/871 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware to be programmed.

When using ICSP, the part must be supplied at 4.5V to 5.5V, if a bulk erase will be executed. This includes reprogramming of the code protect, both from an onstate to off-state. For all other cases of ICSP, the part may be programmed at the normal operating voltages. This means calibration values, unique user IDs, or user code can be reprogrammed or added.

For complete details of serial programming, please refer to the EEPROM Memory Programming Specification for the PIC16F87X (DS39025).

# 11.18 Low Voltage ICSP Programming

The LVP bit of the configuration word enables low voltage ICSP programming. This mode allows the microcontroller to be programmed via ICSP, using a VDD source in the operating voltage range. This only means that VPP does not have to be brought to VIHH, but can instead be left at the normal operating voltage. In this mode, the RB3/PGM pin is dedicated to the programming function and ceases to be a general purpose I/O pin. During programming, VDD is applied to the MCLR pin. To enter Programming mode, VDD must be applied to the RB3/PGM pin, provided the LVP bit is set. The LVP bit defaults to on ('1') from the factory.

- Note 1: The High Voltage Programming mode is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR pin.
  - 2: While in Low Voltage ICSP mode, the RB3 pin can no longer be used as a general purpose I/O pin.
  - 3: When using low voltage ICSP programming (LVP) and the pull-ups on PORTB are enabled, bit 3 in the TRISB register must be cleared to disable the pull-up on RB3 and ensure the proper operation of the device.
  - 4: RB3 should not be allowed to float if LVP is enabled. An external pull-down device should be used to default the device to normal Operating mode. If RB3 floats high, the PIC16F870/871 devices will enter Programming mode.
  - LVP mode is enabled by default on all devices shipped from Microchip. It can be disabled by clearing the LVP bit in the CONFIG register.
  - 6: Disabling LVP will provide maximum compatibility to other PIC16CXXX devices.

If Low Voltage Programming mode is not used, the LVP bit can be programmed to a '0' and RB3/PGM becomes a digital I/O pin. However, the LVP bit may only be programmed when programming is entered with VIHH on MCLR. The LVP bit can only be charged when using high voltage on MCLR.

It should be noted, that once the LVP bit is programmed to 0, only the High Voltage Programming mode is available and only High Voltage Programming mode can be used to program the device.

When using low voltage ICSP, the part must be supplied at 4.5V to 5.5V, if a bulk erase will be executed. This includes reprogramming of the code protect bits from an on-state to off-state. For all other cases of low voltage ICSP, the part may be programmed at the normal operating voltage. This means calibration values, unique user IDs, or user code can be reprogrammed or added.

CALL	Call Subroutine
Syntax:	[ <i>label</i> ] CALL k
Operands:	$0 \leq k \leq 2047$
Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

CLRWDT	Clear Watchdog Timer
Syntax:	[label] CLRWDT
Operands:	None
Operation: Status Affected:	$\begin{array}{l} 00h \rightarrow WDT \\ 0 \rightarrow WDT \text{ prescaler,} \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow \overline{PD} \\ \overline{TO}, \overline{PD} \end{array}$
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

CLRF	Clear f
Syntax:	[label] CLRF f
Operands:	$0 \leq f \leq 127$
Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

COMF	Complement f				
Syntax:	[ <i>label</i> ] COMF f,d				
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$				
Operation:	$(\overline{f}) \rightarrow (destination)$				
Status Affected:	Z				
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.				

CLRW	Clear W
Syntax:	[ label ] CLRW
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow (W) \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

DECF	Decrement f
Syntax:	[ label ] DECF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$
Operation:	(f) - 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

# 14.0 ELECTRICAL CHARACTERISTICS

# Absolute Maximum Ratings †

Ambient temperature under bias	55 to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR. and RA4)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	0.3 to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0 to +13.25V
Voltage on RA4 with respect to Vss	0 to +8.5V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, Iık (Vı < 0 or Vı > VDD)	± 20 mA
Output clamp current, Ioк (Vo < 0 or Vo > VDD)	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined) (Note 3)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined) (Note 3)	200 mA
Maximum current sunk by PORTC and PORTD (combined) (Note 3)	200 mA
Maximum current sourced by PORTC and PORTD (combined) (Note 3)	200 mA
<b>Note 1:</b> Power dissipation is calculated as follows: Pdis = VDD x {IDD - $\sum$ IOH} + $\sum$ {(VDD	- VOH) x IOH} + $\Sigma$ (VOI x IOL)
2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80	) mA, may cause latch-up.

- 2: Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin, rather than pulling this pin directly to VSS.
- 3: PORTD and PORTE are not implemented on the 28-pin devices.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### FIGURE 14-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



Param No.	Sym		Characteristic		Min	Тур†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5 TCY + 20	—	_	ns	Must also meet
				With Prescaler	10	_		ns	parameter 42
41*	Tt0L	T0CKI Low Pulse W	/idth	No Prescaler	0.5 TCY + 20	_	_	ns	Must also meet
				With Prescaler	10	—	—	ns	parameter 42
42*	Tt0P	T0CKI Period		No Prescaler	TCY + 40	—	—	ns	
		,		With Prescaler	Greater of: 20 or <u>Tcy + 40</u> N	_	_	ns	N = prescale value (2, 4,, 256)
45*	Tt1H	T1CKI High Time	Synchronous, Pres	scaler = 1	0.5 TCY + 20	_	_	ns	Must also meet
			Synchronous,	Standard(F)	15	—	_	ns	parameter 47
			Prescaler = 2,4,8	Extended(LF)	25	—		ns	
			Asynchronous	Standard(F)	30	—		ns	
				Extended(LF)	50	—		ns	
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5 TCY + 20	—		ns	Must also meet
			Synchronous, Prescaler = 2,4,8 Asynchronous	Standard(F)	15	—	—	ns	parameter 47
				Extended(LF)	25	—	_	ns	
				Standard(F)	30	—	_	ns	
				Extended(LF)	50	—	_	ns	
47*	Tt1P	t1P T1CKI input period	Synchronous	Standard(F)	<u>Greater of:</u> 30 or <u>Tcy + 40</u> N	_		ns	N = prescale value (1, 2, 4, 8)
				Extended(LF)	<u>Greater of:</u> 50 or <u>Tcy + 40</u> N				N = prescale value $(1, 2, 4, 8)$
			Asynchronous	Standard(F)	60	—		ns	
				Extended(LF)	100	—	-	ns	
	Ft1	Timer1 oscillator inp (oscillator enabled b	out frequency range by setting bit T1OSCEN)		DC	—	200	kHz	
48	TCKEZtmr1	Delay from external	clock edge to time	r increment	2 Tosc	—	7 Tosc	_	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



#### TABLE 14-10: A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
130	TAD	A/D clock period	Standard(F)	1.6			μs	Tosc based, VREF $\geq$ 3.0V
			Extended(LF)	3.0		_	μS	Tosc based, VREF $\geq$ 2.0V
			Standard(F)	2.0	4.0	6.0	μS	A/D RC Mode
			Extended(LF)	3.0	6.0	9.0	μS	A/D RC Mode
131	TCNV	Conversion time (not in (Note 1)	cluding S/H time)			12	Tad	
132	TACQ	Acquisition time		(Note 2)	40	_	μS	
					_	_	μs	The minimum time is the ampli- fier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 20.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to A/D clock start			Tosc/2 §		_	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

**Note 1:** ADRES register may be read on the following TCY cycle.

**2:** See Section 10.1 for min conditions.







# 28-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES*		N	<b>MILLIMETERS</b>		
Dimension	MIN	NOM	MAX	MIN	NOM	MAX		
Number of Pins	n		28			28		
Pitch	р		.050			1.27		
Overall Height	Α	.093	.099	.104	2.36	2.50	2.64	
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39	
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30	
Overall Width	E	.394	.407	.420	10.01	10.34	10.67	
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59	
Overall Length	D	.695	.704	.712	17.65	17.87	18.08	
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74	
Foot Length	L	.016	.033	.050	0.41	0.84	1.27	
Foot Angle Top	¢	0	4	8	0	4	8	
Lead Thickness	С	.009	.011	.013	0.23	0.28	0.33	
Lead Width	В	.014	.017	.020	0.36	0.42	0.51	
Mold Draft Angle Top	α	0	12	15	0	12	15	
Mold Draft Angle Bottom	β	0	12	15	0	12	15	

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013

Drawing No. C04-052