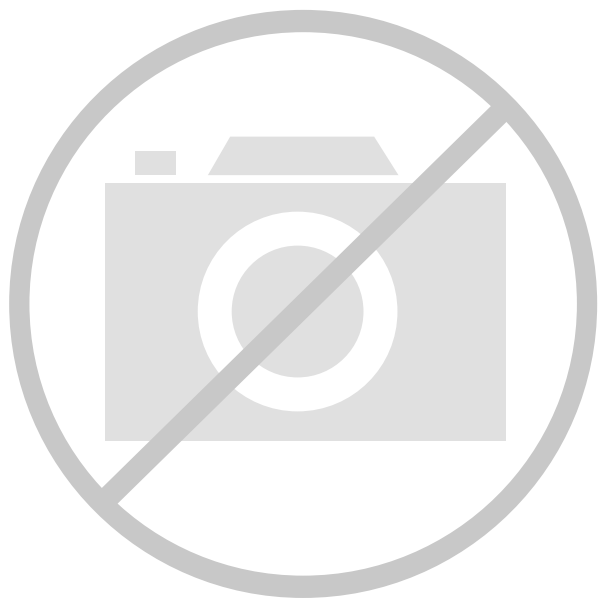




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BCBGA, FCBGA
Supplier Device Package	1152-CFCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga115e-5fc1152i

toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-9 illustrates the DCS Block diagram.

Figure 2-9. DCS Block Diagram

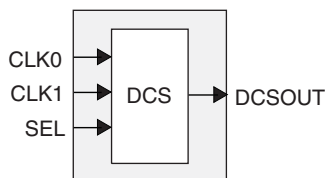
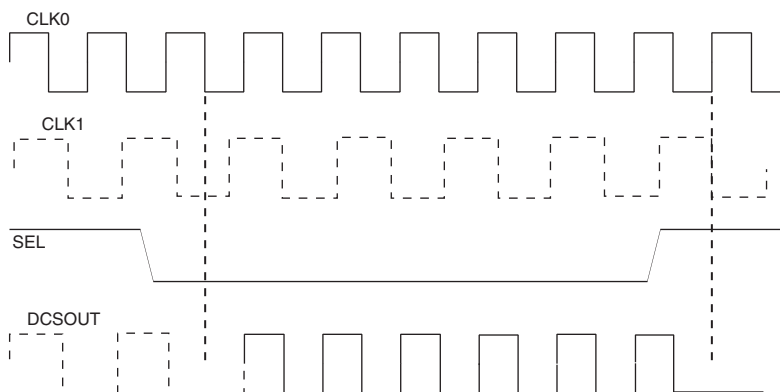


Figure 2-10 shows timing waveforms for one of the DCS operating modes. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-10. DCS Waveforms



Clock Boosting

There are programmable delays available in the clock signal paths in the PFU, PIC and EBR blocks. These allow setup and clock-to-output times to be traded to meet critical timing without slowing the system clock. If this feature is enabled then the design tool automatically uses these delays to improve timing performance.

Global Set/Reset

There is a global set/reset (GSR) network on the device that is distributed to all FFs, PLLs, DLLs and other blocks on the device. This GSR network can operate in two modes:

- asynchronous - no clock is required to get into or out of the reset state.
- synchronous - The global GSR net is synchronized to a user selected clock. In this mode it continues to be asynchronous to get into the reset state, but is synchronous to get out of the reset state. This allows all registers on the device to become operational in the same clock period. The synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met (not from the GSR being released).

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider and two clock output dividers. The input divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal.

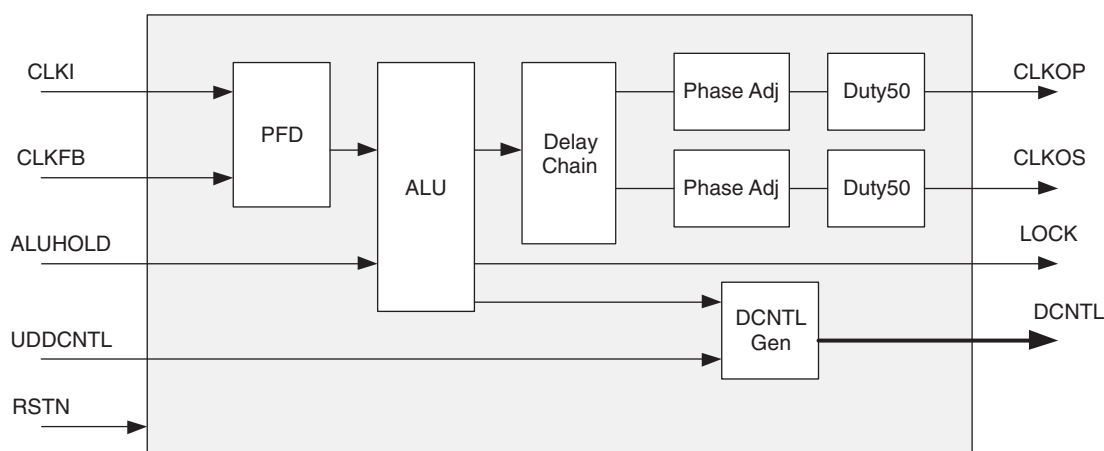
There is a Digital Control (DCNTL) bus available from the DLL block. This Digital Control bus is available to the delay lines in the PIC blocks in the adjacent banks. The UDDCNTL signal allows the user to latch the current value on the digital control bus.

Figure 2-12 shows the DLL block diagram of the DLL inputs and outputs. The output of the phase frequency detector controls an arithmetic logic unit (ALU) to add or subtract one delay tap. The digital output of this ALU is used to control the delay value of the delay chain and this digital code is transmitted via the DCNTL bus.

The sysCLOCK DLL can be configured at power-up, then, if desired, reconfigured dynamically through the Serial Memory Interface bus which interfaces with the on-chip Microprocessor Interface (MPI) bus. In addition, users can drive the SMI interface from routing if desired.

The user can configure the DLL for many common functions such as clock injection match and single delay cell. Lattice provides primitives in its design for time reference delay (DDR memory) and clock injection delay removal.

Figure 2-12. DLL Diagram



PLL/DLL Cascading

The LatticeSC devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are as follows:

- PLL to PLL
- PLL to DLL
- DLL to DLL
- DLL to PLL

DLLs are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLL and PLLs.

When cascading the DLL to the PLL, the DLL can be used to drive the PLL to create fine phase shifts of an input clock signal. Figure 2-13 shows a shift of all outputs for CLKOP and CLKOS out in time.

3. Bottom Side (Banks 4 and 5)

These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but true HLVDS and RSDS differential drivers are not available. Adaptive input logic is available on PIOs A or C.

Table 2-8 lists the standards supported by each side.

Table 2-8. I/O Standards Supported by Different Banks

Description	Top Side Banks 1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
I/O Buffer Type	Single-ended, Differential Receiver	Single-ended, Differen- tial Receiver and Driver	Single-ended, Differential Receiver	Single-ended, Differen- tial Receiver and Driver
Output Standards Supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_I, II SSTL33_I, II HSTL15_I, II, III ¹ , IV ¹ HSTL18_I, II, III ¹ , IV ¹ SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL ² , GTL+ ²	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_I, II HSTL15_I, III HSTL18_I, II, III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL ² , GTL+ ²	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_I, II SSTL33_I, II HSTL15_I, II, III ¹ , IV ¹ HSTL18_I, II, III ¹ , IV ¹ SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL ² , GTL+ ²	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_I, II HSTL15_I, III HSTL18_I, II, III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL ² , GTL+ ²
Input Standards Supported	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Clock Inputs	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Differential Output Support via Emulation	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL
AIL Support	No	Yes	Yes	Yes

1. Input only.

2. Input only. Outputs supported by bussing multiple outputs together.

Supported Standards

The LatticeSC PURESPEED I/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 12, 15, 18, 25 and 33 standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, termination resistance, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL, HSTL, GTL (input only), GTL+ (input only), PCI33, PCIX33, PCIX15, AGP-1X33 and AGP-2X33. Differential standards supported include LVDS, RSDS, BLVDS, MLVDS, LVPECL, differential SSTL and differential HSTL. Tables 12 and 13 show the I/O standards (together with their supply and reference voltages) supported by the LatticeSC devices. The tables also provide the available internal termination schemes. For further information on utilizing the PURESPEED I/O buffer to support a variety of standards please see details of additional technical documentation at the end of this data sheet.

Single Ended Inputs: The SC devices support a number of different termination schemes for single ended inputs:

- Parallel to V_{CCIO} or GND
- Parallel to $V_{CCIO}/2$
- Parallel to V_{TT}

Figure 2-28 shows the single ended input schemes that are supported. The nominal values of the termination resistors are shown in Table 2-9.

Figure 2-28. Input Termination Schemes

Termination Type	Discrete Off-Chip Solution	Lattice On-Chip Solution
Parallel termination to to V_{CCIO} , or parallel to GND receiving end		
Parallel termination to $V_{CCIO}/2$ receiving end		
Parallel termination to V_{TT} at receiving end		

In many situations designers can chose whether to use Thevenin or parallel to V_{TT} termination. The Thevenin approach has the benefit of not requiring a termination voltage to be applied to the device. The parallel to V_{TT} approach consumes less power.

VTT Termination Resources

Each I/O bank, except bank 1, has a number of V_{TT} pins that must be connected if V_{TT} is used. Note V_{TT} pins can sink or source current and the power supply they are connected to must be able to handle the relatively high currents associated with the termination circuits. Note: V_{TT} is not available in all package styles.

On-chip parallel termination to V_{TT} is supported at the receiving end only. On-chip parallel output termination to V_{TT} is not supported.

The V_{TT} internal bus is also connected to the internal V_{CMT} node. Thus in one bank designers can implement either V_{TT} termination or V_{CMT} termination for differential inputs.

DDRII/RLDRAMII Termination Support

The DDR II memory and RLDRAMII (in Bidirection Data mode) standards require that the on-chip termination to V_{TT} be turned on when a pin is an input and off when the pin is an output. The LatticeSC devices contain the required circuitry to support this behavior. For additional detail refer to technical information at the end of the data sheet.

PURESPEED I/O Recommended Operating Conditions

Standard	V _{CCIO} (V)			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 33	3.135	3.3	3.465	—	—	—
LVC MOS 25	2.375	2.5	2.625	—	—	—
LVC MOS 18	1.71	1.8	1.89	—	—	—
LVC MOS 15	1.425	1.5	1.575	—	—	—
LVC MOS 12	1.14	1.2	1.26	—	—	—
LV TTL	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
PCIX33	3.135	3.3	3.465	—	—	—
PCIX15	1.425	1.5	1.575	0.49V _{CCIO}	0.5V _{CCIO}	0.51V _{CCIO}
AGP1X33	3.135	3.3	3.465	—	—	—
AGP2X33	3.135	3.3	3.465	0.39V _{CCIO}	0.4V _{CCIO}	0.41V _{CCIO}
SSTL18_I, II ³	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II ³	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II ³	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I, II ³	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15_III ^{1,3} and IV ^{1,3}	1.425	1.5	1.575	0.68	0.9	0.9
HSTL 18_I ³ , II ³	1.71	1.8	1.89	0.816	0.9	1.08
HSTL 18_III ^{1,3} , IV ^{1,3}	1.71	1.8	1.89	0.816	1.08	1.08
GTL12 ^{1,3} , GTLPLUS15 ^{1,3}	—	—	—	0.882	1.0	1.122
LVDS	—	—	—	—	—	—
Mini-LVDS	—	—	—	—	—	—
RSDS	—	—	—	—	—	—
LVPECL33 (outputs) ²	3.135	3.3	3.465	—	—	—
LVPECL33 (inputs) ^{2,4}	—	≤ 2.5	—	—	—	—
BLVDS25 ^{2,3}	2.375	2.5	2.625	—	—	—
MLVDS25 ^{2,3}	2.375	2.5	2.625	—	—	—
SSTL18D_I ³ , II ³	1.71	1.8	1.89	—	—	—
SSTL25D_I ³ , II ³	2.375	2.5	2.625	—	—	—
SSTL33D_I ³ , II ³	3.135	3.3	3.465	—	—	—
HSTL15D_I ³ , II ³	1.425	1.5	1.575	—	—	—
HSTL18D_I ³ , II ³	1.71	1.8	1.89	—	—	—

1. Input only.

2. Inputs on chip. Outputs are implemented with the addition of external resistors.

3. Input for this standard does not depend on the value of V_{CCIO}.

4. Inputs for this standard cannot be in 3.3V VCCIO banks (≤ 2.5V only).

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
GTLPLUS15	GTLPLUS15	-0.013	-0.017	0.012	0.004	0.037	0.024	ns
GTL12	GTL12	-0.063	-0.071	-0.007	-0.048	0.056	-0.032	ns
Output Adjusters								
LVDS	LVDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
RSDS	RSDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
BLVDS25	BLVDS	-0.129	0.05	-0.136	0.069	-0.136	0.083	ns
MLVDS25	MLVDS	-0.059	0.059	-0.057	0.096	-0.054	0.133	ns
LVPECL33	LVPECL	-0.334	-0.181	-0.325	-1.389	-0.315	-2.598	ns
HSTL18_I	HSTL_18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18_II	HSTL_18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL18D_I	Differential HSTL 18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18D_II	Differential HSTL 18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL15_I	HSTL_15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15_II	HSTL_15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
HSTL15D_I	Differential HSTL 15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15D_II	Differential HSTL 15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
SSTL33_I	SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33_II	SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL33D_I	Differential SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33D_II	Differential SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL25_I	SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25_II	SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL25D_I	Differential SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25D_II	Differential SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL18_I	SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18_II	SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
SSTL18D_I	Differential SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18D_II	Differential SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
LVTTTL33_8mA	LVTTTL 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVTTTL33_16mA	LVTTTL 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVTTTL33_24mA	LVTTTL 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVC MOS33_24mA	LVC MOS 3.3 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive	-0.174	0.004	-0.195	0.002	-0.215	0	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive	0	0	0	0	0	0	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive	0.094	-0.025	0.107	0.096	0.12	0.216	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive	0.145	-0.054	0.162	0.063	0.181	0.179	ns
LVC MOS25_OD	LVC MOS 2.5 open drain	0.073	-0.125	0.081	-0.081	0.091	-0.09	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive	-0.278	-0.099	-0.312	-0.115	-0.345	-0.131	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive	-0.073	-0.078	-0.078	-0.084	-0.083	-0.089	ns

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.024	-0.106	0.019	-0.004	0.016	0.099	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.074	-0.134	0.08	-0.022	0.088	0.089	ns
LVC MOS18_OD	LVC MOS 1.8 open drain	0.002	-0.206	0	-0.196	-0.002	-0.221	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	-0.344	-0.164	-0.379	-0.186	-0.412	-0.209	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	-0.125	-0.137	-0.145	-0.157	-0.164	-0.176	ns
LVC MOS15_12mA	LVC MOS 1.5 12mA drive	-0.027	-0.166	-0.043	-0.07	-0.059	0.026	ns
LVC MOS15_16mA	LVC MOS 1.5 16mA drive	0.025	-0.195	0.013	-0.089	0.003	0.017	ns
LVC MOS15_OD	LVC MOS 1.5 open drain	-0.047	-0.267	-0.067	-0.267	-0.087	-0.299	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	-0.473	-0.293	-0.505	-0.317	-0.537	-0.34	ns
LVC MOS12_4mA	LVC MOS 1.2 4mA drive	-0.218	-0.239	-0.25	-0.271	-0.28	-0.303	ns
LVC MOS12_8mA	LVC MOS 1.2 8mA drive	-0.109	-0.269	-0.143	-0.181	-0.176	-0.093	ns
LVC MOS12_12mA	LVC MOS 1.2 12mA drive	-0.054	-0.3	-0.085	-0.203	-0.114	-0.106	ns
LVC MOS12_OD	LVC MOS 1.2 open drain	-0.126	-0.371	-0.166	-0.398	-0.204	-0.43	ns
PCI33	PCI	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX33	PCI-X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX15	PCI-X 1.5	0.208	0.227	0.233	0.312	0.259	0.398	ns
AGP1X33	AGP-1X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
AGP2X33	AGP-2X	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB47C	4	PCLKT4_6	PB54C	4	PCLKT4_6
AH10	PB47D	4	PCLKC4_6	PB54D	4	PCLKC4_6
AK12	PB49A	4	PCLKT4_0	PB55A	4	PCLKT4_0
AJ12	PB49B	4	PCLKC4_0	PB55B	4	PCLKC4_0
AF14	PB49C	4	VREF2_4	PB55C	4	VREF2_4
AE14	PB49D	4		PB55D	4	
AL11	PB51A	4	PCLKT4_5	PB57A	4	PCLKT4_5
AL10	PB51B	4	PCLKC4_5	PB57B	4	PCLKC4_5
AH9	PB51C	4		PB57C	4	
AH8	PB51D	4		PB57D	4	
AK11	PB52A	4	PCLKT4_3	PB58A	4	PCLKT4_3
AJ11	PB52B	4	PCLKC4_3	PB58B	4	PCLKC4_3
AH7	PB52C	4	PCLKT4_4	PB58C	4	PCLKT4_4
AH6	PB52D	4	PCLKC4_4	PB58D	4	PCLKC4_4
AK8	PB53A	4		PB67A	4	
AJ8	PB53B	4		PB67B	4	
AF11	PB53C	4		PB67C	4	
AD12	PB55A	4		PB69A	4	
AE12	PB55B	4		PB69B	4	
AM6	PB56A	4		PB70A	4	
AM5	PB56B	4		PB70B	4	
AC12	PB56C	4		PB70C	4	
AL6	PB57A	4		PB73A	4	
AL5	PB57B	4		PB73B	4	
AG7	PB59A	4		PB74A	4	
AG8	PB59B	4		PB74B	4	
AK6	PB60A	4		PB75A	4	
AJ6	PB60B	4		PB75B	4	
AF10	PB60C	4		PB75C	4	
AE11	PB60D	4		PB75D	4	
AM4	PB61A	4		PB77A	4	
AM3	PB61B	4		PB77B	4	
AH5	PB63A	4		PB78A	4	
AH4	PB63B	4		PB78B	4	
AK5	PB64A	4		PB79A	4	
AJ5	PB64B	4		PB79B	4	
AF8	PB64C	4		PB79C	4	
AF7	PB64D	4		PB79D	4	
AL4	PB65A	4		PB81A	4	
AL3	PB65B	4		PB81B	4	
AG5	PB65C	4		PB81C	4	
AF6	PB65D	4		PB81D	4	
AK3	PB67A	4		PB82A	4	
AJ3	PB67B	4		PB82B	4	
AE10	PB67C	4	VREF1_4	PB82C	4	VREF1_4
AD10	PB67D	4		PB82D	4	
AL2	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AK2	PB68B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AE9	PB68C	4		PB83C	4	
AE8	PB68D	4		PB83D	4	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AC19	VTT_5	5		VTT_5	5	
AC20	VTT_5	5		VTT_5	5	
AD22	VTT_5	5		VTT_5	5	
AB24	VTT_6	6		VTT_6	6	
W23	VTT_6	6		VTT_6	6	
Y23	VTT_6	6		VTT_6	6	
N24	VTT_7	7		VTT_7	7	
R23	VTT_7	7		VTT_7	7	
T23	VTT_7	7		VTT_7	7	
M12	VDDAX25_R	-		VDDAX25_R	-	
M23	VDDAX25_L	-		VDDAX25_L	-	
Y16	GND	-		GND	-	
Y14	GND	-		GND	-	
N21	VCC12	-		VCC12	-	
P22	VCC12	-		VCC12	-	
AA22	VCC12	-		VCC12	-	
AB21	VCC12	-		VCC12	-	
AB14	VCC12	-		VCC12	-	
AA13	VCC12	-		VCC12	-	
P13	VCC12	-		VCC12	-	
N14	VCC12	-		VCC12	-	
G26	NC	-		NC	-	
G9	NC	-		NC	-	
J12	NC	-		NC	-	
H12	NC	-		NC	-	
H23	NC	-		NC	-	
J23	NC	-		NC	-	

1. Differential pair grouping within a PCI is A (True) and B (complement) and C (True) and D (Complement).

2. The LatticeSC/M40 and LatticeSC/M80 in an 1152-pin package support a 32-bit MPI interface.

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP27	PB26A	5	
AP26	PB26B	5	
AK25	PB26C	5	
AK24	PB26D	5	
AN25	PB29A	5	
AN24	PB29B	5	
AE22	PB29C	5	
AE21	PB29D	5	
AM26	PB31A	5	
AM25	PB31B	5	
AF22	PB31C	5	
AF21	PB31D	5	
AN23	PB47A	5	
AN22	PB47B	5	
AP23	PB57A	5	
AP22	PB57B	5	
AG21	PB57C	5	
AG20	PB57D	5	
AP25	PB50A	5	PCLKT5_3
AP24	PB50B	5	PCLKC5_3
AD21	PB50C	5	PCLKT5_4
AD20	PB50D	5	PCLKC5_4
AL23	PB51A	5	PCLKT5_5
AL22	PB51B	5	PCLKC5_5
AH24	PB51C	5	
AH23	PB51D	5	
AM23	PB53A	5	PCLKT5_0
AM22	PB53B	5	PCLKC5_0
AJ24	PB53C	5	
AJ23	PB53D	5	VREF2_5
AN21	PB54A	5	PCLKT5_1
AN20	PB54B	5	PCLKC5_1
AE19	PB54C	5	PCLKT5_6
AD19	PB54D	5	PCLKC5_6
AK21	PB55A	5	PCLKT5_2
AK20	PB55B	5	PCLKC5_2
AK23	PB55C	5	PCLKT5_7
AK22	PB55D	5	PCLKC5_7
AL20	PB58A	5	
AL19	PB58B	5	
AG19	PB58C	5	
AF19	PB58D	5	
AP21	PB61A	5	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
L21	PT55D	1	A16/MPI_ADDR30
L20	PT55C	1	D13/MPI_DATA13
D20	PT55B	1	A15/MPI_ADDR29
E20	PT55A	1	A17/MPI_ADDR31
L19	PT54D	1	A19/MPI_TSI21
K19	PT54C	1	A20/MPI_BDIP
D21	PT54B	1	A18/MPI_TSI20
E21	PT54A	1	MPI_TEA
M20	PT51D	1	D14/MPI_DATA14
M19	PT51C	1	DP1/MPI_PAR1
F21	PT51B	1	A21/MPI_BURST
G21	PT51A	1	D15/MPI_DATA15
H24	B_REFCLKP_L	-	
J24	B_REFCLKN_L	-	
L22	VCC12	-	
E26	B_VDDIB3_L	-	
G22	VCC12	-	
E22	B_HDINP3_L	-	PCS 361 CH 3 IN P
F22	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
L24	VCC12	-	
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D22	B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D23	B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
K24	VCC12	-	
F23	B_HDINN2_L	-	PCS 361 CH 2 IN N
E23	B_HDINP2_L	-	PCS 361 CH 2 IN P
D26	B_VDDIB2_L	-	
G23	VCC12	-	
D27	B_VDDIB1_L	-	
G24	VCC12	-	
E24	B_HDINP1_L	-	PCS 361 CH 1 IN P
F24	B_HDINN1_L	-	PCS 361 CH 1 IN N
A23	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L25	VCC12	-	
B23	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-	
B24	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-	
A24	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
K25	VCC12	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
F25	B_HDINN0_L	-	PCS 361 CH 0 IN N
E25	B_HDINP0_L	-	PCS 361 CH 0 IN P
D28	B_VDDIB0_L	-	
G25	VCC12	-	
D29	A_VDDIB3_L	-	
C25	VCC12	-	
A25	A_HDINP3_L	-	PCS 360 CH 3 IN P
B25	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
E27	VCC12	-	
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
F26	A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
F27	A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E28	VCC12	-	
B28	A_HDINN2_L	-	PCS 360 CH 2 IN N
A28	A_HDINP2_L	-	PCS 360 CH 2 IN P
D30	A_VDDIB2_L	-	
C28	VCC12	-	
D31	A_VDDIB1_L	-	
C29	VCC12	-	
A29	A_HDINP1_L	-	PCS 360 CH 1 IN P
B29	A_HDINN1_L	-	PCS 360 CH 1 IN N
A30	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
E29	VCC12	-	
B30	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
F28	A_VDDOB1_L	-	
B31	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
F29	A_VDDOB0_L	-	
A31	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E30	VCC12	-	
B32	A_HDINN0_L	-	PCS 360 CH 0 IN N
A32	A_HDINP0_L	-	PCS 360 CH 0 IN P
D32	A_VDDIB0_L	-	
C32	VCC12	-	
E34	PL30A	7	
F34	PL30B	7	
F33	PL34A	7	
G33	PL34B	7	
K30	PL38A	7	
L30	PL38B	7	
G34	PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCI/O Bank	Dual Function	Ball Function	VCCI/O Bank	Dual Function
AY41	PB12A	5		PB13A	5	
BA41	PB12B	5		PB13B	5	
AT39	PB12C	5		PB13C	5	
AT38	PB12D	5		PB13D	5	
AV37	PB13A	5		PB15A	5	
AV36	PB13B	5		PB15B	5	
AM31	PB13C	5		PB15C	5	
AM32	PB13D	5		PB15D	5	
BA40	PB15A	5		PB16A	5	
BB40	PB15B	5		PB16B	5	
AM29	PB15C	5		PB16C	5	
AL29	PB15D	5		PB16D	5	
AY39	PB16A	5		PB17A	5	
AY38	PB16B	5		PB17B	5	
AN33	PB16C	5		PB17C	5	
AN32	PB16D	5		PB17D	5	
BA39	PB17A	5		PB19A	5	
BA38	PB17B	5		PB19B	5	
AT37	PB17C	5		PB19C	5	
AT36	PB17D	5		PB19D	5	
AW36	PB19A	5		PB20A	5	
AW35	PB19B	5		PB20B	5	
AM28	PB19C	5		PB20C	5	
AL28	PB19D	5		PB20D	5	
BB38	PB20A	5		PB21A	5	
BB39	PB20B	5		PB21B	5	
AR34	PB20C	5		PB21C	5	
AR33	PB20D	5		PB21D	5	
AV35	PB21A	5		PB23A	5	
AV34	PB21B	5		PB23B	5	
AT33	PB21C	5		PB23C	5	
AT34	PB21D	5		PB23D	5	
BA37	PB23A	5		PB25A	5	
BA36	PB23B	5		PB25B	5	
AP33	PB23C	5		PB25C	5	
AP32	PB23D	5		PB25D	5	
AY36	PB24A	5		PB26A	5	
AY35	PB24B	5		PB26B	5	
AN31	PB24C	5		PB26C	5	
AN30	PB24D	5		PB26D	5	
BB37	PB25A	5		PB27A	5	
BB36	PB25B	5		PB27B	5	
AP31	PB25C	5		PB27C	5	
AP30	PB25D	5		PB27D	5	
AV33	PB27A	5		PB29A	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BA19	PB73A	4		PB87A	4	
BA18	PB73B	4		PB87B	4	
AU19	PB73C	4		PB87C	4	
AU18	PB73D	4		PB87D	4	
AV19	PB74A	4	PCLKT4_2	PB89A	4	PCLKT4_2
AV18	PB74B	4	PCLKC4_2	PB89B	4	PCLKC4_2
AN19	PB74C	4	PCLKT4_7	PB89C	4	PCLKT4_7
AP19	PB74D	4	PCLKC4_7	PB89D	4	PCLKC4_7
BB17	PB75A	4	PCLKT4_1	PB90A	4	PCLKT4_1
BB16	PB75B	4	PCLKC4_1	PB90B	4	PCLKC4_1
AT19	PB75C	4	PCLKT4_6	PB90C	4	PCLKT4_6
AT18	PB75D	4	PCLKC4_6	PB90D	4	PCLKC4_6
BA17	PB77A	4	PCLKT4_0	PB91A	4	PCLKT4_0
BA16	PB77B	4	PCLKC4_0	PB91B	4	PCLKC4_0
AR19	PB77C	4	VREF2_4	PB91C	4	VREF2_4
AR18	PB77D	4		PB91D	4	
AY17	PB79A	4	PCLKT4_5	PB93A	4	PCLKT4_5
AY16	PB79B	4	PCLKC4_5	PB93B	4	PCLKC4_5
AN18	PB79C	4		PB93C	4	
AP18	PB79D	4		PB93D	4	
AW17	PB80A	4	PCLKT4_3	PB94A	4	PCLKT4_3
AW16	PB80B	4	PCLKC4_3	PB94B	4	PCLKC4_3
AU17	PB80C	4	PCLKT4_4	PB94C	4	PCLKT4_4
AU16	PB80D	4	PCLKC4_4	PB94D	4	PCLKC4_4
AV17	PB81A	4		PB95A	4	
AV16	PB81B	4		PB95B	4	
AL18	PB81C	4		PB95C	4	
AM18	PB81D	4		PB95D	4	
BB15	PB83A	4		PB97A	4	
BB14	PB83B	4		PB97B	4	
AP17	PB83C	4		PB97C	4	
AN17	PB83D	4		PB97D	4	
BA15	PB84A	4		PB98A	4	
BA14	PB84B	4		PB98B	4	
AT16	PB84C	4		PB98C	4	
AT15	PB84D	4		PB98D	4	
AV15	PB85A	4		PB99A	4	
AV14	PB85B	4		PB99B	4	
AR16	PB85C	4		PB99C	4	
AR15	PB85D	4		PB99D	4	
AY14	PB87A	4		PB101A	4	
AY13	PB87B	4		PB101B	4	
AU15	PB87C	4		PB101C	4	
AU14	PB87D	4		PB101D	4	
BB13	PB88A	4		PB102A	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP8	PB117D	4		PB131D	4	
AY3	PB119A	4		PB133A	4	
AW3	PB119B	4		PB133B	4	
AR6	PB119C	4		PB133C	4	
AR5	PB119D	4		PB133D	4	
AU5	PB120A	4		PB134A	4	
AV5	PB120B	4		PB134B	4	
AL12	PB120C	4		PB134C	4	
AL11	PB120D	4		PB134D	4	
AV3	PB121A	4		PB135A	4	
AV4	PB121B	4		PB135B	4	
AN9	PB121C	4		PB135C	4	
AN8	PB121D	4		PB135D	4	
AW1	PB123A	4		PB138A	4	
AY1	PB123B	4		PB138B	4	
AK14	PB123C	4	VREF1_4	PB138C	4	VREF1_4
AK13	PB123D	4		PB138D	4	
AV2	PB124A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB139A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AW2	PB124B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB139B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AM10	PB124C	4		PB139C	4	
AM9	PB124D	4		PB139D	4	
AV1	PB125A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB141A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AU1	PB125B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB141B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AL10	PB125C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB141C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AL9	PB125D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB141D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AT3	PROBE_VCC	-		PROBE_VCC	-	
AU2	PROBE_GND	-		PROBE_GND	-	
AP7	PR95D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR117D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AN7	PR95C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR117C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AR3	PR95B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR117B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AR4	PR95A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR117A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AP6	PR94D	3		PR116D	3	
AN6	PR94C	3		PR116C	3	
AT2	PR94B	3		PR116B	3	
AR2	PR94A	3		PR116A	3	
AM6	PR93D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR115D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AL6	PR93C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR115C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AP5	PR93B	3		PR115B	3	
AN5	PR93A	3		PR115A	3	
AL8	PR91D	3		PR112D	3	
AK8	PR91C	3		PR112C	3	
AP2	PR91B	3		PR112B	3	
AN2	PR91A	3		PR112A	3	
AJ12	PR90D	3		PR109D	3	
AH12	PR90C	3		PR109C	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AE1	PR74A	3		PR88A	3	
AF12	PR73D	3		PR87D	3	
AE12	PR73C	3		PR87C	3	
AF2	PR73B	3		PR87B	3	
AE2	PR73A	3		PR87A	3	
AF11	PR72D	3		PR86D	3	
AE11	PR72C	3		PR86C	3	
AF5	PR72B	3		PR86B	3	
AE5	PR72A	3		PR86A	3	
AF10	PR69D	3		PR83D	3	
AE10	PR69C	3		PR83C	3	
AD1	PR69B	3		PR83B	3	
AC1	PR69A	3		PR83A	3	
AF9	PR68D	3		PR82D	3	
AE9	PR68C	3		PR82C	3	
AD2	PR68B	3		PR82B	3	
AC2	PR68A	3		PR82A	3	
AF6	PR67D	3		PR81D	3	
AE6	PR67C	3		PR81C	3	
AD3	PR67B	3		PR81B	3	
AC3	PR67A	3		PR81A	3	
AE8	PR65D	3		PR79D	3	
AD8	PR65C	3		PR79C	3	
AD4	PR65B	3		PR79B	3	
AC4	PR65A	3		PR79A	3	
AE7	PR64D	3		PR78D	3	
AD7	PR64C	3		PR78C	3	
AD5	PR64B	3		PR78B	3	
AC5	PR64A	3		PR78A	3	
AD6	PR63D	3		PR77D	3	
AC6	PR63C	3		PR77C	3	
AB1	PR63B	3		PR77B	3	
AA1	PR63A	3		PR77A	3	
AD9	PR61D	3		PR75D	3	
AC9	PR61C	3		PR75C	3	
AB2	PR61B	3		PR75B	3	
AA2	PR61A	3		PR75A	3	
AD14	PR60D	3		PR74D	3	
AC14	PR60C	3		PR74C	3	
AB5	PR60B	3		PR74B	3	
AA5	PR60A	3		PR74A	3	
AD10	PR59D	3		PR73D	3	
AC10	PR59C	3		PR73C	3	
Y1	PR59B	3		PR73B	3	
W1	PR59A	3		PR73A	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K14	VCC12	-		VCC12	-	
H11	B_VDDIB2_R	-		B_VDDIB2_R	-	
D8	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
E8	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
G5	VCC12	-		VCC12	-	
B9	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
L12	B_VDDOB2_R	-		B_VDDOB2_R	-	
A9	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
C5	B_VDDOB3_R	-		B_VDDOB3_R	-	
A10	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
H5	VCC12	-		VCC12	-	
B10	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
E9	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
D9	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
J13	VCC12	-		VCC12	-	
H12	B_VDDIB3_R	-		B_VDDIB3_R	-	
J12	VCC12	-		VCC12	-	
M14	B_REFCLKN_R	-		B_REFCLKN_R	-	
L14	B_REFCLKP_R	-		B_REFCLKP_R	-	
J14	VCC12	-		VCC12	-	
G12	C_VDDIB0_R	-		C_VDDIB0_R	-	
D10	C_HDINP0_R	-	PCS 3E2 CH 0 IN P	C_HDINP0_R	-	PCS 3E2 CH 0 IN P
E10	C_HDINN0_R	-	PCS 3E2 CH 0 IN N	C_HDINN0_R	-	PCS 3E2 CH 0 IN N
H6	VCC12	-		VCC12	-	
B11	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P
M12	C_VDDOB0_R	-		C_VDDOB0_R	-	
A11	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N
L11	C_VDDOB1_R	-		C_VDDOB1_R	-	
A12	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N
K11	VCC12	-		VCC12	-	
B12	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P
E11	C_HDINN1_R	-	PCS 3E2 CH 1 IN N	C_HDINN1_R	-	PCS 3E2 CH 1 IN N
D11	C_HDINP1_R	-	PCS 3E2 CH 1 IN P	C_HDINP1_R	-	PCS 3E2 CH 1 IN P
H13	VCC12	-		VCC12	-	
C6	C_VDDIB1_R	-		C_VDDIB1_R	-	
H15	VCC12	-		VCC12	-	
G13	C_VDDIB2_R	-		C_VDDIB2_R	-	
D12	C_HDINP2_R	-	PCS 3E2 CH 2 IN P	C_HDINP2_R	-	PCS 3E2 CH 2 IN P
E12	C_HDINN2_R	-	PCS 3E2 CH 2 IN N	C_HDINN2_R	-	PCS 3E2 CH 2 IN N
J9	VCC12	-		VCC12	-	
B13	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P
K10	C_VDDOB2_R	-		C_VDDOB2_R	-	
A13	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N
J10	C_VDDOB3_R	-		C_VDDOB3_R	-	
A14	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-7FFN1020C ¹	-7	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-6FFN1020C ¹	-6	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-5FFN1020C ¹	-5	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-7FCN1152C ²	-7	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-6FCN1152C ²	-6	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-5FCN1152C ²	-5	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	40.4
LFSC3GA40E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	40.4
LFSC3GA40E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-7FFN1020C ¹	-7	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-6FFN1020C ¹	-6	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-5FFN1020C ¹	-5	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-7FFAN1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-6FFAN1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-5FFAN1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-7FCN1152C ²	-7	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FCN1152C ²	-6	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FCN1152C ²	-5	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-7FFN1152C	-7	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FFN1152C	-6	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FFN1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-6FFN1020I ¹	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-5FFN1020I ¹	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-6FCN1152I ²	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FCN1152I ²	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSC3GA80E-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).