Lattice Semiconductor Corporation - LFSC3GA115E-5FCN1704C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	942
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BCBGA, FCBGA
Supplier Device Package	1704-CFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga115e-5fcn1704c

Figure 2-1. Simplified Block Diagram (Top Level)

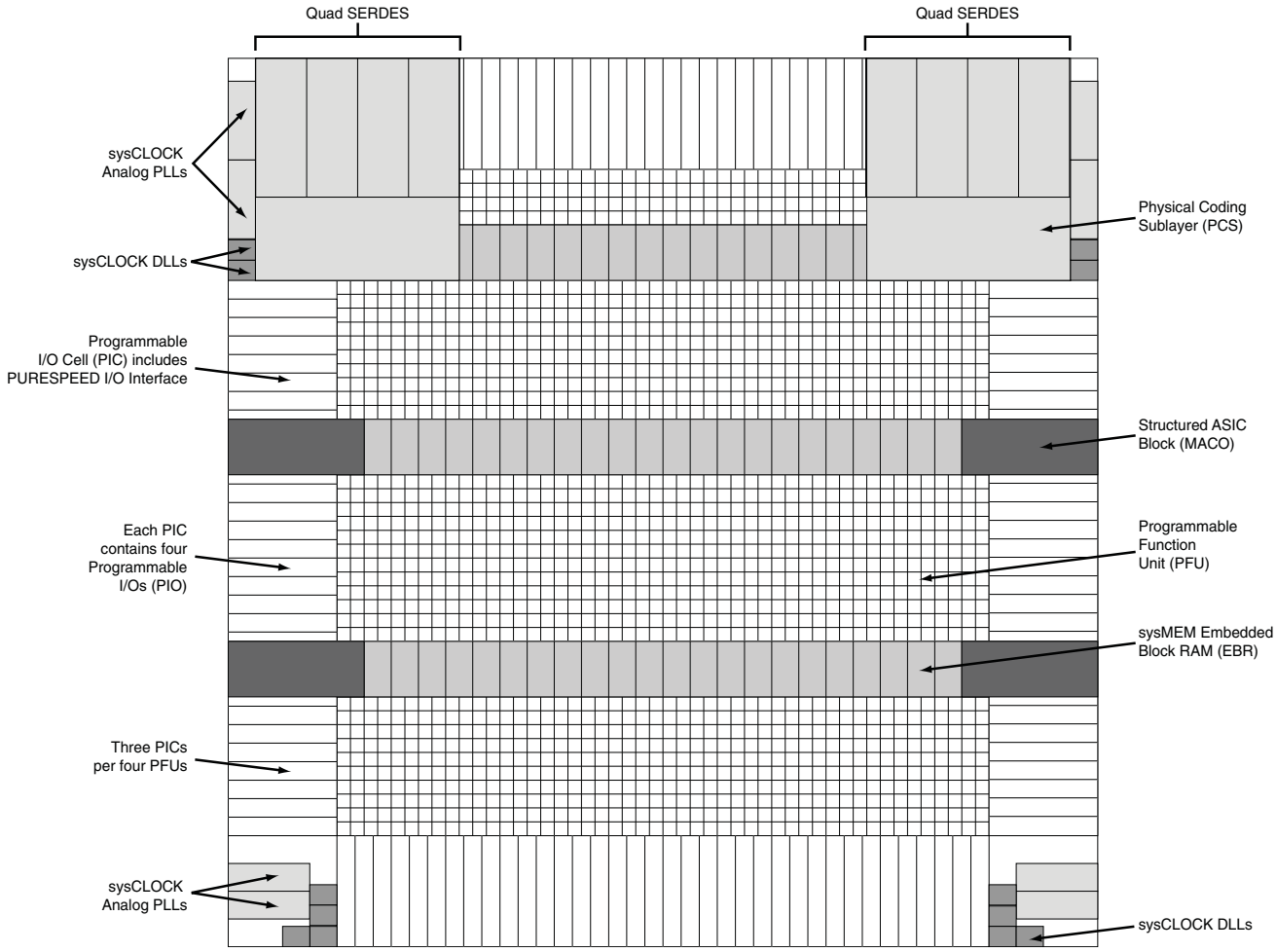
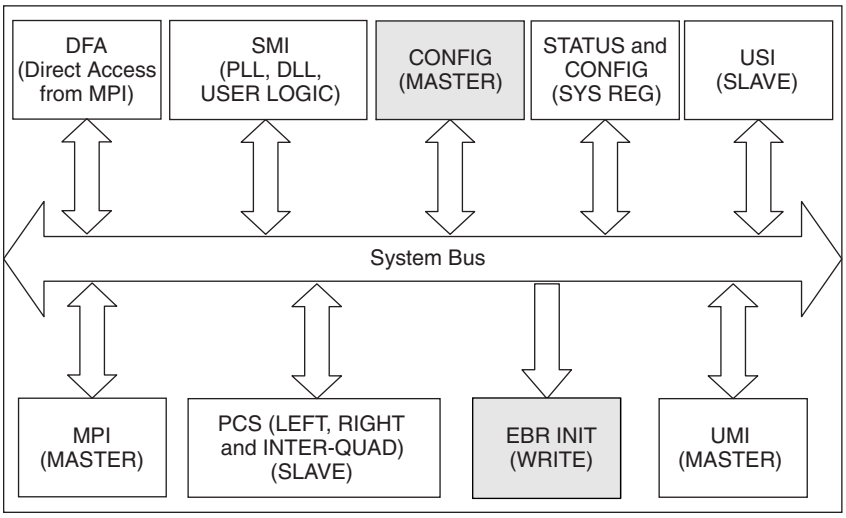


Figure 2-31. LatticeSC System Bus Interfaces



Several interfaces exist between the System Bus and other FPGA elements. The MPI interface acts as a bridge between the external microprocessor bus and System Bus. The MPI may work in an independent clock domain from the System Bus if the System Bus clock is not sourced from the external microprocessor clock. Pipelined operation allows high-speed memory interface to the EBR and peripheral access without the requirement for additional cycles on the bus. Burst transfers allow optimal use of the memory interface by giving advance information of the nature of the transfers.

Details for the majority of the peripherals can be found in the associated technical documentation, see details at the end of this data sheet. Additional details of the MPI are provided below.

Microprocessor Interface (MPI)

The LatticeSC family devices have a dedicated synchronous MPI function block. The MPI is programmable to operate with PowerPC/PowerQUICC MPC860/MPC8260 series microprocessors. The MPI implements an 8-, 16-, or 32-bit interface with 1-bit, 2-bit, or 4-bit parity to the host processor (PowerPC) that can be used for configuration and read-back of the FPGA as well as for user-defined data processing and general monitoring of FPGA functions.

The control portion of the MPI is available following power-up of the FPGA if the mode pins specify MPI mode, even if the FPGA is not yet configured. The width of the data port is selectable among 8-, 16-, or 32-bit and the parity bus can be 1-, 2-, or 4-bit. In configuration mode the data and parity bus width are related to the state of the M[0:3] mode pins. For post-configuration use, the MPI must be included in the configuration bit stream by using an MPI library element in your design from the ispLEVER primitive library, or by setting the bit of the MPI configuration control register prior to the start of configuration. The user can also enable and disable the parity bus through the configuration bit stream. These pads can be used as general I/O when they are not needed for MPI use.

The MPI block also provides the capability to interface directly to the FPGA fabric with a databus after configuration.The bus protocol is still handled by the MPI block but the direct FPGA access allows high-speed block data transfers such as DMA transactions. Figure 2-32 shows one of the ways a PowerPC is connected to MPI.

LatticeSC/M Family Timing Adders

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Input Adjusters								
LVDS	LVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
RSDS	RSDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
BLVDS25	BLVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
MLVDS25	MLVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
LVPECL33	LVPECL	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
HSTL18_I	HSTL_18 class I	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL18_II	HSTL_18 class II	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL18_III	HSTL_18 class III	-0.016	-0.018	0.008	0.003	0.032	0.023	ns
HSTL18_IV	HSTL_18 class IV	-0.016	-0.018	0.008	0.003	0.032	0.023	ns
HSTL18D_I	Differential HSTL 18 class I	0.006	0.001	0.029	0.024	0.052	0.046	ns
HSTL18D_II	Differential HSTL 18 class II	0.006	0.001	0.029	0.024	0.052	0.046	ns
HSTL15_I	HSTL_15 class I	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
HSTL15_II	HSTL_15 class II	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
HSTL15_III	HSTL_15 class III	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL15_IV	HSTL_15 class IV	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL15D_I	Differential HSTL 15 class I	-0.021	-0.022	0.001	-0.009	0.022	0.003	ns
HSTL15D_II	Differential HSTL 15 class II	-0.021	-0.022	0.001	-0.009	0.022	0.003	ns
SSTL33_I	SSTL_3 class I	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns
SSTL33_II	SSTL_3 class II	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns
SSTL33D_I	Differential SSTL_3 class I	0.012	0.012	0.034	0.028	0.055	0.043	ns
SSTL33D_II	Differential SSTL_3 class II	0.012	0.012	0.034	0.028	0.055	0.043	ns
SSTL25_I	SSTL_2 class I	0.003	-0.008	0.03	0.011	0.058	0.03	ns
SSTL25_II	SSTL_2 class II	0.003	-0.008	0.03	0.011	0.058	0.03	ns
SSTL25D_I	Differential SSTL_2 class I	0.006	0	0.031	0.023	0.056	0.046	ns
SSTL25D_II	Differential SSTL_2 class II	0.006	0	0.031	0.023	0.056	0.046	ns
SSTL18_I	SSTL_18 class I	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
SSTL18_II	SSTL_18 class II	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
SSTL18D_I	Differential SSTL_18 class I	0.006	0.001	0.029	0.024	0.052	0.046	ns
SSTL18D_II	Differential SSTL_18 class II	0.006	0.001	0.029	0.024	0.052	0.046	ns
LVTTL33	LVTTL	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
LVCMOS33	LVCMOS 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
LVCMOS25	LVCMOS 2.5	0	0	0	0	0	0	ns
LVCMOS18	LVCMOS 1.8	-0.068	-0.068	-0.087	-0.087	-0.105	-0.105	ns
LVCMOS15	LVCMOS 1.5	-0.131	-0.131	-0.186	-0.186	-0.241	-0.241	ns
LVCMOS12	LVCMOS 1.2	-0.238	-0.238	-0.364	-0.364	-0.49	-0.49	ns
PCI33	PCI	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
PCIX33	PCI-X 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
PCIX15	PCI-X 1.5	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
AGP1X33	AGP-1X 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
AGP2X33	AGP-2X	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns

LatticeSC/M sysCONFIG Port Timing (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Asynchronous Peripheral Configuration Mode				
t_{WRAP}	WRN, CS0N and CS1 Pulse Width	5	-	ns
t_{SAP}	D[7:0] Setup Time	1.5	-	ns
t_{RDYAP}	RDY Delay	—	8	ns
t_{BAP}	RDY Low	1	8	CCLK periods
t_{WR2AP}	Earliest WRN After RDY Goes High	0	—	ns
t_{DENAP}	RDN to D[7:0] Enable/Disable	—	7.5	ns
t_{DAP}	CCLK to DOUT	—	7.5	ns
sysCONFIG Slave Serial Configuration Mode				
t_{SSS}	DIN Setup Time	5.2	—	ns
t_{HSS}	DIN Hold Time	0	—	ns
t_{CHSS}	CCLK High Time	3.75	—	ns
t_{CLSS}	CCLK Low Time	3.75	—	ns
f_{CSS}	CCLK Frequency	—	150	MHz
t_{DSS}	CCLK to DOUT	—	7.5	ns
sysCONFIG Slave Parallel Configuration Mode				
t_{S1SP}	CS0N, CS1, WRN Setup Time	5.2	—	ns
t_{H1SP}	CS0N, CS1, WRN Hold Time	0	—	ns
t_{S2SP}	D[7:0] Setup Time	5.2	—	ns
t_{H2SP}	D[7:0] Hold Time	0	—	ns
t_{CHSP}	CCLK High Time	3.75	—	ns
t_{CL}	CCLK Low Time	3.75	—	ns
f_{CSP}	CCLK Frequency	—	150	MHz

sysCONFIG MPI Port

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{MPICTRL\_SET}$	MPI Control (MPCSTRBN, MPCWRN, MPCCLK, etc.) to MPCCLK Setup Time	4.9	—	5.2	—	5.5	—	ns
t_{MPIADR_SET}	MPI Address to MPCCLK Setup Time	3.9	—	4.2	—	4.5	—	ns
t_{MPIDAT_SET}	MPI Write Data to MPCCLK Setup Time	4.9	—	5.2	—	5.5	—	ns
$t_{MPIDPAR\_SET}$	MPI Write Parity Data to MPCCLK Setup Time	3.9	—	4.2	—	4.5	—	ns
t_{MPI_HLD}	All Hold Times	0	—	0	—	0	—	ns
$t_{MPICTRL\_DEL}$	MPCCLK to MPI Control (MPCTA, MPC-TEA, MPCRETRY)	—	5.6	—	6.7	—	8.7	ns
t_{MPIDAT_DEL}	MPCCLK to MPI Data	—	5.6	—	6.7	—	8.7	ns
$t_{MPIDPAR\_DEL}$	MPCCLK to MPI Parity Data	—	4.9	—	5.7	—	7.7	ns
$f_{MPI\_CLK\_FRQ}$	MPCCLK Frequency	—	100	—	83	—	66	MHz

Signal Descriptions (Cont.)

Signal Name	I/O	Description
RESETN		Reset. (Also sent to general routing). During configuration it resets the configuration state machine. After configuration this pin can perform the global set/reset (GSR) functions or can be used as a general input pin.
CFGIRQN	O	MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins.
TSALLN	I	Tristates all I/O.
Configuration Pads (User I/O if not used. Used during sysCONFIG.)		
HDC/SI	O	High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete. For SPI modes, this pin is used to download the read command and initial read address into the Flash memory device on the falling edge of SCK. This pin will be connected to SI of the memory. If the SPI mode is used, the 8-bit instruction code 0x03 will be downloaded followed by a 24-bit starting address of 0x000000 or a non-zero stat address for partial reconfiguration. If the SPIX mode has been selected, the 8-bit instruction captured on D[7:0] at power-up will be shifted in and followed by a 32-bit starting address of 0x000000.
LDCN/SCS	O	Low During Configuration is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete. For SPI modes, this is an active low chip select for Flash memories. It will go active after INITN goes high but before SCK begins. During power up LDCN will be low. Once INITN goes high, LDCN will go high for 100ns-200ns after which time it will go back low and configuration can begin. During the 100ns-200ns period, the read instruction will be latched for SPIX mode.
DOUT	O	Serial data output that can drive the D0/DIN of daisy-chained slave devices. The data-stream from this output will propagate preamble bits of the bitstream to daisy-chained devices. Data out on DOUT changes on the rising edge of CCLK.
QOUT/CEON	O	During daisy-chaining configuration, QOUT is the serial data output that can drive the D0/DIN of daisy-chained slave devices that do not propagate preamble bits. Data out on QOUT changes on the rising edge of CCLK. During parallel-chaining configuration, active low CEON enables the cascaded slave device to receive bitstream data.
RDN	I	Used in the asynchronous peripheral configuration mode. A low on RDN changes D[7:3] into status outputs. WRN and RDN should not be used simultaneously. If they are, the write strobe overrides.
WRN	I	When the FPGA is selected, a low on the write strobe, WRN, loads the data on D[7:0] inputs into an internal data buffer.
CS0N CS1	I	Used in the asynchronous peripheral, slave parallel and MPI modes. The FPGA is selected when CS0N is low and CS1 is high. During configuration, a pull-up is enabled on both except with MPI DMA access control.
A[21:0]	I/O	In master parallel mode, A[21:0] is an output and will address the configuration EPROMs up to 4 MB space. For MPI configuration mode, A[17:0] will be the MPI address MPI_ADDR[31:14], A[19:18] will be the transfer size and A[21:20] will be the burst mode and burst in process.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB10	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
J10	VCC	-		VCC	-	
J21	VCC	-		VCC	-	
K10	VCC	-		VCC	-	
K11	VCC	-		VCC	-	
K12	VCC	-		VCC	-	
K13	VCC	-		VCC	-	
K14	VCC	-		VCC	-	
K17	VCC	-		VCC	-	
K18	VCC	-		VCC	-	
K19	VCC	-		VCC	-	
K20	VCC	-		VCC	-	
K21	VCC	-		VCC	-	
K22	VCC	-		VCC	-	
K9	VCC	-		VCC	-	
L10	VCC	-		VCC	-	
L21	VCC	-		VCC	-	
M10	VCC	-		VCC	-	
M21	VCC	-		VCC	-	
N10	VCC	-		VCC	-	
N21	VCC	-		VCC	-	
P10	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
U10	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V10	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W10	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y10	VCC	-		VCC	-	
Y21	VCC	-		VCC	-	
H11	VCCAUX	-		VCCAUX	-	
H12	VCCAUX	-		VCCAUX	-	
H19	VCCAUX	-		VCCAUX	-	
H20	VCCAUX	-		VCCAUX	-	
M23	VCCAUX	-		VCCAUX	-	
M24	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
N24	VCCAUX	-		VCCAUX	-	
U23	VCCAUX	-		VCCAUX	-	
U24	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	
V24	VCCAUX	-		VCCAUX	-	
W23	VCCAUX	-		VCCAUX	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H1	PR25B	2		PR23B	2	
H2	PR25A	2		PR23A	2	
N8	PR22D	2		PR25D	2	
M8	PR22C	2		PR25C	2	
H4	PR22B	2		PR25B	2	
J4	PR22A	2		PR25A	2	
G1	PR21B	2		PR22B	2	
G2	PR21A	2		PR22A	2	
L7	PR20D	2		PR21D	2	
L8	PR20C	2		PR21C	2	
F2	PR20B	2		PR21B	2	
F1	PR20A	2		PR21A	2	
K5	PR18D	2	VREF2_2	PR18D	2	VREF2_2
J5	PR18C	2		PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
E1	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
N10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
M10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
D2	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
D1	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
K6	PR16D	2		PR16D	2	
K7	PR16C	2		PR16C	2	
J8	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
K8	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
J10	VCCJ	-		VCCJ	-	
J9	TDO	-	TDO	TDO	-	TDO
K9	TMS	-		TMS	-	
J12	TCK	-		TCK	-	
J13	TDI	-		TDI	-	
K12	PROGRAMN	1		PROGRAMN	1	
K13	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
K10	CCLK	1		CCLK	1	
F5	RESP_URC	-		RESP_URC	-	
B5	VCC12	-		VCC12	-	
D5	A_REFCLKN_R	-		A_REFCLKN_R	-	
C5	A_REFCLKP_R	-		A_REFCLKP_R	-	
B2	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
C2	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
A3	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
D3	A_VDDOB0_R	-		A_VDDOB0_R	-	
B3	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
D4	A_VDDOB1_R	-		A_VDDOB1_R	-	
B4	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
A4	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
H5	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
G5	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
F4	A_VDDIB1_R	-		A_VDDIB1_R	-	
H6	A_VDDIB2_R	-		A_VDDIB2_R	-	
F6	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
U12	VCC12	-		VCC12	-	
U21	VCC12	-		VCC12	-	
AA16	VCC12	-		VCC12	-	
AA17	VCC12	-		VCC12	-	
M14	VCC12	-		VCC12	-	
P12	VCC12	-		VCC12	-	
W12	VCC12	-		VCC12	-	
AA14	VCC12	-		VCC12	-	
AA19	VCC12	-		VCC12	-	
W21	VCC12	-		VCC12	-	
P21	VCC12	-		VCC12	-	
M19	VCC12	-		VCC12	-	
A2	GND	-		GND	-	
A10	GND	-		GND	-	
E28	NC	-		NC	-	
E5	NC	-		NC	-	
F10	NC	-		NC	-	
E10	NC	-		NC	-	
E23	NC	-		NC	-	
F23	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M25 and LatticeSC/M40 in a 1020-pin package support a 16-bit MPI interface.

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L33	PL27B	7		PL35B	7	
M30	PL27C	7		PL35C	7	
N30	PL27D	7		PL35D	7	
M31	PL29A	7		PL37A	7	
N31	PL29B	7		PL37B	7	
P24	PL29C	7		PL37C	7	
R24	PL29D	7		PL37D	7	
M33	PL30A	7		PL42A	7	
N33	PL30B	7		PL42B	7	
U25	PL30C	7		PL42C	7	
T25	PL30D	7		PL42D	7	
L34	PL31A	7		PL43A	7	
M34	PL31B	7		PL43B	7	
P29	PL31C	7		PL43C	7	
R29	PL31D	7		PL43D	7	
N34	PL34A	7		PL46A	7	
P34	PL34B	7		PL46B	7	
R27	PL34C	7		PL46C	7	
T27	PL34D	7		PL46D	7	
R32	PL35A	7	PCLKT7_1	PL47A	7	PCLKT7_1
R31	PL35B	7	PCLKC7_1	PL47B	7	PCLKC7_1
U24	PL35C	7	PCLKT7_3	PL47C	7	PCLKT7_3
T24	PL35D	7	PCLKC7_3	PL47D	7	PCLKC7_3
P33	PL36A	7	PCLKT7_0	PL48A	7	PCLKT7_0
R33	PL36B	7	PCLKC7_0	PL48B	7	PCLKC7_0
T26	PL36C	7	PCLKT7_2	PL48C	7	PCLKT7_2
U26	PL36D	7	PCLKC7_2	PL48D	7	PCLKC7_2
T32	PL38A	6	PCLKT6_0	PL50A	6	PCLKT6_0
T31	PL38B	6	PCLKC6_0	PL50B	6	PCLKC6_0
U29	PL38C	6	PCLKT6_1	PL50C	6	PCLKT6_1
V29	PL38D	6	PCLKC6_1	PL50D	6	PCLKC6_1
T30	PL39A	6		PL51A	6	
U30	PL39B	6		PL51B	6	
U27	PL39C	6	PCLKT6_3	PL51C	6	PCLKT6_3
V27	PL39D	6	PCLKC6_3	PL51D	6	PCLKC6_3
R34	PL40A	6		PL52A	6	
T34	PL40B	6		PL52B	6	
U28	PL40C	6	PCLKT6_2	PL52C	6	PCLKT6_2
V28	PL40D	6	PCLKC6_2	PL52D	6	PCLKC6_2
V30	PL43A	6		PL55A	6	
W30	PL43B	6		PL55B	6	
W27	PL43C	6	VREF1_6	PL55C	6	VREF1_6
Y27	PL43D	6		PL55D	6	
T33	PL44A	6		PL56A	6	
U33	PL44B	6		PL56B	6	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F15	PT55A	1	D5/MPI_DATA5	PT74A	1	D5/MPI_DATA5
K14	PT54D	1	D4/MPI_DATA4	PT73D	1	D4/MPI_DATA4
K13	PT54C	1	D3/MPI_DATA3	PT73C	1	D3/MPI_DATA3
B15	PT53B	1	D2/MPI_DATA2	PT73B	1	D2/MPI_DATA2
A15	PT53A	1	D1/MPI_DATA1	PT73A	1	D1/MPI_DATA1
J14	PT51D	1	D16/PCLKC1_3/MPI_DATA16	PT71D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT51C	1	D17/PCLKT1_3/MPI_DATA17	PT71C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT51B	1	D0/MPI_DATA0	PT71B	1	D0/MPI_DATA0
B16	PT51A	1	QOUT/CEON	PT71A	1	QOUT/CEON
J13	PT50D	1	VREF2_1	PT70D	1	VREF2_1
H13	PT50C	1	D18/MPI_DATA18	PT70C	1	D18/MPI_DATA18
D15	PT50B	1	DOUT	PT70B	1	DOUT
E15	PT50A	1	MCA_DONE_IN	PT70A	1	MCA_DONE_IN
J16	PT49D	1	D19/PCLKC1_2/MPI_DATA19	PT69D	1	D19/PCLKC1_2/MPI_DATA19
J17	PT49C	1	D20/PCLKT1_2/MPI_DATA20	PT69C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT49B	1	MCA_CLK_P1_OUT	PT69B	1	MCA_CLK_P1_OUT
E16	PT49A	1	MCA_CLK_P1_IN	PT69A	1	MCA_CLK_P1_IN
H15	PT47D	1	D21/PCLKC1_1/MPI_DATA21	PT67D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT47C	1	D22/PCLKT1_1/MPI_DATA22	PT67C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT47B	1	MCA_CLK_P2_OUT	PT67B	1	MCA_CLK_P2_OUT
C16	PT47A	1	MCA_CLK_P2_IN	PT67A	1	MCA_CLK_P2_IN
L17	PT46D	1	MCA_DONE_OUT	PT66D	1	MCA_DONE_OUT
K17	PT46C	1	BUSYN/RCLK/SCK	PT66C	1	BUSYN/RCLK/SCK
E17	PT46B	1	DP0/MPI_PAR0	PT66B	1	DP0/MPI_PAR0
F17	PT46A	1	MPI_TA	PT66A	1	MPI_TA
G17	PT45D	1	D23/MPI_DATA23	PT65D	1	D23/MPI_DATA23
H17	PT45C	1	DP2/MPI_PAR2	PT65C	1	DP2/MPI_PAR2
A17	PT45B	1	PCLKC1_0	PT65B	1	PCLKC1_0
B17	PT45A	1	PCLKT1_0/MPI_CLK	PT65A	1	PCLKT1_0/MPI_CLK
G18	PT43D	1	DP3/PCLKC1_4/MPI_PAR3	PT63D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT43C	1	D24/PCLKT1_4/MPI_DATA24	PT63C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT43B	1	MPI_RETRY	PT63B	1	MPI_RETRY
F18	PT43A	1	A0/MPI_ADDR14	PT63A	1	A0/MPI_ADDR14
J18	PT42D	1	A1/MPI_ADDR15	PT61D	1	A1/MPI_ADDR15
J19	PT42C	1	A2/MPI_ADDR16	PT61C	1	A2/MPI_ADDR16
C20	PT42B	1	A3/MPI_ADDR17	PT61B	1	A3/MPI_ADDR17
C19	PT42A	1	A4/MPI_ADDR18	PT61A	1	A4/MPI_ADDR18
K18	PT41D	1	D25/PCLKC1_5/MPI_DATA25	PT60D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT41C	1	D26/PCLKT1_5/MPI_DATA26	PT60C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT41B	1	A5/MPI_ADDR19	PT60B	1	A5/MPI_ADDR19
E19	PT41A	1	A6/MPI_ADDR20	PT60A	1	A6/MPI_ADDR20
H19	PT39D	1	D27/MPI_DATA27	PT59D	1	D27/MPI_DATA27
H20	PT39C	1	VREF1_1	PT59C	1	VREF1_1
A18	PT39B	1	A7/MPI_ADDR21	PT59B	1	A7/MPI_ADDR21
B18	PT39A	1	A8/MPI_ADDR22	PT59A	1	A8/MPI_ADDR22

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
F6	A_VDDOB0_R	-	
B4	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
F7	A_VDDOB1_R	-	
B5	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
E6	VCC12	-	
A5	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
B6	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
A6	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
C6	VCC12	-	
D4	A_VDDIB1_R	-	
C7	VCC12	-	
D5	A_VDDIB2_R	-	
A7	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
B7	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
E7	VCC12	-	
A8	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
F8	A_VDDOB2_R	-	
B8	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
F9	A_VDDOB3_R	-	
B9	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
E8	VCC12	-	
A9	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
B10	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
A10	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
C10	VCC12	-	
D6	A_VDDIB3_R	-	
G10	VCC12	-	
D7	B_VDDIB0_R	-	
E10	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
F10	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
K10	VCC12	-	
A11	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D10	B_VDDOB0_R	-	
B11	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D11	B_VDDOB1_R	-	
B12	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L10	VCC12	-	
A12	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
F11	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
E11	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
G11	VCC12	-	
D8	B_VDDIB1_R	-	
G12	VCC12	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
U22	VCCAUX	-	
V13	VCCAUX	-	
V22	VCCAUX	-	
V23	VCCAUX	-	
W13	VCCAUX	-	
W22	VCCAUX	-	
Y21	GND	-	
Y25	GND	-	
C18	VCCIO1	-	
D17	VCCIO1	-	
F16	VCCIO1	-	
G19	VCCIO1	-	
J20	VCCIO1	-	
K12	VCCIO1	-	
K15	VCCIO1	-	
L23	VCCIO1	-	
Y9	GND	-	
J9	VCCIO1	-	
E3	VCCIO2	-	
G6	VCCIO2	-	
H4	VCCIO2	-	
K7	VCCIO2	-	
L3	VCCIO2	-	
M11	VCCIO2	-	
N6	VCCIO2	-	
P4	VCCIO2	-	
R9	VCCIO2	-	
AA3	VCCIO3	-	
AB7	VCCIO3	-	
AC10	VCCIO3	-	
AD4	VCCIO3	-	
AE6	VCCIO3	-	
AG3	VCCIO3	-	
AK4	VCCIO3	-	
T7	VCCIO3	-	
U3	VCCIO3	-	
V4	VCCIO3	-	
W6	VCCIO3	-	
Y10	VCCIO3	-	
AD12	VCCIO4	-	
AF15	VCCIO4	-	
AF9	VCCIO4	-	
AH10	VCCIO4	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AY41	PB12A	5		PB13A	5	
BA41	PB12B	5		PB13B	5	
AT39	PB12C	5		PB13C	5	
AT38	PB12D	5		PB13D	5	
AV37	PB13A	5		PB15A	5	
AV36	PB13B	5		PB15B	5	
AM31	PB13C	5		PB15C	5	
AM32	PB13D	5		PB15D	5	
BA40	PB15A	5		PB16A	5	
BB40	PB15B	5		PB16B	5	
AM29	PB15C	5		PB16C	5	
AL29	PB15D	5		PB16D	5	
AY39	PB16A	5		PB17A	5	
AY38	PB16B	5		PB17B	5	
AN33	PB16C	5		PB17C	5	
AN32	PB16D	5		PB17D	5	
BA39	PB17A	5		PB19A	5	
BA38	PB17B	5		PB19B	5	
AT37	PB17C	5		PB19C	5	
AT36	PB17D	5		PB19D	5	
AW36	PB19A	5		PB20A	5	
AW35	PB19B	5		PB20B	5	
AM28	PB19C	5		PB20C	5	
AL28	PB19D	5		PB20D	5	
BB38	PB20A	5		PB21A	5	
BB39	PB20B	5		PB21B	5	
AR34	PB20C	5		PB21C	5	
AR33	PB20D	5		PB21D	5	
AV35	PB21A	5		PB23A	5	
AV34	PB21B	5		PB23B	5	
AT33	PB21C	5		PB23C	5	
AT34	PB21D	5		PB23D	5	
BA37	PB23A	5		PB25A	5	
BA36	PB23B	5		PB25B	5	
AP33	PB23C	5		PB25C	5	
AP32	PB23D	5		PB25D	5	
AY36	PB24A	5		PB26A	5	
AY35	PB24B	5		PB26B	5	
AN31	PB24C	5		PB26C	5	
AN30	PB24D	5		PB26D	5	
BB37	PB25A	5		PB27A	5	
BB36	PB25B	5		PB27B	5	
AP31	PB25C	5		PB27C	5	
AP30	PB25D	5		PB27D	5	
AV33	PB27A	5		PB29A	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP26	PB41C	5		PB43C	5	
AN26	PB41D	5		PB43D	5	
AY30	PB43A	5		PB45A	5	
AY29	PB43B	5		PB45B	5	
AU30	PB43C	5		PB45C	5	
AU31	PB43D	5		PB45D	5	
AV27	PB44A	5		PB46A	5	
AV26	PB44B	5		PB46B	5	
AT28	PB44C	5		PB46C	5	
AT27	PB44D	5		PB46D	5	
BA29	PB45A	5		PB47A	5	
BA28	PB45B	5		PB47B	5	
AL25	PB45C	5		PB47C	5	
AM25	PB45D	5		PB47D	5	
BB29	PB47A	5		PB49A	5	
BB28	PB47B	5		PB49B	5	
AN25	PB47C	5		PB49C	5	
AP25	PB47D	5		PB49D	5	
AY27	PB48A	5	PCLKT5_3	PB50A	5	PCLKT5_3
AY26	PB48B	5	PCLKC5_3	PB50B	5	PCLKC5_3
AT25	PB48C	5	PCLKT5_4	PB50C	5	PCLKT5_4
AT24	PB48D	5	PCLKC5_4	PB50D	5	PCLKC5_4
AW27	PB49A	5	PCLKT5_5	PB51A	5	PCLKT5_5
AW26	PB49B	5	PCLKC5_5	PB51B	5	PCLKC5_5
AU29	PB49C	5		PB51C	5	
AU28	PB49D	5		PB51D	5	
BB27	PB51A	5	PCLKT5_0	PB53A	5	PCLKT5_0
BB26	PB51B	5	PCLKC5_0	PB53B	5	PCLKC5_0
AR25	PB51C	5		PB53C	5	
AR24	PB51D	5	VREF2_5	PB53D	5	VREF2_5
BA27	PB52A	5	PCLKT5_1	PB54A	5	PCLKT5_1
BA26	PB52B	5	PCLKC5_1	PB54B	5	PCLKC5_1
AP24	PB52C	5	PCLKT5_6	PB54C	5	PCLKT5_6
AN24	PB52D	5	PCLKC5_6	PB54D	5	PCLKC5_6
AV25	PB53A	5	PCLKT5_2	PB55A	5	PCLKT5_2
AV24	PB53B	5	PCLKC5_2	PB55B	5	PCLKC5_2
AU27	PB53C	5	PCLKT5_7	PB55C	5	PCLKT5_7
AU26	PB53D	5	PCLKC5_7	PB55D	5	PCLKC5_7
BA25	PB55A	5		PB57A	5	
BA24	PB55B	5		PB57B	5	
AU24	PB55C	5		PB57C	5	
AU25	PB55D	5		PB57D	5	
BB24	PB56A	5		PB58A	5	
BB25	PB56B	5		PB58B	5	
AM23	PB56C	5		PB58C	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BA19	PB73A	4		PB87A	4	
BA18	PB73B	4		PB87B	4	
AU19	PB73C	4		PB87C	4	
AU18	PB73D	4		PB87D	4	
AV19	PB74A	4	PCLKT4_2	PB89A	4	PCLKT4_2
AV18	PB74B	4	PCLKC4_2	PB89B	4	PCLKC4_2
AN19	PB74C	4	PCLKT4_7	PB89C	4	PCLKT4_7
AP19	PB74D	4	PCLKC4_7	PB89D	4	PCLKC4_7
BB17	PB75A	4	PCLKT4_1	PB90A	4	PCLKT4_1
BB16	PB75B	4	PCLKC4_1	PB90B	4	PCLKC4_1
AT19	PB75C	4	PCLKT4_6	PB90C	4	PCLKT4_6
AT18	PB75D	4	PCLKC4_6	PB90D	4	PCLKC4_6
BA17	PB77A	4	PCLKT4_0	PB91A	4	PCLKT4_0
BA16	PB77B	4	PCLKC4_0	PB91B	4	PCLKC4_0
AR19	PB77C	4	VREF2_4	PB91C	4	VREF2_4
AR18	PB77D	4		PB91D	4	
AY17	PB79A	4	PCLKT4_5	PB93A	4	PCLKT4_5
AY16	PB79B	4	PCLKC4_5	PB93B	4	PCLKC4_5
AN18	PB79C	4		PB93C	4	
AP18	PB79D	4		PB93D	4	
AW17	PB80A	4	PCLKT4_3	PB94A	4	PCLKT4_3
AW16	PB80B	4	PCLKC4_3	PB94B	4	PCLKC4_3
AU17	PB80C	4	PCLKT4_4	PB94C	4	PCLKT4_4
AU16	PB80D	4	PCLKC4_4	PB94D	4	PCLKC4_4
AV17	PB81A	4		PB95A	4	
AV16	PB81B	4		PB95B	4	
AL18	PB81C	4		PB95C	4	
AM18	PB81D	4		PB95D	4	
BB15	PB83A	4		PB97A	4	
BB14	PB83B	4		PB97B	4	
AP17	PB83C	4		PB97C	4	
AN17	PB83D	4		PB97D	4	
BA15	PB84A	4		PB98A	4	
BA14	PB84B	4		PB98B	4	
AT16	PB84C	4		PB98C	4	
AT15	PB84D	4		PB98D	4	
AV15	PB85A	4		PB99A	4	
AV14	PB85B	4		PB99B	4	
AR16	PB85C	4		PB99C	4	
AR15	PB85D	4		PB99D	4	
AY14	PB87A	4		PB101A	4	
AY13	PB87B	4		PB101B	4	
AU15	PB87C	4		PB101C	4	
AU14	PB87D	4		PB101D	4	
BB13	PB88A	4		PB102A	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AU9	PB103C	4		PB117C	4	
AU8	PB103D	4		PB117D	4	
AY8	PB104A	4		PB118A	4	
AY7	PB104B	4		PB118B	4	
AU7	PB104C	4		PB118C	4	
AU6	PB104D	4		PB118D	4	
BA7	PB105A	4		PB119A	4	
BA6	PB105B	4		PB119B	4	
AN13	PB105C	4		PB119C	4	
AN12	PB105D	4		PB119D	4	
AV9	PB107A	4		PB121A	4	
AV8	PB107B	4		PB121B	4	
AT10	PB107C	4		PB121C	4	
AT9	PB107D	4		PB121D	4	
AW8	PB108A	4		PB122A	4	
AW7	PB108B	4		PB122B	4	
AP11	PB108C	4		PB122C	4	
AP10	PB108D	4		PB122D	4	
BB5	PB109A	4		PB123A	4	
BB4	PB109B	4		PB123B	4	
AR10	PB109C	4		PB123C	4	
AR9	PB109D	4		PB123D	4	
BA5	PB111A	4		PB125A	4	
BA4	PB111B	4		PB125B	4	
AT7	PB111C	4		PB125C	4	
AT6	PB111D	4		PB125D	4	
BB3	PB112A	4		PB126A	4	
BA3	PB112B	4		PB126B	4	
AM14	PB112C	4		PB126C	4	
AL14	PB112D	4		PB126D	4	
AY5	PB113A	4		PB127A	4	
AY4	PB113B	4		PB127B	4	
AN11	PB113C	4		PB127C	4	
AN10	PB113D	4		PB127D	4	
AV7	PB115A	4		PB129A	4	
AV6	PB115B	4		PB129B	4	
AM12	PB115C	4		PB129C	4	
AM11	PB115D	4		PB129D	4	
AW5	PB116A	4		PB130A	4	
AW4	PB116B	4		PB130B	4	
AT5	PB116C	4		PB130C	4	
AT4	PB116D	4		PB130D	4	
AY2	PB117A	4		PB131A	4	
BA2	PB117B	4		PB131B	4	
AP9	PB117C	4		PB131C	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L8	VCCIO2	-		VCCIO2	-	
M3	VCCIO2	-		VCCIO2	-	
P7	VCCIO2	-		VCCIO2	-	
R4	VCCIO2	-		VCCIO2	-	
T12	VCCIO2	-		VCCIO2	-	
U8	VCCIO2	-		VCCIO2	-	
V3	VCCIO2	-		VCCIO2	-	
W11	VCCIO2	-		VCCIO2	-	
Y7	VCCIO2	-		VCCIO2	-	
AB3	VCCIO3	-		VCCIO3	-	
AC7	VCCIO3	-		VCCIO3	-	
AD11	VCCIO3	-		VCCIO3	-	
AE4	VCCIO3	-		VCCIO3	-	
AF8	VCCIO3	-		VCCIO3	-	
AG12	VCCIO3	-		VCCIO3	-	
AH3	VCCIO3	-		VCCIO3	-	
AJ7	VCCIO3	-		VCCIO3	-	
AK11	VCCIO3	-		VCCIO3	-	
AL4	VCCIO3	-		VCCIO3	-	
AM8	VCCIO3	-		VCCIO3	-	
AP3	VCCIO3	-		VCCIO3	-	
AR7	VCCIO3	-		VCCIO3	-	
AU4	VCCIO3	-		VCCIO3	-	
AL16	VCCIO4	-		VCCIO4	-	
AM13	VCCIO4	-		VCCIO4	-	
AM19	VCCIO4	-		VCCIO4	-	
AR11	VCCIO4	-		VCCIO4	-	
AR17	VCCIO4	-		VCCIO4	-	
AT14	VCCIO4	-		VCCIO4	-	
AT20	VCCIO4	-		VCCIO4	-	
AT8	VCCIO4	-		VCCIO4	-	
AW15	VCCIO4	-		VCCIO4	-	
AW21	VCCIO4	-		VCCIO4	-	
AW9	VCCIO4	-		VCCIO4	-	
AY12	VCCIO4	-		VCCIO4	-	
AY18	VCCIO4	-		VCCIO4	-	
AY6	VCCIO4	-		VCCIO4	-	
AL27	VCCIO5	-		VCCIO5	-	
AM24	VCCIO5	-		VCCIO5	-	
AM30	VCCIO5	-		VCCIO5	-	
AR26	VCCIO5	-		VCCIO5	-	
AR32	VCCIO5	-		VCCIO5	-	
AT23	VCCIO5	-		VCCIO5	-	
AT29	VCCIO5	-		VCCIO5	-	
AT35	VCCIO5	-		VCCIO5	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AW25	VCCIO5	-		VCCIO5	-	
AW31	VCCIO5	-		VCCIO5	-	
AW37	VCCIO5	-		VCCIO5	-	
AY22	VCCIO5	-		VCCIO5	-	
AY28	VCCIO5	-		VCCIO5	-	
AY34	VCCIO5	-		VCCIO5	-	
AB39	VCCIO6	-		VCCIO6	-	
AC36	VCCIO6	-		VCCIO6	-	
AD32	VCCIO6	-		VCCIO6	-	
AE40	VCCIO6	-		VCCIO6	-	
AF35	VCCIO6	-		VCCIO6	-	
AG31	VCCIO6	-		VCCIO6	-	
AH39	VCCIO6	-		VCCIO6	-	
AJ36	VCCIO6	-		VCCIO6	-	
AK32	VCCIO6	-		VCCIO6	-	
AL40	VCCIO6	-		VCCIO6	-	
AM35	VCCIO6	-		VCCIO6	-	
AP39	VCCIO6	-		VCCIO6	-	
AR36	VCCIO6	-		VCCIO6	-	
AU40	VCCIO6	-		VCCIO6	-	
AA40	VCCIO7	-		VCCIO7	-	
H36	VCCIO7	-		VCCIO7	-	
J40	VCCIO7	-		VCCIO7	-	
L35	VCCIO7	-		VCCIO7	-	
M39	VCCIO7	-		VCCIO7	-	
P36	VCCIO7	-		VCCIO7	-	
R40	VCCIO7	-		VCCIO7	-	
T31	VCCIO7	-		VCCIO7	-	
U35	VCCIO7	-		VCCIO7	-	
V39	VCCIO7	-		VCCIO7	-	
W32	VCCIO7	-		VCCIO7	-	
Y36	VCCIO7	-		VCCIO7	-	
AA14	VTT_2	2		VTT_2	2	
AA15	VTT_2	2		VTT_2	2	
R12	VTT_2	2		VTT_2	2	
V14	VTT_2	2		VTT_2	2	
AB14	VTT_3	3		VTT_3	3	
AB15	VTT_3	3		VTT_3	3	
AE14	VTT_3	3		VTT_3	3	
AJ13	VTT_3	3		VTT_3	3	
AH21	VTT_4	4		VTT_4	4	
AJ18	VTT_4	4		VTT_4	4	
AJ19	VTT_4	4		VTT_4	4	
AJ20	VTT_4	4		VTT_4	4	
AJ21	VTT_4	4		VTT_4	4	

Lead-Free Packaging

Commercial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Date	Version	Section	Change Summary
December 2011	02.4	DC and Switching Characteristics	Updated JTAG Port Timing Specifications table.