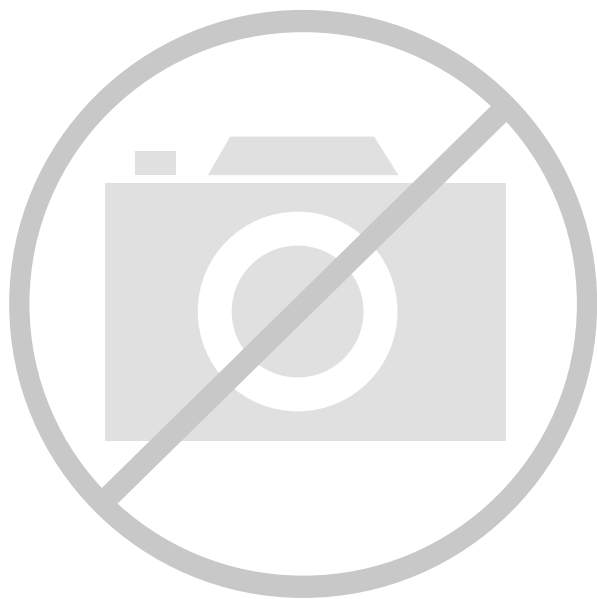




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga115e-5ffn1152c

Table 1-1. LatticeSC Family Selection Guide¹

Device	SC15	SC25	SC40	SC80	SC115
LUT4s (K)	15	25	40	80	115
sysMEM Blocks (18Kb)	56	104	216	308	424
Embedded Memory (Mbits)	1.03	1.92	3.98	5.68	7.8
Max. Distributed Memory (Mbits)	0.24	0.41	0.65	1.28	1.84
Number of 3.8Gbps SERDES (Max.)	8	16	16	32	32
DLLs	12	12	12	12	12
Analog PLLs	8	8	8	8	8
MACO Blocks	4	6	10	10	12
Package I/O/SERDES Combinations (1mm ball pitch)					
256-ball fpBGA (17 x 17mm)	139/4				
900-ball fpBGA (31 x 31mm)	300/8	378/8			
1020-ball fcBGA (33 x 33mm) ²		476/16	562/16		
1152-ball fcBGA (35 x 35mm) ³			604/16	660/16	660/16
1704-ball fcBGA (42.5 x 42.5mm) ³				904/32	942/32

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per [PCN #02A-10](#).
3. Ceramic fcBGA converted to organic fcBGA per [PCN #01A-10](#).

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

Table 1-2. LatticeSCM Family

Device	SCM15	SCM25	SCM40	SCM80	SCM115
flexiMAC Blocks • 1GbE Mode • 10GbE Mode • PCI Express Mode	1	2	2	2	4
SPI4.2 Blocks	1	2	2	2	2
Memory Controller Blocks • DDR/DDR2 DRAM Mode • QDR II/II+ SRAM Mode • RLDRAM I • RLDRAM II CIO/SIO	1	2	2	2	2
Low-Speed CDR Blocks	0	0	2	2	2
PCI Express LTSSM (PHY) Blocks	1	0	2	2	2

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

Table 2-10. Supported Output Standards⁴

Output Standard	Drive	V _{CCIO} (Nom)	On-chip Output Termination
Single-ended Interfaces			
LVTTL/D ¹	8mA, 16mA, 24mA	3.3	None.
LVC MOS33/D ¹	8mA, 16mA, 24mA	3.3	None
LVC MOS25/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	2.5	None, series: 25, 33, 50, 100
LVC MOS18/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	1.8	None, series: 25, 33, 50, 100
LVC MOS15/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	1.5	None, series: 25, 33, 50, 100
LVC MOS12/D ^{1,2}	2mA, 4mA, 8mA, 12mA	1.2	None, series: 25, 33, 50, 100
PCIX15	N/A	1.5	None
PCI33, PCIX33, AGP1X33, AGP2X33	N/A	3.3	None
HSTL18_I	N/A	1.8	None, series: 50
HSTL18_II	N/A	1.8	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
HSTL15_I	N/A	1.5	None, series: 50
HSTL15_II	N/A	1.5	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
SSTL33_I	N/A	3.3	None
SSTL33_II	N/A	3.3	None
SSTL25_I	N/A	2.5	None, series: 50
SSTL25_II	N/A	2.5	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
SSTL18_I	N/A	1.8	None, series: 33
SSTL18_II	N/A	1.8	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
Differential Interfaces			
SSTL18D_I	N/A	1.8	None, series: 33
SSTL25D_I	N/A	2.5	None, series: 50
SSTL18D_II, SSTL25D_II	N/A	1.2/2.5/3.3	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
SSTL33D_I, II	N/A	3.3	None
HSTL15D_I, HSTL18D_I	N/A	1.5/1.8	None, series: 50
HST15D_II, HSTL18D_II	N/A	1.5/1.8	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
LVDS	2mA, 3.5mA, 4mA, 6mA	N/A	None
Mini-LVDS	3.5mA, 4mA, 6mA	N/A	None
BLVDS25	N/A	N/A	None
MLVDS25	N/A	N/A	None
LVPECL33 ³	N/A	3.3	None
RSDS	2mA, 3.5mA, 4mA, 6mA	N/A	None

1. D refers to open drain capability.

2. User can select either drive current or driver impedances but not both.

3. Emulated with external resistors.

4. No GTL or GTL+ support.

PCI Clamp

A programmable PCI clamp is available on the top and bottom banks of the device. The PCI clamp can be turned “ON” or “OFF” on each pin independently. The PCI clamp is used when implementing a 3.3V PCI interface. The

Internal Logic Analyzer Capability (ispTRACY)

All LatticeSC devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time. For additional detail refer to technical information at the end of the data sheet.

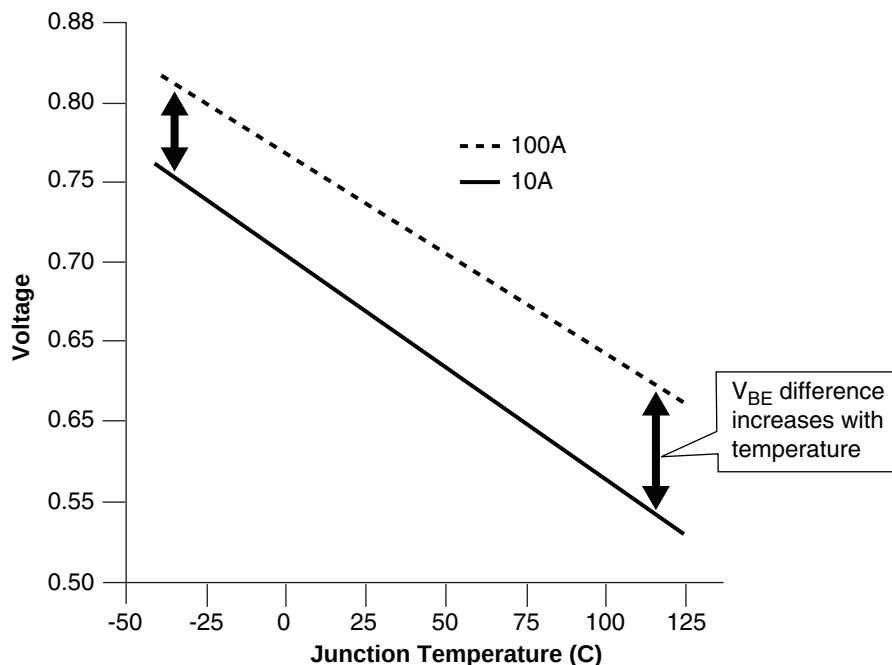
Temperature Sensing

Lattice provides a way to monitor the die temperature by using a temperature-sensing diode that is designed into every LatticeSC device. The difference in V_{BE} of the diode at two different forward currents varies with temperature. This relationship is shown in Figure 2-33. The accuracy of the temperature-sensing diode is typically $\pm 10^{\circ}\text{C}$.

On packages that include PROBE_GND, the most accurate measurements will occur between the TEMP pin and the PROBE_GND pin. On packages that do not include PROBE_GND, measurements should be made between the TEMP pin and board ground.

This temperature-sensing diode is designed to work with an external temperature sensor such as the Maxim 1617A. The Maxim 1617A is configured to measure difference in V_{BE} (of the temperature-sensing diode) at $10\mu\text{A}$ and at $100\mu\text{A}$. This difference in V_{BE} voltage varies with temperature at approximately $1.64\text{ mV}/^{\circ}\text{C}$. A typical device with a 85°C junction temperature will measure approximately 593mV . For additional detail refer to TN1115, [Temperature Sensing Diode in LatticeSC Devices](#).

Figure 2-33. Sensing Diode Typical Characteristics



Oscillator

Every LatticeSC device has an internal CMOS oscillator, which is used as a master serial clock for configuration and is also available as a potential general purpose clock (MCK) for the FPGA core. There is a K divider (divide by 2/4/8/16/32/64/128) available with this oscillator to get lower MCK frequencies. This clock is available as a general purpose clock signal to the software routing tool. For additional detail refer to technical information at the end of the data sheet.

LatticeSC/M Internal Timing Parameters¹

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Symbol	Description	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
PFU Logic Mode Timing									
t _{LUT4_PFU}	CTOF_DEL	LUT4 delay (A to D inputs to F output)	—	0.045	—	0.050	—	0.054	ns
t _{LUT5_PFU}	MTOOFX_DEL	LUT5 delay (inputs to output)	—	0.152	—	0.172	—	0.192	ns
t _{LSR_PFU}	LSR_DEL	Set/Reset to output (asynchronous)	—	0.378	—	0.426	—	0.474	ns
t _{SUM_PFU}	M_SET	Clock to Mux (M0,M1) input setup time	0.113	—	0.131	—	0.148	—	ns
t _{HM_PFU}	M_HLD	Clock to Mux (M0,M1) input hold time	-0.041	—	-0.046	—	-0.052	—	ns
t _{SUD_PFU}	DIN_SET	Clock to D input setup time	0.072	—	0.083	—	0.094	—	ns
t _{HD_PFU}	DIN_HLD	Clock to D input hold time	-0.028	—	-0.032	—	-0.035	—	ns
t _{CK2Q_PFU}	REG_DEL	Clock to Q delay, D-type register configuration	—	0.224	—	0.252	—	0.279	ns
t _{LE2Q_PFU}	LTCH_DEL	Clock to Q delay latch configuration	—	0.294	—	0.331	—	0.367	ns
t _{LD2Q_PFU}	TLTCH_DEL	D to Q throughput delay when latch is enabled	—	0.300	—	0.338	—	0.376	ns
PFU Memory Mode Timing									
t _{CORAM_PFU}	CLKTOF_DEL	Clock to Output	—	0.575	—	0.649	—	0.724	ns
t _{SUDATA_PFU}	DIN_SET	Data Setup Time	-0.024	—	-0.026	—	-0.027	—	ns
t _{HDATA_PFU}	DIN_HLD	Data Hold Time	0.075	—	0.084	—	0.094	—	ns
t _{SUADDR_PFU}	WAD_SET	Address Setup Time	-0.176	—	-0.196	—	-0.215	—	ns
t _{HADDR_PFU}	WAD_HLD	Address Hold Time	0.110	—	0.124	—	0.138	—	ns
t _{SUWREN_PFU}	WE_SET	Write/Read Enable Setup Time	0.014	—	0.019	—	0.024	—	ns
t _{HWREN_PFU}	WE_HLD	Write/Read Enable Hold Time	0.078	—	0.086	—	0.094	—	ns
PIC Timing									
PIO Input/Output Buffer Timing									
t _{IN_PIO}	IN_DEL	Input Buffer Delay(LVCMOS25)	—	0.578	—	0.661	—	0.744	ns
t _{OUT_PIO}	DOPADI_DEL	Output Buffer Delay(LVCMOS25)	—	2.712	—	3.027	—	3.395	ns
t _{SUI_PIO}	DIN_SET	Input Register Setup Time (Data Before Clock)	0.277	—	0.312	—	0.348	—	ns
t _{HI_PIO}	DIN_HLD	Input Register Hold Time (Data after Clock)	-0.267	—	-0.306	—	-0.345	—	ns
t _{COO_PIO}	CK_DEL	Output Register Clock to Output Delay	—	0.513	—	0.571	—	0.639	ns
t _{SUCE_PIO}	CE_SET	Input Register Clock Enable Setup Time	—	0.000	—	0.000	—	0.000	ns
t _{HCE_PIO}	CE_HLD	Input Register Clock Enable Hold Time	—	0.129	—	0.145	—	0.161	ns
t _{SULSR_PIO}	LSR_SET	Set/Reset Setup Time	0.057	—	0.060	—	0.063	—	ns
t _{HLSR_PIO}	LSR_HLD	Set/Reset Hold Time	-0.151	—	-0.159	—	-0.169	—	ns
t _{LE2Q_PIO}	CK_DEL	Input Register Clock to Q delay latch configuration	—	0.335	—	0.372	—	0.410	ns
t _{LD2Q_PIO}	DIN_DEL	Input Register D to Q throughput delay when latch is enabled	—	0.578	—	0.647	—	0.717	ns

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PIC row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
VREF1_x, VREF2_x	—	The reference supply pins for I/O bank x. Any I/O pin in a bank can be assigned as a reference supply pin, but software defaults use designated pin.
NC	—	No connect. NC pins should not be connected to any active signals, VCC or GND.
Non-SERDES Power Supplies		
VCCIOx	—	VCCIO - The power supply pins for I/O bank x. Dedicated pins.
VCC12 ¹	—	1.2V supply for configuration logic, PLLs and SERDES Rx, Tx and PLL. All VCC12 pins must be connected. As VCC12 supplies power for analog circuitry, VCC12 should be quiet and isolated from noisy digital board supplies.
VTT_x	—	Termination voltage for bank x. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.
GND	—	GND - Ground. Dedicated pins. All grounds must be electrically connected at the board level.
VCC	—	VCC - The power supply pins for core logic. Dedicated pins (1.2V/1.0V).
VCCAUX	—	VCCAUX - Auxiliary power supply pin - powers all differential and referenced input buffers. Dedicated pins (2.5V).
VCCJ	—	VCCJ - The power supply pin for JTAG Test Access Port.
PROBE_VCC	—	VCC signal - Connected to internal VCC node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
MPI_STRBN	I	Driven active low indicates the start of a transaction on the PowerPC bus. MPI will strobe the address bus at next rising edge of clock.
MPI_ADDR[31:14]	I	Address bus driven by a PowerPC bus master. Only 18-bit width is needed. It has to be the least significant bit of the PowerPC 32-bit address A[31:14].
MPI_DAT[n:0]	I/O	Selectable data bus width from 8, and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
MPI_PAR[m:0]	I/O	Selectable parity bus width from 1, 2, and 3-bit. MPI_DP[0] for MPI_D[7:0], MPI_DP[1] for MPI_D[15:8] and MPI_DP[2] for MPI_D[23:16].
MPI_TA	O	Transfer acknowledge. Driven active low indicates that MPI received the data on the write cycle or returned data on the read cycle.
MPI_TEA	O	Transfer Error Acknowledge. Driven active low indicates that MPI detects a bus error on the internal system bus for current transaction.
MPI_RETRY	O	Active low MPI Retry requests the MPC860 to relinquish the bus and retry the cycle.
Multi-chip Alignment (User I/O if not used.)		
MCA_DONE_OUT	O	Multi-chip alignment done output (to second MCA chip)
MCA_DONE_IN	I	Multi-chip alignment done input (from second MCA chip)
MCA_CLK_P[1:2]_OUT	O	Multi-chip alignment clock [1:2] output (sourced by MCA master chip)
MCA_CLK_P[1:2]_IN	I	Multi-chip alignment clock [1:2] input (from MCA master chip)
TEMP	—	Temperature sensing diode pin. Dedicated pin. Accuracy is typically +/- 10°C.
Miscellaneous Dedicated Pins		
XRES	—	External reference resistor between this pin and ground. The reference resistor is used to calibrate the programmable terminating resistors used in the I/Os. Dedicated pin. Value: 1K ± 1% ohm.
DIFFRx	—	Only used if a differential driver is used in a bank. This DIFFRx must be connected to ground via an external 1K ± 1% ohm resistor for all banks that have a differential driver.
SERDES Block (Dedicated Pins)		
[A:D]_HDINPx_[L/R]	I	High-speed input (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDINNx_[L/R]	I	High-speed input (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTPx_[L/R]	O	High-speed output (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTNx_[L/R]	O	High-speed output (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_REFCLKP_[L/R]	I	Ref clock input (positive), aux channel on left [L] or right [R] side of device.
[A:D]_REFCLKN_[L/R]	I	Ref clock input (negative), aux channel on left [L] or right [R] side of device.

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2}

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
E4	A_VDDAX25_L	-	
B1	A_REFCLKP_L	-	
C1	A_REFCLKN_L	-	
D2	RESP_ULC	-	
F5	RESETN	1	
D1	DONE	1	
E1	INITN	1	
E2	M0	1	
E3	M1	1	
E5	M2	1	
E6	M3	1	
F2	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
F1	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
F3	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G1	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
G4	PL18D	7	VREF2_7
H3	PL22A	7	
H2	PL22B	7	
H5	PL22C	7	VREF1_7
G5	PL22D	7	DIFFR_7
H1	PL23A	7	PCLKT7_1
J1	PL23B	7	PCLKC7_1
J2	PL24A	7	PCLKT7_0
J3	PL24B	7	PCLKC7_0
H4	PL24C	7	PCLKT7_2
H6	PL24D	7	PCLKC7_2
J4	PL26A	6	PCLKT6_0
K5	PL26B	6	PCLKC6_0
J5	PL26C	6	PCLKT6_1
J6	PL26D	6	PCLKC6_1
K1	PL28A	6	
L1	PL28B	6	
L4	PL28C	6	PCLKT6_2
K4	PL28D	6	PCLKC6_2
L2	PL31C	6	VREF1_6
L3	PL35A	6	
M3	PL35B	6	
M2	PL35D	6	DIFFR_6
M1	PL37A	6	
N1	PL37B	6	
P2	PL41D	6	VREF2_6
M5	PL43A	6	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AK14	PB25A	5		PB35A	5	
AK15	PB25B	5		PB35B	5	
AK16	PB27A	4		PB37A	4	
AK17	PB27B	4		PB37B	4	
AJ16	PB28A	4		PB38A	4	
AJ17	PB28B	4		PB38B	4	
AE16	PB28C	4		PB38C	4	
AH16	PB29A	4		PB39A	4	
AG16	PB29B	4		PB39B	4	
AK18	PB31A	4		PB41A	4	
AK19	PB31B	4		PB41B	4	
AH17	PB32A	4		PB42A	4	
AH18	PB32B	4		PB42B	4	
AG17	PB32D	4		PB42D	4	
AJ18	PB33A	4		PB43A	4	
AJ19	PB33B	4		PB43B	4	
AK20	PB35A	4	PCLKT4_2	PB46A	4	PCLKT4_2
AK21	PB35B	4	PCLKC4_2	PB46B	4	PCLKC4_2
AF18	PB36A	4	PCLKT4_1	PB47A	4	PCLKT4_1
AG18	PB36B	4	PCLKC4_1	PB47B	4	PCLKC4_1
AJ20	PB37A	4	PCLKT4_0	PB49A	4	PCLKT4_0
AJ21	PB37B	4	PCLKC4_0	PB49B	4	PCLKC4_0
AG19	PB37C	4	VREF2_4	PB49C	4	VREF2_4
AK22	PB39A	4	PCLKT4_5	PB51A	4	PCLKT4_5
AK23	PB39B	4	PCLKC4_5	PB51B	4	PCLKC4_5
AH19	PB39C	4		PB51C	4	
AK24	PB40A	4	PCLKT4_3	PB52A	4	PCLKT4_3
AK25	PB40B	4	PCLKC4_3	PB52B	4	PCLKC4_3
AE19	PB40C	4	PCLKT4_4	PB52C	4	PCLKT4_4
AE20	PB40D	4	PCLKC4_4	PB52D	4	PCLKC4_4
AE21	PB41A	4		PB53A	4	
AF21	PB41B	4		PB53B	4	
AG21	PB43A	4		PB55A	4	
AG22	PB43B	4		PB55B	4	
AH22	PB44A	4		PB56A	4	
AH23	PB44B	4		PB56B	4	
AH21	PB44C	4		PB56C	4	
AK28	PB45A	4		PB60A	4	
AK29	PB45B	4		PB60B	4	
AE22	PB45C	4		PB60C	4	
AJ28	PB47A	4		PB67A	4	
AH28	PB47B	4		PB67B	4	
AE24	PB47C	4	VREF1_4	PB67C	4	VREF1_4
AE25	PB47D	4		PB67D	4	
AJ29	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D14	PT15B	1	A15/MPI_ADDR29	PT25B	1	A15/MPI_ADDR29
D13	PT15A	1	A17/MPI_ADDR31	PT25A	1	A17/MPI_ADDR31
F12	PT13D	1	A19/MPI_TSI21	PT24D	1	A19/MPI_TSI21
F13	PT13C	1	A20/MPI_BDIP	PT24C	1	A20/MPI_BDIP
B12	PT11B	1	A18/MPI_TSI20	PT24B	1	A18/MPI_TSI20
B11	PT11A	1	MPI_TEA	PT24A	1	MPI_TEA
E12	PT10D	1	D14/MPI_DATA14	PT23D	1	D14/MPI_DATA14
D12	PT10C	1	DP1/MPI_PAR1	PT23C	1	DP1/MPI_PAR1
G10	PT9B	1	A21/MPI_BURST	PT23B	1	A21/MPI_BURST
G9	PT9A	1	D15/MPI_DATA15	PT23A	1	D15/MPI_DATA15
C10	A_VDDIB3_L	-		A_VDDIB3_L	-	
E9	VCC12	-		VCC12	-	
B10	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
B9	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A10	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
D9	VCC12	-		VCC12	-	
A9	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
C9	A_VDDOB3_L	-		A_VDDOB3_L	-	
A8	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
C8	A_VDDOB2_L	-		A_VDDOB2_L	-	
A7	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E8	VCC12	-		VCC12	-	
B8	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
B7	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
C7	A_VDDIB2_L	-		A_VDDIB2_L	-	
D8	VCC12	-		VCC12	-	
C6	A_VDDIB1_L	-		A_VDDIB1_L	-	
E7	VCC12	-		VCC12	-	
B6	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
B5	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A6	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
D7	VCC12	-		VCC12	-	
A5	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
C5	A_VDDOB1_L	-		A_VDDOB1_L	-	
A4	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
C4	A_VDDOB0_L	-		A_VDDOB0_L	-	
A3	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E6	VCC12	-		VCC12	-	
B4	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
B3	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
C3	A_VDDIB0_L	-		A_VDDIB0_L	-	
D6	VCC12	-		VCC12	-	
L5	NC	-		PL21A	7	
M5	NC	-		PL21B	7	
G2	NC	-		PL20A	7	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y9	VCCIO6	-		VCCIO6	-	
J7	VCCIO7	-		VCCIO7	-	
J8	VCCIO7	-		VCCIO7	-	
K7	VCCIO7	-		VCCIO7	-	
K8	VCCIO7	-		VCCIO7	-	
L8	VCCIO7	-		VCCIO7	-	
L9	VCCIO7	-		VCCIO7	-	
M9	VCCIO7	-		VCCIO7	-	
N9	VCCIO7	-		VCCIO7	-	
P9	VCCIO7	-		VCCIO7	-	
R9	VCCIO7	-		VCCIO7	-	
A1	GND	-		GND	-	
A30	GND	-		GND	-	
AA15	GND	-		GND	-	
AA16	GND	-		GND	-	
AK1	GND	-		GND	-	
AK30	GND	-		GND	-	
K15	GND	-		GND	-	
K16	GND	-		GND	-	
L11	GND	-		GND	-	
L12	GND	-		GND	-	
L13	GND	-		GND	-	
L14	GND	-		GND	-	
L15	GND	-		GND	-	
L16	GND	-		GND	-	
L17	GND	-		GND	-	
L18	GND	-		GND	-	
L19	GND	-		GND	-	
L20	GND	-		GND	-	
M11	GND	-		GND	-	
M12	GND	-		GND	-	
M13	GND	-		GND	-	
M14	GND	-		GND	-	
M15	GND	-		GND	-	
M16	GND	-		GND	-	
M17	GND	-		GND	-	
M18	GND	-		GND	-	
M19	GND	-		GND	-	
M20	GND	-		GND	-	
N11	GND	-		GND	-	
N12	GND	-		GND	-	
N13	GND	-		GND	-	
N14	GND	-		GND	-	
N15	GND	-		GND	-	
N16	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM21	PB29A	5		PB38A	5	
AM20	PB29B	5		PB38B	5	
AH21	PB29C	5		PB38C	5	
AH20	PB29D	5		PB38D	5	
AJ18	PB31A	5		PB39A	5	
AK18	PB31B	5		PB39B	5	
AH19	PB31C	5		PB39C	5	
AH18	PB31D	5		PB39D	5	
AL19	PB32A	5		PB41A	5	
AM19	PB32B	5		PB41B	5	
AH17	PB32C	5		PB41C	5	
AG17	PB32D	5		PB41D	5	
AL18	PB33A	5		PB42A	5	
AM18	PB33B	5		PB42B	5	
AC17	PB33C	5		PB42C	5	
AD17	PB33D	5		PB42D	5	
AL17	PB35A	5		PB43A	5	
AM17	PB35B	5		PB43B	5	
AE17	PB35C	5		PB43C	5	
AF17	PB35D	5		PB43D	5	
AM16	PB37A	4		PB45A	4	
AL16	PB37B	4		PB45B	4	
AF16	PB37C	4		PB45C	4	
AE16	PB37D	4		PB45D	4	
AM15	PB38A	4		PB46A	4	
AL15	PB38B	4		PB46B	4	
AD16	PB38C	4		PB46C	4	
AC16	PB38D	4		PB46D	4	
AM14	PB39A	4		PB47A	4	
AL14	PB39B	4		PB47B	4	
AG16	PB39C	4		PB47C	4	
AH16	PB39D	4		PB47D	4	
AK15	PB41A	4		PB49A	4	
AJ15	PB41B	4		PB49B	4	
AH15	PB41C	4		PB49C	4	
AH14	PB41D	4		PB49D	4	
AM13	PB42A	4		PB50A	4	
AM12	PB42B	4		PB50B	4	
AH13	PB42C	4		PB50C	4	
AH12	PB42D	4		PB50D	4	
AK14	PB43A	4		PB51A	4	
AJ14	PB43B	4		PB51B	4	
AE15	PB43C	4		PB51C	4	
AD15	PB43D	4		PB51D	4	
AL13	PB46A	4	PCLKT4_2	PB53A	4	PCLKT4_2
AL12	PB46B	4	PCLKC4_2	PB53B	4	PCLKC4_2
AG14	PB46C	4	PCLKT4_7	PB53C	4	PCLKT4_7
AG13	PB46D	4	PCLKC4_7	PB53D	4	PCLKC4_7
AM11	PB47A	4	PCLKT4_1	PB54A	4	PCLKT4_1
AM10	PB47B	4	PCLKC4_1	PB54B	4	PCLKC4_1

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B30	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
D30	A_VDDOB0_L	-		A_VDDOB0_L	-	
A30	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
C31	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
C32	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
B31	A_VDDIB0_L	-		A_VDDIB0_L	-	
AL25	NC	-		PB26A	5	
AL24	NC	-		PB26B	5	
AG27	NC	-		PB26C	5	
AH27	NC	-		PB26D	5	
AM25	NC	-		PB27A	5	
AM24	NC	-		PB27B	5	
AL9	NC	-		PB62A	4	
AL8	NC	-		PB62B	4	
AK9	NC	-		PB63A	4	
AJ9	NC	-		PB63B	4	
AG10	NC	-		PB63C	4	
AG11	NC	-		PB63D	4	
J30	NC	-		PL26A	7	
H30	NC	-		PL26B	7	
M28	NC	-		PL26C	7	
N28	NC	-		PL26D	7	
J32	NC	-		PL27A	7	
J31	NC	-		PL27B	7	
N26	NC	-		PL27C	7	
N27	NC	-		PL27D	7	
K31	NC	-		PL29A	7	
K32	NC	-		PL29B	7	
P25	NC	-		PL29C	7	
P26	NC	-		PL29D	7	
L27	NC	-		PL22C	7	
L28	NC	-		PL22D	7	
M29	NC	-		PL30A	7	
L29	NC	-		PL30B	7	
M30	NC	-		PL31A	7	
L30	NC	-		PL31B	7	
L31	NC	-		PL34A	7	
M31	NC	-		PL34B	7	
AA29	NC	-		PL56A	6	
AA30	NC	-		PL56B	6	
AB31	NC	-		PL57A	6	
AA31	NC	-		PL57B	6	
AG30	NC	-		PL57C	6	
AG29	NC	-		PL57D	6	
AB29	NC	-		PL58A	6	
AB30	NC	-		PL58B	6	
Y25	NC	-		PL58C	6	
AA25	NC	-		PL58D	6	
AA8	NC	-		PR58D	3	
Y8	NC	-		PR58C	3	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
U12	VCC12	-		VCC12	-	
U21	VCC12	-		VCC12	-	
AA16	VCC12	-		VCC12	-	
AA17	VCC12	-		VCC12	-	
M14	VCC12	-		VCC12	-	
P12	VCC12	-		VCC12	-	
W12	VCC12	-		VCC12	-	
AA14	VCC12	-		VCC12	-	
AA19	VCC12	-		VCC12	-	
W21	VCC12	-		VCC12	-	
P21	VCC12	-		VCC12	-	
M19	VCC12	-		VCC12	-	
A2	GND	-		GND	-	
A10	GND	-		GND	-	
E28	NC	-		NC	-	
E5	NC	-		NC	-	
F10	NC	-		NC	-	
E10	NC	-		NC	-	
E23	NC	-		NC	-	
F23	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M25 and LatticeSC/M40 in a 1020-pin package support a 16-bit MPI interface.

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD8	PR65C	3		PR89C	3	
AJ3	PR65B	3		PR89B	3	
AH3	PR65A	3		PR89A	3	
AD7	PR62D	3		PR86D	3	
AC7	PR62C	3		PR86C	3	
AJ2	PR62B	3		PR86B	3	
AH2	PR62A	3		PR86A	3	
AF6	PR61D	3		PR85D	3	
AF5	PR61C	3		PR85C	3	
AF4	PR61B	3		PR85B	3	
AE4	PR61A	3		PR85A	3	
AD6	PR60D	3		PR84D	3	
AC6	PR60C	3		PR84C	3	
AG2	PR60B	3		PR84B	3	
AF2	PR60A	3		PR84A	3	
AC8	PR58D	3		PR82D	3	
AB8	PR58C	3		PR82C	3	
AK1	PR58B	3		PR82B	3	
AJ1	PR58A	3		PR82A	3	
AB10	PR57D	3		PR81D	3	
AA10	PR57C	3		PR81C	3	
AF3	PR57B	3		PR81B	3	
AE3	PR57A	3		PR81A	3	
AE5	PR56D	3		PR80D	3	
AD5	PR56C	3		PR80C	3	
AE2	PR56B	3		PR80B	3	
AD2	PR56A	3		PR80A	3	
AC5	PR53D	3		PR78D	3	
AB5	PR53C	3		PR78C	3	
AF1	PR53B	3		PR78B	3	
AE1	PR53A	3		PR78A	3	
AA11	PR52D	3		PR77D	3	
Y11	PR52C	3		PR77C	3	
AC4	PR52B	3		PR77B	3	
AB4	PR52A	3		PR77A	3	
AA8	PR51D	3	DIFFR_3	PR76D	3	DIFFR_3
AA9	PR51C	3		PR76C	3	
AC3	PR51B	3		PR76B	3	
AB3	PR51A	3		PR76A	3	
AA7	PR49D	3		PR65D	3	
Y7	PR49C	3		PR65C	3	
AA2	PR49B	3		PR65B	3	
Y2	PR49A	3		PR65A	3	
AA6	PR48D	3		PR63D	3	
Y6	PR48C	3		PR63C	3	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D7	B_VDDIB0_R	-		B_VDDIB0_R	-	
E10	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
F10	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
K10	VCC12	-		VCC12	-	
A11	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D10	B_VDDOB0_R	-		B_VDDOB0_R	-	
B11	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D11	B_VDDOB1_R	-		B_VDDOB1_R	-	
B12	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L10	VCC12	-		VCC12	-	
A12	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
F11	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
E11	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
G11	VCC12	-		VCC12	-	
D8	B_VDDIB1_R	-		B_VDDIB1_R	-	
G12	VCC12	-		VCC12	-	
D9	B_VDDIB2_R	-		B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-		VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-		B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-		B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-		VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-		VCC12	-	
E9	B_VDDIB3_R	-		B_VDDIB3_R	-	
L13	VCC12	-		VCC12	-	
J11	B_REFCLKN_R	-		B_REFCLKN_R	-	
H11	B_REFCLKP_R	-		B_REFCLKP_R	-	
M15	PT61D	1	HDC/SI	PT77D	1	HDC/SI
M16	PT61C	1	LDCN/SCS	PT77C	1	LDCN/SCS
F14	PT59B	1	D8/MPI_DATA8	PT77B	1	D8/MPI_DATA8
G14	PT59A	1	CS1/MPI_CS1	PT77A	1	CS1/MPI_CS1
L15	PT58D	1	D9/MPI_DATA9	PT75D	1	D9/MPI_DATA9
L14	PT58C	1	D10/MPI_DATA10	PT75C	1	D10/MPI_DATA10
D14	PT57B	1	CS0N/MPI_CS0N	PT75B	1	CS0N/MPI_CS0N
E14	PT57A	1	RDN/MPI_STRB_N	PT75A	1	RDN/MPI_STRB_N
L16	PT55D	1	WRN/MPI_WR_N	PT74D	1	WRN/MPI_WR_N
K16	PT55C	1	D7/MPI_DATA7	PT74C	1	D7/MPI_DATA7
G15	PT55B	1	D6/MPI_DATA6	PT74B	1	D6/MPI_DATA6

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J3	PR45A	2	
M8	PR43D	2	DIFFR_2
L8	PR43C	2	VREF1_2
K4	PR43B	2	
J4	PR43A	2	
M7	PR26D	2	
L7	PR26C	2	
J5	PR26B	2	
H5	PR26A	2	
N9	PR19D	2	
P9	PR19C	2	
G3	PR19B	2	
F3	PR19A	2	
J6	PR18D	2	VREF2_2
H6	PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
D2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
G4	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
F4	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
J7	PR15D	2	
H7	PR15C	2	
G5	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
F5	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
C2	VCCJ	-	
M9	TDO	-	TDO
L9	TMS	-	
D1	TCK	-	
C1	TDI	-	
J8	PROGRAMN	1	
K8	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
B2	CCLK	1	
H9	RESP_URC	-	
H10	VCC12	-	
H8	A_REFCLKN_R	-	
G8	A_REFCLKP_R	-	
C3	VCC12	-	
D3	A_VDDIB0_R	-	
A3	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B3	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E5	VCC12	-	
A4	A_HDOUPT0_R	-	PCS 3E0 CH 0 OUT P

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2}

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G34	A_REFCLKP_L	-		A_REFCLKP_L	-	
H34	A_REFCLKN_L	-		A_REFCLKN_L	-	
N30	VCC12	-		VCC12	-	
H33	RESP_ULC	-		RESP_ULC	-	
P25	RESETN	1		RESETN	1	
P26	TSALLN	1		TSALLN	1	
P31	DONE	1		DONE	1	
P23	INITN	1		INITN	1	
P30	M0	1		M0	1	
P22	M1	1		M1	1	
P24	M2	1		M2	1	
R22	M3	1		M3	1	
J37	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J38	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
P32	PL16C	7		PL15C	7	
R32	PL16D	7		PL15D	7	
G40	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
H40	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N33	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P33	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
G41	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
H41	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
T29	PL18C	7		PL18C	7	
U29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
G42	PL20A	7		PL19A	7	
H42	PL20B	7		PL19B	7	
M34	PL20C	7		PL19C	7	
M35	PL20D	7		PL19D	7	
K37	PL21A	7		PL26A	7	
L37	PL21B	7		PL26B	7	
N34	PL21C	7		PL26C	7	
P34	PL21D	7		PL26D	7	
K38	PL22A	7		PL30A	7	
L38	PL22B	7		PL30B	7	
T33	PL22C	7		PL30C	7	
R33	PL22D	7		PL30D	7	
J41	PL24A	7		PL34A	7	
K41	PL24B	7		PL34B	7	
U31	PL24C	7		PL34C	7	
V31	PL24D	7		PL34D	7	
K42	PL25A	7		PL38A	7	
J42	PL25B	7		PL38B	7	
J36	PL25C	7		PL38C	7	
K36	PL25D	7		PL38D	7	
N38	PL26A	7		PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H18	PT77C	1	LDCN/SCS	PT93C	1	LDCN/SCS
F18	PT77B	1	D8/MPI_DATA8	PT93B	1	D8/MPI_DATA8
E18	PT77A	1	CS1/MPI_CS1	PT93A	1	CS1/MPI_CS1
H19	PT75D	1	D9/MPI_DATA9	PT90D	1	D9/MPI_DATA9
G19	PT75C	1	D10/MPI_DATA10	PT90C	1	D10/MPI_DATA10
D19	PT75B	1	CS0N/MPI_CS0N	PT90B	1	CS0N/MPI_CS0N
D18	PT75A	1	RDN/MPI_STRB_N	PT90A	1	RDN/MPI_STRB_N
J20	PT74D	1	WRN/MPI_WR_N	PT89D	1	WRN/MPI_WR_N
K20	PT74C	1	D7/MPI_DATA7	PT89C	1	D7/MPI_DATA7
E19	PT74B	1	D6/MPI_DATA6	PT89B	1	D6/MPI_DATA6
F19	PT74A	1	D5/MPI_DATA5	PT89A	1	D5/MPI_DATA5
K18	PT73D	1	D4/MPI_DATA4	PT87D	1	D4/MPI_DATA4
J18	PT73C	1	D3/MPI_DATA3	PT87C	1	D3/MPI_DATA3
A19	PT73B	1	D2/MPI_DATA2	PT87B	1	D2/MPI_DATA2
B19	PT73A	1	D1/MPI_DATA1	PT87A	1	D1/MPI_DATA1
H17	PT71D	1	D16/PCLKC1_3/MPI_DATA16	PT86D	1	D16/PCLKC1_3/MPI_DATA16
J17	PT71C	1	D17/PCLKT1_3/MPI_DATA17	PT86C	1	D17/PCLKT1_3/MPI_DATA17
B20	PT71B	1	D0/MPI_DATA0	PT86B	1	D0/MPI_DATA0
C20	PT71A	1	QOUT/CEON	PT86A	1	QOUT/CEON
M20	PT70D	1	VREF2_1	PT83D	1	VREF2_1
L20	PT70C	1	D18/MPI_DATA18	PT83C	1	D18/MPI_DATA18
F20	PT70B	1	DOUT	PT83B	1	DOUT
G20	PT70A	1	MCA_DONE_IN	PT83A	1	MCA_DONE_IN
K19	PT69D	1	D19/PCLKC1_2/MPI_DATA19	PT81D	1	D19/PCLKC1_2/MPI_DATA19
J19	PT69C	1	D20/PCLKT1_2/MPI_DATA20	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D20	PT69B	1	MCA_CLK_P1_OUT	PT81B	1	MCA_CLK_P1_OUT
E20	PT69A	1	MCA_CLK_P1_IN	PT81A	1	MCA_CLK_P1_IN
H21	PT67D	1	D21/PCLKC1_1/MPI_DATA21	PT78D	1	D21/PCLKC1_1/MPI_DATA21
G21	PT67C	1	D22/PCLKT1_1/MPI_DATA22	PT78C	1	D22/PCLKT1_1/MPI_DATA22
B21	PT67B	1	MCA_CLK_P2_OUT	PT78B	1	MCA_CLK_P2_OUT
C21	PT67A	1	MCA_CLK_P2_IN	PT78A	1	MCA_CLK_P2_IN
M21	PT66D	1	MCA_DONE_OUT	PT75D	1	MCA_DONE_OUT
L21	PT66C	1	BUSYN/RCLK/SCK	PT75C	1	BUSYN/RCLK/SCK
A21	PT66B	1	DP0/MPI_PAR0	PT75B	1	DP0/MPI_PAR0
A20	PT66A	1	MPI_TA	PT75A	1	MPI_TA
J21	PT65D	1	D23/MPI_DATA23	PT73D	1	D23/MPI_DATA23
K21	PT65C	1	DP2/MPI_PAR2	PT73C	1	DP2/MPI_PAR2
E21	PT65B	1	PCLKC1_0	PT73B	1	PCLKC1_0
F21	PT65A	1	PCLKT1_0/MPI_CLK	PT73A	1	PCLKT1_0/MPI_CLK
G22	PT63D	1	DP3/PCLKC1_4/MPI_PAR3	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H22	PT63C	1	D24/PCLKT1_4/MPI_DATA24	PT71C	1	D24/PCLKT1_4/MPI_DATA24
A23	PT63B	1	MPI_RETRY	PT71B	1	MPI_RETRY
A22	PT63A	1	A0/MPI_ADDR14	PT71A	1	A0/MPI_ADDR14
L22	PT61D	1	A1/MPI_ADDR15	PT69D	1	A1/MPI_ADDR15
M22	PT61C	1	A2/MPI_ADDR16	PT69C	1	A2/MPI_ADDR16

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM27	GND	-		GND	-	
AM36	GND	-		GND	-	
AM7	GND	-		GND	-	
AP4	GND	-		GND	-	
AP40	GND	-		GND	-	
AR14	GND	-		GND	-	
AR20	GND	-		GND	-	
AR23	GND	-		GND	-	
AR29	GND	-		GND	-	
AR35	GND	-		GND	-	
AR8	GND	-		GND	-	
AT11	GND	-		GND	-	
AT17	GND	-		GND	-	
AT26	GND	-		GND	-	
AT32	GND	-		GND	-	
AU3	GND	-		GND	-	
AU39	GND	-		GND	-	
AW12	GND	-		GND	-	
AW18	GND	-		GND	-	
AW22	GND	-		GND	-	
AW28	GND	-		GND	-	
AW34	GND	-		GND	-	
AW6	GND	-		GND	-	
AY15	GND	-		GND	-	
AY21	GND	-		GND	-	
AY25	GND	-		GND	-	
AY31	GND	-		GND	-	
AY37	GND	-		GND	-	
AY9	GND	-		GND	-	
B1	GND	-		GND	-	
B42	GND	-		GND	-	
BA1	GND	-		GND	-	
BA42	GND	-		GND	-	
BB2	GND	-		GND	-	
BB41	GND	-		GND	-	
C10	GND	-		GND	-	
C12	GND	-		GND	-	
C13	GND	-		GND	-	
C16	GND	-		GND	-	
C18	GND	-		GND	-	
C19	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C27	GND	-		GND	-	
C28	GND	-		GND	-	