# Lattice Semiconductor Corporation - LFSC3GA115E-6FC1152C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 28750 |
| Number of Logic Elements/Cells | 115000 |
| Total RAM Bits | 7987200 |
| Number of I/O | 660 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BCBGA, FCBGA |
| Supplier Device Package | 1152-CFCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga115e-6fc1152c |

*Table 1-1. LatticeSC Family Selection Guide*[1]

| Device | SC15 | SC25 | SC40 | SC80 | SC115 |
|---|---|---|---|---|---|
| LUT4s (K) | 15 | 25 | 40 | 80 | 115 |
| sysMEM Blocks (18Kb) | 56 | 104 | 216 | 308 | 424 |
| Embedded Memory (Mbits) | 1.03 | 1.92 | 3.98 | 5.68 | 7.8 |
| Max. Distributed Memory (Mbits) | 0.24 | 0.41 | 0.65 | 1.28 | 1.84 |
| Number of 3.8Gbps SERDES (Max.) | 8 | 16 | 16 | 32 | 32 |
| DLLs | 12 | 12 | 12 | 12 | 12 |
| Analog PLLs | 8 | 8 | 8 | 8 | 8 |
| MACO Blocks | 4 | 6 | 10 | 10 | 12 |
| **Package I/O/SERDES Combinations (1mm ball pitch)** | | | | | |
| 256-ball fpBGA (17 x 17mm) | 139/4 | | | | |
| 900-ball fpBGA (31 x 31mm) | 300/8 | 378/8 | | | |
| 1020-ball fcBGA (33 x 33mm)[2] | | 476/16 | 562/16 | | |
| 1152-ball fcBGA (35 x 35mm)[3] | | | 604/16 | 660/16 | 660/16 |
| 1704-ball fcBGA (42.5 x 42.5mm)[3] | | | | 904/32 | 942/32 |

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per PCN #02A-10.
3. Ceramic fcBGA converted to organic fcBGA per PCN #01A-10.

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

*Table 1-2. LatticeSCM Family*

| Device | SCM15 | SCM25 | SCM40 | SCM80 | SCM115 |
|---|---|---|---|---|---|
| flexiMAC Blocks<br>• 1GbE Mode<br>• 10GbE Mode<br>• PCI Express Mode | 1 | 2 | 2 | 2 | 4 |
| SPI4.2 Blocks | 1 | 2 | 2 | 2 | 2 |
| Memory Controller Blocks<br>• DDR/DDR2 DRAM Mode<br>• QDR II/II+ SRAM Mode<br>• RLDRAM I<br>• RLDRAM II CIO/SIO | 1 | 2 | 2 | 2 | 2 |
| Low-Speed CDR Blocks | 0 | 0 | 2 | 2 | 2 |
| PCI Express LTSSM (PHY) Blocks | 1 | 0 | 2 | 2 | 2 |

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

## Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

# LatticeSC/M Family Data Sheet Architecture

**December 2008** **Data Sheet DS1004**

## Architecture Overview

The LatticeSC architecture contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR). The upper left and upper right corners of the devices contain SERDES blocks and their associated PCS blocks, as show in Figure 2-1.

Top left and top right corner of the device contain blocks of SERDES. Each block of SERDES contains four channels (quad). Each channel contains a single serializer and de-serializer, synchronization and word alignment logic. The SERDES quad connects with the Physical Coding Sub-layer (PCS) blocks that contain logic to simultaneously perform alignment, coding, de-coding and other functions. The SERDES quad block has separate supply, ground and reference voltage pins.

The PICs contain logic to facilitate the conditioning of signals to and from the I/O before they leave or enter the FPGA fabric. The block provides DDR and shift register capabilities that act as a gearbox between high speed I/O and the FPGA fabric. The blocks also contain programmable Adaptive Input Logic that adjusts the delay applied to signals as they enter the device to optimize setup and hold times and ensure robust performance.

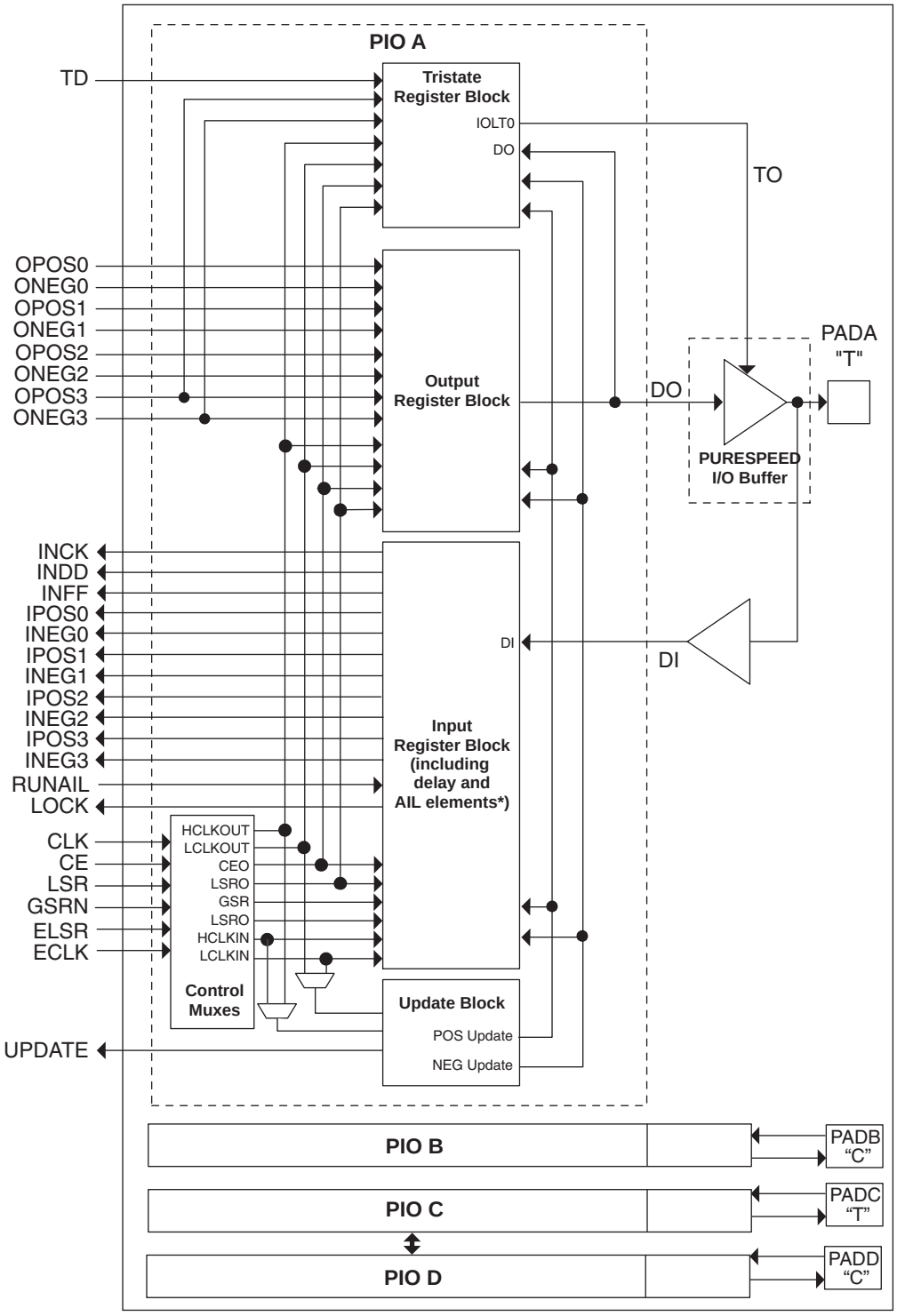
sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM, ROM or FIFO. These blocks have dedicated logic to simplify the implementation of FIFOs.

The PFU, PIC and EBR blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. These blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

The corners contain the sysCLOCK Analog Phase Locked Loop (PLL) and Delay Locked Loop (DLL) Blocks. The PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeSC architecture provides eight analog PLLs per device and 12 DLLs. The DLLs provide a simple delay capability and can also be used to calibrate other delays within the device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG™ port which allows for serial or parallel device configuration. The system bus simplifies the connections of the external microprocessor to the device for tasks such as SERDES and PCS configuration or interface to the general FPGA logic. The LatticeSC devices use 1.2V as their core voltage operation with 1.0V operation also possible.

***Figure 2-17. PIC Diagram***




*AIL only on A or C pads located on the left, right and bottom of the device.

The A/B PIOs on the left and the right of the device can be paired to form a differentiated driver. The A/B and C/D PIOs on all sides of the device can be paired to form differential receivers. Either A or C PIOs on all sides except the one on top also provide a connection to an adaptive input logic capability that facilitates the implementation of

PCI Specification, Revision 2.2 requires the use of clamping diodes for 3.3V operation. For more information on the PCI interface, please refer to the PCI Specification, Revision 2.2.

## Programmable Slew Rate Control

All output and bidirectional buffers have an optional programmable output slew rate control that can be configured for either low noise or high-speed performance. Each I/O pin has an individual slew rate control. This allows designers to specify slew rate control on a pin-by-pin basis. This slew rate control affects both the rising and falling edges.

## Programmable Termination

Many of the I/O standards supported by the LatticeSC devices require termination at the transmitter, receiver or both. The SC devices provide the capability to implement many kinds of termination on-chip, minimizing stub lengths and hence improving performance. Utilizing this feature also has the benefit of reducing the number of discrete components required on the circuit board. The termination schemes can be split into two categories single-ended and differential.

### Single Ended Termination

**Single Ended Outputs:** The SC devices support a number of different terminations for single ended outputs:

- Series
- Parallel to $V_{CCIO}$ or GND
- Parallel to $V_{CCIO}/2$
- Parallel to $V_{CCIO}/2$ combined with series

Figure 2-27 shows the single ended output schemes that are supported. The nominal values of the termination resistors are shown in Table 2-10.

## Switching Test Conditions

Figure 3-15 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-4.

***Figure 3-15. Output Test Load, LVTTL and LVCMOS Standards***

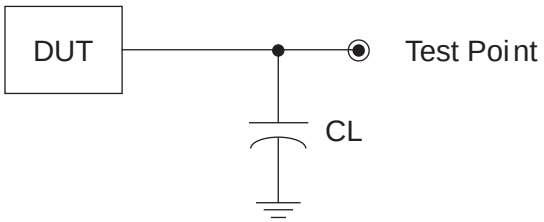



***Table 3-4. Test Fixture Required Components, Non-Terminated Interfaces***

| Test Condition | $C_L$ | Timing Ref. | $V_T$ |
|---|---|---|---|
| LVTTL and other LVCMOS settings (L -> H, H -> L) | 30pF | LVCMOS 3.3 = 1.5V | — |
| | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> H) | 30pF | $V_{CCIO}/2$ | $V_{OL}$ |
| LVCMOS 2.5 I/O (Z -> L) | | $V_{CCIO}/2$ | $V_{OH}$ |
| LVCMOS 2.5 I/O (H -> Z) | | $V_{OH}$ - 0.15 | $V_{OL}$ |
| LVCMOS 2.5 I/O (L -> Z) | | $V_{OL}$ + 0.15 | $V_{OH}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AH29 | PB48B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D | PB68B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D |
| AE26 | PB48C | 4 | | PB68C | 4 | |
| AD25 | PB48D | 4 | | PB68D | 4 | |
| AJ30 | PB49A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B | PB69A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B |
| AH30 | PB49B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B | PB69B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B |
| AG28 | PB49C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C | PB69C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C |
| AG29 | PB49D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C | PB69D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C |
| AF26 | VCC12 | - | | VCC12 | - | |
| AD27 | PROBE_VCC | - | | PROBE_VCC | - | |
| AG27 | VCC12 | - | | VCC12 | - | |
| AE28 | PROBE_GND | - | | PROBE_GND | - | |
| AC25 | PR45D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A | PR57D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A |
| AD26 | PR45C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A | PR57C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A |
| AF28 | PR45B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E | PR57B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E |
| AF29 | PR45A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E | PR57A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E |
| AC26 | PR44D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F | PR55D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F |
| AB26 | PR44C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F | PR55C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F |
| AG30 | PR44B | 3 | | PR55B | 3 | |
| AF30 | PR44A | 3 | | PR55A | 3 | |
| AC28 | PR43B | 3 | | PR52B | 3 | |
| AB28 | PR43A | 3 | | PR52A | 3 | |
| AB27 | PR41D | 3 | VREF2_3 | PR51D | 3 | VREF2_3 |
| AE30 | PR41B | 3 | | PR51B | 3 | |
| AD30 | PR41A | 3 | | PR51A | 3 | |
| AB25 | PR40B | 3 | | PR49B | 3 | |
| AA25 | PR40A | 3 | | PR49A | 3 | |
| AA30 | PR39B | 3 | | PR48B | 3 | |
| Y30 | PR39A | 3 | | PR48A | 3 | |
| W29 | PR37B | 3 | | PR44B | 3 | |
| V29 | PR37A | 3 | | PR44A | 3 | |
| U30 | PR36B | 3 | | PR43B | 3 | |
| T30 | PR36A | 3 | | PR43A | 3 | |
| V25 | PR35D | 3 | DIFFR_3 | PR42D | 3 | DIFFR_3 |
| W28 | PR35B | 3 | | PR42B | 3 | |
| V28 | PR35A | 3 | | PR42A | 3 | |
| R30 | PR33B | 3 | | PR38B | 3 | |
| P30 | PR33A | 3 | | PR38A | 3 | |
| N30 | PR32B | 3 | | PR35B | 3 | |
| M29 | PR32A | 3 | | PR35A | 3 | |
| U26 | PR31D | 3 | | PR34D | 3 | |
| T26 | PR31C | 3 | VREF1_3 | PR34C | 3 | VREF1_3 |
| U28 | PR31B | 3 | | PR34B | 3 | |
| T28 | PR31A | 3 | | PR34A | 3 | |
| M30 | PR28D | 3 | PCLKC3_2 | PR31D | 3 | PCLKC3_2 |
| L29 | PR28C | 3 | PCLKT3_2 | PR31C | 3 | PCLKT3_2 |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| Y24 | PL48C | 6 | | PL61C | 6 | |
| Y23 | PL48D | 6 | | PL61D | 6 | |
| AD29 | PL49A | 6 | | PL62A | 6 | |
| AD30 | PL49B | 6 | | PL62B | 6 | |
| AF28 | PL49C | 6 | | PL62C | 6 | |
| AE28 | PL49D | 6 | | PL62D | 6 | |
| AC28 | PL51A | 6 | | PL65A | 6 | |
| AD28 | PL51B | 6 | | PL65B | 6 | |
| AB26 | PL51C | 6 | | PL65C | 6 | |
| AC26 | PL51D | 6 | VREF2_6 | PL65D | 6 | VREF2_6 |
| AC32 | PL52A | 6 | | PL66A | 6 | |
| AD32 | PL52B | 6 | | PL66B | 6 | |
| AA24 | PL52C | 6 | | PL66C | 6 | |
| AA23 | PL52D | 6 | | PL66D | 6 | |
| AE30 | PL53A | 6 | | PL67A | 6 | |
| AE29 | PL53B | 6 | | PL67B | 6 | |
| AC25 | PL53C | 6 | | PL67C | 6 | |
| AB25 | PL53D | 6 | | PL67D | 6 | |
| AE31 | PL55A | 6 | | PL69A | 6 | |
| AE32 | PL55B | 6 | | PL69B | 6 | |
| AE26 | PL55C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F | PL69C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F |
| AE27 | PL55D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F | PL69D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F |
| AF32 | PL56A | 6 | | PL70A | 6 | |
| AF31 | PL56B | 6 | | PL70B | 6 | |
| AC24 | PL56C | 6 | | PL70C | 6 | |
| AD25 | PL56D | 6 | | PL70D | 6 | |
| AG32 | PL57A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E | PL71A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E |
| AG31 | PL57B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E | PL71B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E |
| AC23 | PL57C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A | PL71C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A |
| AD24 | PL57D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A | PL71D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A |
| AH32 | XRES | - | | XRES | - | |
| AH31 | TEMP | 6 | | TEMP | 6 | |
| AJ32 | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B |
| AK32 | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B |
| AF27 | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| AG28 | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| AK31 | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C |
| AL31 | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C |
| AE25 | PB4C | 5 | | PB4C | 5 | |
| AE24 | PB4D | 5 | | PB4D | 5 | |
| AK30 | PB5A | 5 | | PB5A | 5 | |
| AL30 | PB5B | 5 | | PB5B | 5 | |
| AD23 | PB5C | 5 | | PB5C | 5 | |
| AE23 | PB5D | 5 | VREF1_5 | PB5D | 5 | VREF1_5 |
| AK29 | PB7A | 5 | | PB7A | 5 | |
| AL29 | PB7B | 5 | | PB7B | 5 | |
| AF26 | PB7C | 5 | | PB7C | 5 | |
| AF25 | PB7D | 5 | | PB7D | 5 | |
| AJ28 | PB8A | 5 | | PB8A | 5 | |
| AK28 | PB8B | 5 | | PB8B | 5 | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| F19 | PT24A | 1 | MPI_TEA | PT30A | 1 | MPI_TEA |
| J18 | PT23D | 1 | D14/MPI_DATA14 | PT28D | 1 | D14/MPI_DATA14 |
| K18 | PT23C | 1 | DP1/MPI_PAR1 | PT28C | 1 | DP1/MPI_PAR1 |
| E20 | PT23B | 1 | A21/MPI_BURST | PT27B | 1 | A21/MPI_BURST |
| F20 | PT23A | 1 | D15/MPI_DATA15 | PT27A | 1 | D15/MPI_DATA15 |
| C23 | B_REFCLKP_L | - | | B_REFCLKP_L | - | |
| D23 | B_REFCLKN_L | - | | B_REFCLKN_L | - | |
| B23 | VCC12 | - | | VCC12 | - | |
| H21 | B_VDDIB3_L | - | | B_VDDIB3_L | - | |
| F21 | B_HDINP3_L | - | PCS 361 CH 3 IN P | B_HDINP3_L | - | PCS 361 CH 3 IN P |
| G21 | B_HDINN3_L | - | PCS 361 CH 3 IN N | B_HDINN3_L | - | PCS 361 CH 3 IN N |
| A21 | B_HDOUTP3_L | - | PCS 361 CH 3 OUT P | B_HDOUTP3_L | - | PCS 361 CH 3 OUT P |
| B21 | B_HDOUTN3_L | - | PCS 361 CH 3 OUT N | B_HDOUTN3_L | - | PCS 361 CH 3 OUT N |
| D21 | B_VDDOB3_L | - | | B_VDDOB3_L | - | |
| B22 | B_HDOUTN2_L | - | PCS 361 CH 2 OUT N | B_HDOUTN2_L | - | PCS 361 CH 2 OUT N |
| D22 | B_VDDOB2_L | - | | B_VDDOB2_L | - | |
| A22 | B_HDOUTP2_L | - | PCS 361 CH 2 OUT P | B_HDOUTP2_L | - | PCS 361 CH 2 OUT P |
| G22 | B_HDINN2_L | - | PCS 361 CH 2 IN N | B_HDINN2_L | - | PCS 361 CH 2 IN N |
| F22 | B_HDINP2_L | - | PCS 361 CH 2 IN P | B_HDINP2_L | - | PCS 361 CH 2 IN P |
| H22 | B_VDDIB2_L | - | | B_VDDIB2_L | - | |
| H24 | B_VDDIB1_L | - | | B_VDDIB1_L | - | |
| G23 | B_HDINP1_L | - | PCS 361 CH 1 IN P | B_HDINP1_L | - | PCS 361 CH 1 IN P |
| H23 | B_HDINN1_L | - | PCS 361 CH 1 IN N | B_HDINN1_L | - | PCS 361 CH 1 IN N |
| A24 | B_HDOUTP1_L | - | PCS 361 CH 1 OUT P | B_HDOUTP1_L | - | PCS 361 CH 1 OUT P |
| B24 | B_HDOUTN1_L | - | PCS 361 CH 1 OUT N | B_HDOUTN1_L | - | PCS 361 CH 1 OUT N |
| D24 | B_VDDOB1_L | - | | B_VDDOB1_L | - | |
| B25 | B_HDOUTN0_L | - | PCS 361 CH 0 OUT N | B_HDOUTN0_L | - | PCS 361 CH 0 OUT N |
| D25 | B_VDDOB0_L | - | | B_VDDOB0_L | - | |
| A25 | B_HDOUTP0_L | - | PCS 361 CH 0 OUT P | B_HDOUTP0_L | - | PCS 361 CH 0 OUT P |
| G25 | B_HDINN0_L | - | PCS 361 CH 0 IN N | B_HDINN0_L | - | PCS 361 CH 0 IN N |
| F25 | B_HDINP0_L | - | PCS 361 CH 0 IN P | B_HDINP0_L | - | PCS 361 CH 0 IN P |
| H25 | B_VDDIB0_L | - | | B_VDDIB0_L | - | |
| H26 | A_VDDIB3_L | - | | A_VDDIB3_L | - | |
| F26 | A_HDINP3_L | - | PCS 360 CH 3 IN P | A_HDINP3_L | - | PCS 360 CH 3 IN P |
| G26 | A_HDINN3_L | - | PCS 360 CH 3 IN N | A_HDINN3_L | - | PCS 360 CH 3 IN N |
| A26 | A_HDOUTP3_L | - | PCS 360 CH 3 OUT P | A_HDOUTP3_L | - | PCS 360 CH 3 OUT P |
| B26 | A_HDOUTN3_L | - | PCS 360 CH 3 OUT N | A_HDOUTN3_L | - | PCS 360 CH 3 OUT N |
| D26 | A_VDDOB3_L | - | | A_VDDOB3_L | - | |
| B27 | A_HDOUTN2_L | - | PCS 360 CH 2 OUT N | A_HDOUTN2_L | - | PCS 360 CH 2 OUT N |
| D27 | A_VDDOB2_L | - | | A_VDDOB2_L | - | |
| A27 | A_HDOUTP2_L | - | PCS 360 CH 2 OUT P | A_HDOUTP2_L | - | PCS 360 CH 2 OUT P |
| G27 | A_HDINN2_L | - | PCS 360 CH 2 IN N | A_HDINN2_L | - | PCS 360 CH 2 IN N |
| F27 | A_HDINP2_L | - | PCS 360 CH 2 IN P | A_HDINP2_L | - | PCS 360 CH 2 IN P |
| H27 | A_VDDIB2_L | - | | A_VDDIB2_L | - | |
| F29 | A_VDDIB1_L | - | | A_VDDIB1_L | - | |
| G28 | A_HDINP1_L | - | PCS 360 CH 1 IN P | A_HDINP1_L | - | PCS 360 CH 1 IN P |
| H28 | A_HDINN1_L | - | PCS 360 CH 1 IN N | A_HDINN1_L | - | PCS 360 CH 1 IN N |
| A29 | A_HDOUTP1_L | - | PCS 360 CH 1 OUT P | A_HDOUTP1_L | - | PCS 360 CH 1 OUT P |
| B29 | A_HDOUTN1_L | - | PCS 360 CH 1 OUT N | A_HDOUTN1_L | - | PCS 360 CH 1 OUT N |
| D29 | A_VDDOB1_L | - | | A_VDDOB1_L | - | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| D7 | B_VDDIB0_R | - | | B_VDDIB0_R | - | |
| E10 | B_HDINP0_R | - | PCS 3E1 CH 0 IN P | B_HDINP0_R | - | PCS 3E1 CH 0 IN P |
| F10 | B_HDINN0_R | - | PCS 3E1 CH 0 IN N | B_HDINN0_R | - | PCS 3E1 CH 0 IN N |
| K10 | VCC12 | - | | VCC12 | - | |
| A11 | B_HDOUTP0_R | - | PCS 3E1 CH 0 OUT P | B_HDOUTP0_R | - | PCS 3E1 CH 0 OUT P |
| D10 | B_VDDOB0_R | - | | B_VDDOB0_R | - | |
| B11 | B_HDOUTN0_R | - | PCS 3E1 CH 0 OUT N | B_HDOUTN0_R | - | PCS 3E1 CH 0 OUT N |
| D11 | B_VDDOB1_R | - | | B_VDDOB1_R | - | |
| B12 | B_HDOUTN1_R | - | PCS 3E1 CH 1 OUT N | B_HDOUTN1_R | - | PCS 3E1 CH 1 OUT N |
| L10 | VCC12 | - | | VCC12 | - | |
| A12 | B_HDOUTP1_R | - | PCS 3E1 CH 1 OUT P | B_HDOUTP1_R | - | PCS 3E1 CH 1 OUT P |
| F11 | B_HDINN1_R | - | PCS 3E1 CH 1 IN N | B_HDINN1_R | - | PCS 3E1 CH 1 IN N |
| E11 | B_HDINP1_R | - | PCS 3E1 CH 1 IN P | B_HDINP1_R | - | PCS 3E1 CH 1 IN P |
| G11 | VCC12 | - | | VCC12 | - | |
| D8 | B_VDDIB1_R | - | | B_VDDIB1_R | - | |
| G12 | VCC12 | - | | VCC12 | - | |
| D9 | B_VDDIB2_R | - | | B_VDDIB2_R | - | |
| E12 | B_HDINP2_R | - | PCS 3E1 CH 2 IN P | B_HDINP2_R | - | PCS 3E1 CH 2 IN P |
| F12 | B_HDINN2_R | - | PCS 3E1 CH 2 IN N | B_HDINN2_R | - | PCS 3E1 CH 2 IN N |
| K11 | VCC12 | - | | VCC12 | - | |
| A13 | B_HDOUTP2_R | - | PCS 3E1 CH 2 OUT P | B_HDOUTP2_R | - | PCS 3E1 CH 2 OUT P |
| D12 | B_VDDOB2_R | - | | B_VDDOB2_R | - | |
| B13 | B_HDOUTN2_R | - | PCS 3E1 CH 2 OUT N | B_HDOUTN2_R | - | PCS 3E1 CH 2 OUT N |
| D13 | B_VDDOB3_R | - | | B_VDDOB3_R | - | |
| B14 | B_HDOUTN3_R | - | PCS 3E1 CH 3 OUT N | B_HDOUTN3_R | - | PCS 3E1 CH 3 OUT N |
| L11 | VCC12 | - | | VCC12 | - | |
| A14 | B_HDOUTP3_R | - | PCS 3E1 CH 3 OUT P | B_HDOUTP3_R | - | PCS 3E1 CH 3 OUT P |
| F13 | B_HDINN3_R | - | PCS 3E1 CH 3 IN N | B_HDINN3_R | - | PCS 3E1 CH 3 IN N |
| E13 | B_HDINP3_R | - | PCS 3E1 CH 3 IN P | B_HDINP3_R | - | PCS 3E1 CH 3 IN P |
| G13 | VCC12 | - | | VCC12 | - | |
| E9 | B_VDDIB3_R | - | | B_VDDIB3_R | - | |
| L13 | VCC12 | - | | VCC12 | - | |
| J11 | B_REFCLKN_R | - | | B_REFCLKN_R | - | |
| H11 | B_REFCLKP_R | - | | B_REFCLKP_R | - | |
| M15 | PT61D | 1 | HDC/SI | PT77D | 1 | HDC/SI |
| M16 | PT61C | 1 | LDCN/SCS | PT77C | 1 | LDCN/SCS |
| F14 | PT59B | 1 | D8/MPI_DATA8 | PT77B | 1 | D8/MPI_DATA8 |
| G14 | PT59A | 1 | CS1/MPI_CS1 | PT77A | 1 | CS1/MPI_CS1 |
| L15 | PT58D | 1 | D9/MPI_DATA9 | PT75D | 1 | D9/MPI_DATA9 |
| L14 | PT58C | 1 | D10/MPI_DATA10 | PT75C | 1 | D10/MPI_DATA10 |
| D14 | PT57B | 1 | CS0N/MPI_CS0N | PT75B | 1 | CS0N/MPI_CS0N |
| E14 | PT57A | 1 | RDN/MPI_STRB_N | PT75A | 1 | RDN/MPI_STRB_N |
| L16 | PT55D | 1 | WRN/MPI_WR_N | PT74D | 1 | WRN/MPI_WR_N |
| K16 | PT55C | 1 | D7/MPI_DATA7 | PT74C | 1 | D7/MPI_DATA7 |
| G15 | PT55B | 1 | D6/MPI_DATA6 | PT74B | 1 | D6/MPI_DATA6 |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AM17 | VCCIO4 | - | | VCCIO4 | - | |
| AM5 | VCCIO4 | - | | VCCIO4 | - | |
| AE20 | VCCIO5 | - | | VCCIO5 | - | |
| AE23 | VCCIO5 | - | | VCCIO5 | - | |
| AE26 | VCCIO5 | - | | VCCIO5 | - | |
| AH22 | VCCIO5 | - | | VCCIO5 | - | |
| AH28 | VCCIO5 | - | | VCCIO5 | - | |
| AJ19 | VCCIO5 | - | | VCCIO5 | - | |
| AJ25 | VCCIO5 | - | | VCCIO5 | - | |
| AL18 | VCCIO5 | - | | VCCIO5 | - | |
| AL24 | VCCIO5 | - | | VCCIO5 | - | |
| AL30 | VCCIO5 | - | | VCCIO5 | - | |
| AM21 | VCCIO5 | - | | VCCIO5 | - | |
| AM27 | VCCIO5 | - | | VCCIO5 | - | |
| AA31 | VCCIO6 | - | | VCCIO6 | - | |
| AB29 | VCCIO6 | - | | VCCIO6 | - | |
| AC24 | VCCIO6 | - | | VCCIO6 | - | |
| AD32 | VCCIO6 | - | | VCCIO6 | - | |
| AE28 | VCCIO6 | - | | VCCIO6 | - | |
| AG31 | VCCIO6 | - | | VCCIO6 | - | |
| AK32 | VCCIO6 | - | | VCCIO6 | - | |
| T29 | VCCIO6 | - | | VCCIO6 | - | |
| U31 | VCCIO6 | - | | VCCIO6 | - | |
| V32 | VCCIO6 | - | | VCCIO6 | - | |
| W28 | VCCIO6 | - | | VCCIO6 | - | |
| Y26 | VCCIO6 | - | | VCCIO6 | - | |
| E31 | VCCIO7 | - | | VCCIO7 | - | |
| G28 | VCCIO7 | - | | VCCIO7 | - | |
| H32 | VCCIO7 | - | | VCCIO7 | - | |
| K29 | VCCIO7 | - | | VCCIO7 | - | |
| L31 | VCCIO7 | - | | VCCIO7 | - | |
| M25 | VCCIO7 | - | | VCCIO7 | - | |
| N28 | VCCIO7 | - | | VCCIO7 | - | |
| P32 | VCCIO7 | - | | VCCIO7 | - | |
| R25 | VCCIO7 | - | | VCCIO7 | - | |
| J25 | VCCIO1 | - | | VCCIO1 | - | |
| N11 | VTT_2 | 2 | | VTT_2 | 2 | |
| R12 | VTT_2 | 2 | | VTT_2 | 2 | |
| T12 | VTT_2 | 2 | | VTT_2 | 2 | |
| AB11 | VTT_3 | 3 | | VTT_3 | 3 | |
| W12 | VTT_3 | 3 | | VTT_3 | 3 | |
| Y12 | VTT_3 | 3 | | VTT_3 | 3 | |
| AC15 | VTT_4 | 4 | | VTT_4 | 4 | |
| AC16 | VTT_4 | 4 | | VTT_4 | 4 | |
| AD13 | VTT_4 | 4 | | VTT_4 | 4 | |

## LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AC19 | VTT_5 | 5 | | VTT_5 | 5 | |
| AC20 | VTT_5 | 5 | | VTT_5 | 5 | |
| AD22 | VTT_5 | 5 | | VTT_5 | 5 | |
| AB24 | VTT_6 | 6 | | VTT_6 | 6 | |
| W23 | VTT_6 | 6 | | VTT_6 | 6 | |
| Y23 | VTT_6 | 6 | | VTT_6 | 6 | |
| N24 | VTT_7 | 7 | | VTT_7 | 7 | |
| R23 | VTT_7 | 7 | | VTT_7 | 7 | |
| T23 | VTT_7 | 7 | | VTT_7 | 7 | |
| M12 | VDDAX25_R | - | | VDDAX25_R | - | |
| M23 | VDDAX25_L | - | | VDDAX25_L | - | |
| Y16 | GND | - | | GND | - | |
| Y14 | GND | - | | GND | - | |
| N21 | VCC12 | - | | VCC12 | - | |
| P22 | VCC12 | - | | VCC12 | - | |
| AA22 | VCC12 | - | | VCC12 | - | |
| AB21 | VCC12 | - | | VCC12 | - | |
| AB14 | VCC12 | - | | VCC12 | - | |
| AA13 | VCC12 | - | | VCC12 | - | |
| P13 | VCC12 | - | | VCC12 | - | |
| N14 | VCC12 | - | | VCC12 | - | |
| G26 | NC | - | | NC | - | |
| G9 | NC | - | | NC | - | |
| J12 | NC | - | | NC | - | |
| H12 | NC | - | | NC | - | |
| H23 | NC | - | | NC | - | |
| J23 | NC | - | | NC | - | |

1. Differential pair grouping within a PCI is A (True) and B (complement) and C (True) and D (Complement).
2. The LatticeSC/M40 and LatticeSC/M80 in an 1152-pin package support a 32-bit MPI interface.

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| V8 | PR65D | 3 | PCLKC3_3 |
| U8 | PR65C | 3 | PCLKT3_3 |
| U5 | PR65B | 3 | |
| T5 | PR65A | 3 | |
| V6 | PR64D | 3 | PCLKC3_1 |
| U6 | PR64C | 3 | PCLKT3_1 |
| T4 | PR64B | 3 | PCLKC3_0 |
| T3 | PR64A | 3 | PCLKT3_0 |
| U9 | PR62D | 2 | PCLKC2_2 |
| T9 | PR62C | 2 | PCLKT2_2 |
| R2 | PR62B | 2 | PCLKC2_0 |
| P2 | PR62A | 2 | PCLKT2_0 |
| T11 | PR61D | 2 | PCLKC2_3 |
| U11 | PR61C | 2 | PCLKT2_3 |
| R4 | PR61B | 2 | PCLKC2_1 |
| R3 | PR61A | 2 | PCLKT2_1 |
| T8 | PR60D | 2 | |
| R8 | PR60C | 2 | |
| P1 | PR60B | 2 | |
| N1 | PR60A | 2 | |
| R6 | PR57D | 2 | |
| P6 | PR57C | 2 | |
| M1 | PR57B | 2 | |
| L1 | PR57A | 2 | |
| T10 | PR56D | 2 | |
| U10 | PR56C | 2 | |
| N2 | PR56B | 2 | |
| M2 | PR56A | 2 | |
| R11 | PR51D | 2 | |
| P11 | PR51C | 2 | |
| N4 | PR51B | 2 | |
| M4 | PR51A | 2 | |
| N5 | PR49D | 2 | |
| M5 | PR49C | 2 | |
| L2 | PR49B | 2 | |
| K2 | PR49A | 2 | |
| P8 | PR47D | 2 | |
| N8 | PR47C | 2 | |
| J2 | PR47B | 2 | |
| H2 | PR47A | 2 | |
| M6 | PR45D | 2 | |
| L6 | PR45C | 2 | |
| K3 | PR45B | 2 | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| L5 | PR38B | 2 | |
| K5 | PR38A | 2 | |
| G2 | PR34B | 2 | |
| F2 | PR34A | 2 | |
| F1 | PR30B | 2 | |
| E1 | PR30A | 2 | |
| A2 | GND | - | |
| A33 | GND | - | |
| AA15 | GND | - | |
| AA20 | GND | - | |
| AA32 | GND | - | |
| AA4 | GND | - | |
| AB28 | GND | - | |
| AB6 | GND | - | |
| AC11 | GND | - | |
| AC18 | GND | - | |
| AC25 | GND | - | |
| AD23 | GND | - | |
| AD3 | GND | - | |
| AD31 | GND | - | |
| AE12 | GND | - | |
| AE15 | GND | - | |
| AE29 | GND | - | |
| AE7 | GND | - | |
| AE9 | GND | - | |
| AF20 | GND | - | |
| AF26 | GND | - | |
| AG32 | GND | - | |
| AG4 | GND | - | |
| AH13 | GND | - | |
| AH19 | GND | - | |
| AH25 | GND | - | |
| AH7 | GND | - | |
| AJ10 | GND | - | |
| AJ16 | GND | - | |
| AJ22 | GND | - | |
| AJ28 | GND | - | |
| AK3 | GND | - | |
| AK31 | GND | - | |
| AL11 | GND | - | |
| AL17 | GND | - | |
| AL21 | GND | - | |
| AL27 | GND | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AV32 | PB27B | 5 | | PB29B | 5 | |
| AU36 | PB27C | 5 | | PB29C | 5 | |
| AU37 | PB27D | 5 | | PB29D | 5 | |
| BA35 | PB28A | 5 | | PB30A | 5 | |
| BA34 | PB28B | 5 | | PB30B | 5 | |
| AJ26 | PB28C | 5 | | PB30C | 5 | |
| AJ27 | PB28D | 5 | | PB30D | 5 | |
| AW33 | PB29A | 5 | | PB31A | 5 | |
| AW32 | PB29B | 5 | | PB31B | 5 | |
| AU35 | PB29C | 5 | | PB31C | 5 | |
| AU34 | PB29D | 5 | | PB31D | 5 | |
| BB35 | PB31A | 5 | | PB33A | 5 | |
| BB34 | PB31B | 5 | | PB33B | 5 | |
| AN29 | PB31C | 5 | | PB33C | 5 | |
| AP29 | PB31D | 5 | | PB33D | 5 | |
| AY33 | PB32A | 5 | | PB34A | 5 | |
| AY32 | PB32B | 5 | | PB34B | 5 | |
| AR31 | PB32C | 5 | | PB34C | 5 | |
| AR30 | PB32D | 5 | | PB34D | 5 | |
| AV31 | PB33A | 5 | | PB35A | 5 | |
| AV30 | PB33B | 5 | | PB35B | 5 | |
| AN28 | PB33C | 5 | | PB35C | 5 | |
| AP28 | PB33D | 5 | | PB35D | 5 | |
| BA33 | PB35A | 5 | | PB37A | 5 | |
| BA32 | PB35B | 5 | | PB37B | 5 | |
| AT30 | PB35C | 5 | | PB37C | 5 | |
| AT31 | PB35D | 5 | | PB37D | 5 | |
| BB33 | PB36A | 5 | | PB38A | 5 | |
| BB32 | PB36B | 5 | | PB38B | 5 | |
| AM26 | PB36C | 5 | | PB38C | 5 | |
| AL26 | PB36D | 5 | | PB38D | 5 | |
| AW30 | PB37A | 5 | | PB39A | 5 | |
| AW29 | PB37B | 5 | | PB39B | 5 | |
| AP27 | PB37C | 5 | | PB39C | 5 | |
| AN27 | PB37D | 5 | | PB39D | 5 | |
| BA31 | PB39A | 5 | | PB41A | 5 | |
| BA30 | PB39B | 5 | | PB41B | 5 | |
| AU32 | PB39C | 5 | | PB41C | 5 | |
| AU33 | PB39D | 5 | | PB41D | 5 | |
| BB31 | PB40A | 5 | | PB42A | 5 | |
| BB30 | PB40B | 5 | | PB42B | 5 | |
| AR28 | PB40C | 5 | | PB42C | 5 | |
| AR27 | PB40D | 5 | | PB42D | 5 | |
| AV29 | PB41A | 5 | | PB43A | 5 | |
| AV28 | PB41B | 5 | | PB43B | 5 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AU9 | PB103C | 4 | | PB117C | 4 | |
| AU8 | PB103D | 4 | | PB117D | 4 | |
| AY8 | PB104A | 4 | | PB118A | 4 | |
| AY7 | PB104B | 4 | | PB118B | 4 | |
| AU7 | PB104C | 4 | | PB118C | 4 | |
| AU6 | PB104D | 4 | | PB118D | 4 | |
| BA7 | PB105A | 4 | | PB119A | 4 | |
| BA6 | PB105B | 4 | | PB119B | 4 | |
| AN13 | PB105C | 4 | | PB119C | 4 | |
| AN12 | PB105D | 4 | | PB119D | 4 | |
| AV9 | PB107A | 4 | | PB121A | 4 | |
| AV8 | PB107B | 4 | | PB121B | 4 | |
| AT10 | PB107C | 4 | | PB121C | 4 | |
| AT9 | PB107D | 4 | | PB121D | 4 | |
| AW8 | PB108A | 4 | | PB122A | 4 | |
| AW7 | PB108B | 4 | | PB122B | 4 | |
| AP11 | PB108C | 4 | | PB122C | 4 | |
| AP10 | PB108D | 4 | | PB122D | 4 | |
| BB5 | PB109A | 4 | | PB123A | 4 | |
| BB4 | PB109B | 4 | | PB123B | 4 | |
| AR10 | PB109C | 4 | | PB123C | 4 | |
| AR9 | PB109D | 4 | | PB123D | 4 | |
| BA5 | PB111A | 4 | | PB125A | 4 | |
| BA4 | PB111B | 4 | | PB125B | 4 | |
| AT7 | PB111C | 4 | | PB125C | 4 | |
| AT6 | PB111D | 4 | | PB125D | 4 | |
| BB3 | PB112A | 4 | | PB126A | 4 | |
| BA3 | PB112B | 4 | | PB126B | 4 | |
| AM14 | PB112C | 4 | | PB126C | 4 | |
| AL14 | PB112D | 4 | | PB126D | 4 | |
| AY5 | PB113A | 4 | | PB127A | 4 | |
| AY4 | PB113B | 4 | | PB127B | 4 | |
| AN11 | PB113C | 4 | | PB127C | 4 | |
| AN10 | PB113D | 4 | | PB127D | 4 | |
| AV7 | PB115A | 4 | | PB129A | 4 | |
| AV6 | PB115B | 4 | | PB129B | 4 | |
| AM12 | PB115C | 4 | | PB129C | 4 | |
| AM11 | PB115D | 4 | | PB129D | 4 | |
| AW5 | PB116A | 4 | | PB130A | 4 | |
| AW4 | PB116B | 4 | | PB130B | 4 | |
| AT5 | PB116C | 4 | | PB130C | 4 | |
| AT4 | PB116D | 4 | | PB130D | 4 | |
| AY2 | PB117A | 4 | | PB131A | 4 | |
| BA2 | PB117B | 4 | | PB131B | 4 | |
| AP9 | PB117C | 4 | | PB131C | 4 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| J1 | PR25B | 2 | | PR38B | 2 | |
| K1 | PR25A | 2 | | PR38A | 2 | |
| V12 | PR24D | 2 | | PR34D | 2 | |
| U12 | PR24C | 2 | | PR34C | 2 | |
| K2 | PR24B | 2 | | PR34B | 2 | |
| J2 | PR24A | 2 | | PR34A | 2 | |
| R10 | PR22D | 2 | | PR30D | 2 | |
| T10 | PR22C | 2 | | PR30C | 2 | |
| L5 | PR22B | 2 | | PR30B | 2 | |
| K5 | PR22A | 2 | | PR30A | 2 | |
| P9 | PR21D | 2 | | PR26D | 2 | |
| N9 | PR21C | 2 | | PR26C | 2 | |
| L6 | PR21B | 2 | | PR26B | 2 | |
| K6 | PR21A | 2 | | PR26A | 2 | |
| M8 | PR20D | 2 | | PR19D | 2 | |
| M9 | PR20C | 2 | | PR19C | 2 | |
| H1 | PR20B | 2 | | PR19B | 2 | |
| G1 | PR20A | 2 | | PR19A | 2 | |
| U14 | PR18D | 2 | VREF2_2 | PR18D | 2 | VREF2_2 |
| T14 | PR18C | 2 | | PR18C | 2 | |
| H2 | PR18B | 2 | URC_DLLC_IN_D/URC_DLLC_FB_C | PR18B | 2 | URC_DLLC_IN_D/URC_DLLC_FB_C |
| G2 | PR18A | 2 | URC_DLLT_IN_D/URC_DLLT_FB_C | PR18A | 2 | URC_DLLT_IN_D/URC_DLLT_FB_C |
| P10 | PR17D | 2 | URC_PLLC_IN_B/URC_PLLC_FB_A | PR17D | 2 | URC_PLLC_IN_B/URC_PLLC_FB_A |
| N10 | PR17C | 2 | URC_PLLT_IN_B/URC_PLLT_FB_A | PR17C | 2 | URC_PLLT_IN_B/URC_PLLT_FB_A |
| H3 | PR17B | 2 | URC_DLLC_IN_C/URC_DLLC_FB_D | PR17B | 2 | URC_DLLC_IN_C/URC_DLLC_FB_D |
| G3 | PR17A | 2 | URC_DLLT_IN_C/URC_DLLT_FB_D | PR17A | 2 | URC_DLLT_IN_C/URC_DLLT_FB_D |
| R11 | PR16D | 2 | | PR15D | 2 | |
| P11 | PR16C | 2 | | PR15C | 2 | |
| J5 | PR16B | 2 | URC_PLLC_IN_A/URC_PLLC_FB_B | PR15B | 2 | URC_PLLC_IN_A/URC_PLLC_FB_B |
| J6 | PR16A | 2 | URC_PLLT_IN_A/URC_PLLT_FB_B | PR15A | 2 | URC_PLLT_IN_A/URC_PLLT_FB_B |
| P18 | VCCJ | - | | VCCJ | - | |
| P19 | TDO | - | TDO | TDO | - | TDO |
| R21 | TMS | - | | TMS | - | |
| P20 | TCK | - | | TCK | - | |
| P12 | TDI | - | | TDI | - | |
| P17 | PROGRAMN | 1 | | PROGRAMN | 1 | |
| P21 | MPIIRQN | 1 | CFGIRQN/MPI_IRQ_N | MPIIRQN | 1 | CFGIRQN/MPI_IRQ_N |
| P13 | CCLK | 1 | | CCLK | 1 | |
| H10 | RESP_URC | - | | RESP_URC | - | |
| N13 | VCC12 | - | | VCC12 | - | |
| H9 | A_REFCLKN_R | - | | A_REFCLKN_R | - | |
| G9 | A_REFCLKP_R | - | | A_REFCLKP_R | - | |
| F2 | VCC12 | - | | VCC12 | - | |
| H4 | A_VDDIB0_R | - | | A_VDDIB0_R | - | |
| C1 | A_HDINP0_R | - | PCS 3E0 CH 0 IN P | A_HDINP0_R | - | PCS 3E0 CH 0 IN P |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AC24 | GND | - | | GND | - | |
| AC26 | GND | - | | GND | - | |
| AC35 | GND | - | | GND | - | |
| AC8 | GND | - | | GND | - | |
| AD12 | GND | - | | GND | - | |
| AD16 | GND | - | | GND | - | |
| AD18 | GND | - | | GND | - | |
| AD20 | GND | - | | GND | - | |
| AD23 | GND | - | | GND | - | |
| AD25 | GND | - | | GND | - | |
| AD27 | GND | - | | GND | - | |
| AD31 | GND | - | | GND | - | |
| AE17 | GND | - | | GND | - | |
| AE19 | GND | - | | GND | - | |
| AE24 | GND | - | | GND | - | |
| AE26 | GND | - | | GND | - | |
| AE3 | GND | - | | GND | - | |
| AE39 | GND | - | | GND | - | |
| AF18 | GND | - | | GND | - | |
| AF20 | GND | - | | GND | - | |
| AF23 | GND | - | | GND | - | |
| AF25 | GND | - | | GND | - | |
| AF36 | GND | - | | GND | - | |
| AF7 | GND | - | | GND | - | |
| AG11 | GND | - | | GND | - | |
| AG16 | GND | - | | GND | - | |
| AG19 | GND | - | | GND | - | |
| AG24 | GND | - | | GND | - | |
| AG27 | GND | - | | GND | - | |
| AG32 | GND | - | | GND | - | |
| AH15 | GND | - | | GND | - | |
| AH28 | GND | - | | GND | - | |
| AH4 | GND | - | | GND | - | |
| AH40 | GND | - | | GND | - | |
| AJ35 | GND | - | | GND | - | |
| AJ8 | GND | - | | GND | - | |
| AK12 | GND | - | | GND | - | |
| AK31 | GND | - | | GND | - | |
| AL13 | GND | - | | GND | - | |
| AL19 | GND | - | | GND | - | |
| AL24 | GND | - | | GND | - | |
| AL3 | GND | - | | GND | - | |
| AL30 | GND | - | | GND | - | |
| AL39 | GND | - | | GND | - | |
| AM16 | GND | - | | GND | - | |

**Commercial, Cont.**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA80E-7FC1152C[1] | -7 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-6FC1152C[1] | -6 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-5FC1152C[1] | -5 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-7FF1152C | -7 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-6FF1152C | -6 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-5FF1152C | -5 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-7FC1704C[1] | -7 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSC3GA80E-6FC1704C[1] | -6 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSC3GA80E-5FC1704C[1] | -5 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSC3GA80E-7FF1704C | -7 | Organic fcBGA | 1704 | COM | 80.1 |
| LFSC3GA80E-6FF1704C | -6 | Organic fcBGA | 1704 | COM | 80.1 |
| LFSC3GA80E-5FF1704C | -5 | Organic fcBGA | 1704 | COM | 80.1 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA80EP1-7FC1152C[1] | -7 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-6FC1152C[1] | -6 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-5FC1152C[1] | -5 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-7FF1152C | -7 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-6FF1152C | -6 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-5FF1152C | -5 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-7FC1704C[1] | -7 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSCM3GA80EP1-6FC1704C[1] | -6 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSCM3GA80EP1-5FC1704C[1] | -5 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSCM3GA80EP1-7FF1704C | -7 | Organic fcBGA | 1704 | COM | 80.1 |
| LFSCM3GA80EP1-6FF1704C | -6 | Organic fcBGA | 1704 | COM | 80.1 |
| LFSCM3GA80EP1-5FF1704C | -5 | Organic fcBGA | 1704 | COM | 80.1 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA115E-6FC1152C[1] | -6 | Ceramic fcBGA | 1152 | COM | 115.2 |
| LFSC3GA115E-5FC1152C[1] | -5 | Ceramic fcBGA | 1152 | COM | 115.2 |
| LFSC3GA115E-6FF1152C | -6 | Organic fcBGA | 1152 | COM | 115.2 |
| LFSC3GA115E-5FF1152C | -5 | Organic fcBGA | 1152 | COM | 115.2 |
| LFSC3GA115E-6FC1704C[1] | -6 | Ceramic fcBGA | 1704 | COM | 115.2 |
| LFSC3GA115E-5FC1704C[1] | -5 | Ceramic fcBGA | 1704 | COM | 115.2 |
| LFSC3GA115E-6FF1704C | -6 | Organic fcBGA | 1704 | COM | 115.2 |
| LFSC3GA115E-5FF1704C | -5 | Organic fcBGA | 1704 | COM | 115.2 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

**Commercial, Cont.**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA115EP1-6FCN1152C[1] | -6 | Lead-Free Ceramic fcBGA | 1152 | COM | 115.2 |
| LFSCM3GA115EP1-5FCN1152C[1] | -5 | Lead-Free Ceramic fcBGA | 1152 | COM | 115.2 |
| LFSCM3GA115EP1-6FFN1152C | -6 | Lead-Free Organic fcBGA | 1152 | COM | 115.2 |
| LFSCM3GA115EP1-5FFN1152C | -5 | Lead-Free Organic fcBGA | 1152 | COM | 115.2 |
| LFSCM3GA115EP1-6FCN1704C[1] | -6 | Lead-Free Ceramic fcBGA | 1704 | COM | 115.2 |
| LFSCM3GA115EP1-5FCN1704C[1] | -5 | Lead-Free Ceramic fcBGA | 1704 | COM | 115.2 |
| LFSCM3GA115EP1-6FFN1704C | -6 | Lead-Free Organic fcBGA | 1704 | COM | 115.2 |
| LFSCM3GA115EP1-5FFN1704C | -5 | Lead-Free Organic fcBGA | 1704 | COM | 115.2 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| December 2011 | 02.4 | DC and Switching Characteristics | Updated JTAG Port Timing Specifications table. |