Lattice Semiconductor Corporation - LFSC3GA115E-6FCN1152C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

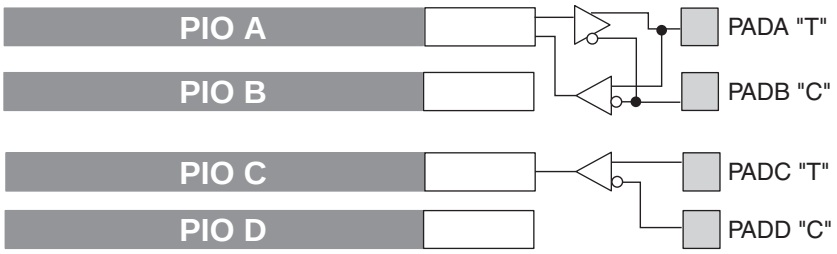
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga115e-6fcn1152c

high-speed interfaces in the LatticeSC devices. Figure 2-18 shows how differential receivers and drivers are arranged between PIOs.

Figure 2-18. Differential Drivers and Receivers



*Differential Driver only available on right and left of the device.

PIO

The PIO contains five blocks: an input register block, output register block, tristate register block, update block, and a control logic block. These blocks contain registers for both single data rate (SDR), double data rate (DDR), and shift register operation along with the necessary clock and selection logic.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 show the diagram of the input register block. The signal from the PURESPEED I/O buffer (DI) enters the input register block and can be used for three purposes, as a source for the combinatorial (INDD) and clock outputs (INCK), the input into the SDR register/latch block and the input to the delay block. The output of the delay block can be used as combinatorial (INDD) and clock (INCK) outputs, an input to the DDR/Shift Register Block or an input into the SDR register block.

Input SDR Register/Latch Block

The SDR register/latch block has a latch and a register/latch that can be used in a variety of combinations to provide a registered or latched output (INFF). The latch operates off high-speed input clocks and latches data on the positive going edge. The register/latch operates off the low-speed input clock and registers/latches data on the positive going edge. Both the latch and the register/latch have a clock enable input that is driven by the input clock enable. In addition both have a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register and latch LSR inputs are driven from LSRI, which is generated from the PIO control MUX. The GSR inputs are driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Input Delay Block

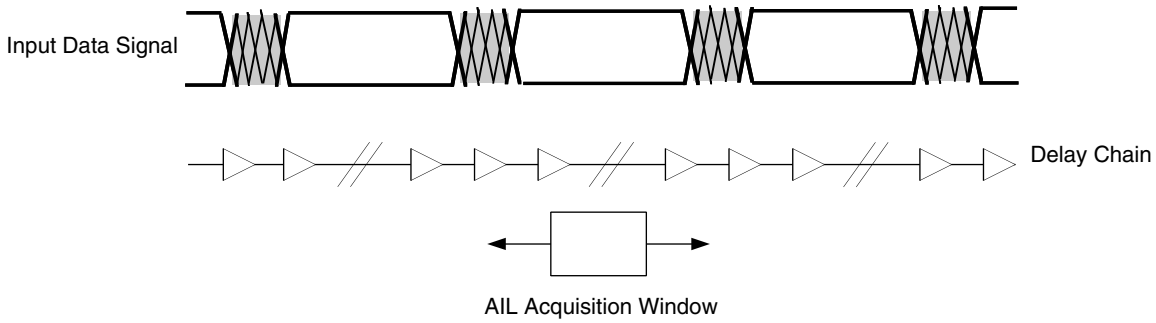
The delay block uses 144 tapped delay lines to obtain coarse and fine delay resolution. These delays can be adjusted during configuration or automatically via DLL or AIL blocks. The Adaptive Input Logic (AIL) uses this delay block to adjust automatically the delay in the data path to ensure that it has sufficient setup and hold time.

The delay line in this block matches the delay line that is used in the 12 on-chip DLLs. The delay line can be set via configuration bits or driven from a calibration bus that allows the setting to be controlled either from one of the on-chip DLLs or user logic. Controlling the delay from one of the on-chip DLLs allow the delay to be calibrated to the DLL clock and hence compensated for the variations in process, voltage and temperature.

Adaptive Input Logic (AIL) Overview

The Adaptive Input Logic (AIL) provides the ability of the input logic to dynamically find a solution by monitoring multiple samples of the input data. The input data signal from the input buffer is run through a delay chain. Data, transitions, jitter, noise are all contained inside of the delay chain. The AIL will then search the delay chain for a clean sampling point for data. Once found the AIL will monitor and walk with the data dynamically. This novel approach of using a delay chain to create multiple copies of the data provides a lower power solution than oversampling data with a higher speed clock. Figure 2-19 provides a high level view of the AIL methodology.

Figure 2-19. LatticeSC AIL Delay of Input Data Waveform



The AIL slides the acquisition window through the delay chain searching for stable data based solely on data transitions. A specific training pattern is not required to perform this bit alignment, simply data transitions. The size of the acquisition window is user-selectable allowing the AIL to operate over the full range of the PURESPEED I/O range. Based on dynamic user control the AIL can either continuously adjust the window location based on data edge detection or it can be locked to a specific delay.

The AIL operates on single data and double data rate interfaces and is available on most FPGA input pins on the LatticeSC device and all buffer types. The AIL block is low power using only 0.003 mW/MHz typical (6 mW @ 2 Gbps) for PRBS 2^7 data. Multiple AIL inputs can be used to create a bus with a FPGA circuit to realign the bus to a common clock cycle. The FPGA circuit to realign the bus is required and is provided by Lattice as a reference design.

For more information on the LatticeSC AIL please refer to TN1158 LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide.

Input DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer to the low-speed clock domain. It functions as a gearbox allowing high-speed incoming data to be passed into the FPGA fabric. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. The PIOs A and C on the left, right and bottom of the device also contain an optional Adaptive Input Logic (AIL) element. This logic automatically aligns incoming data with the clock allowing for easy design of high-speed interfaces. Figure 2-21 shows a simplified block diagram of the shift register block. The shift block in conjunction with the update and clock divider blocks automatically handles the hand off between the low-speed and high-speed clock domains.

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the PURESPEED I/O buffers. The block contains a register for SDR operation and a group of three registers for DDR and shift register operation. The output signal tri-state control signal (TO) can be derived directly from one of the inputs (bypass mode), the SDR shift register, the DDR registers or the data associated with the buffer (for open drain emulation). Figure 2-24 shows the diagram of the Tristate Register Block.

Tristate SDR Register/Latch Block

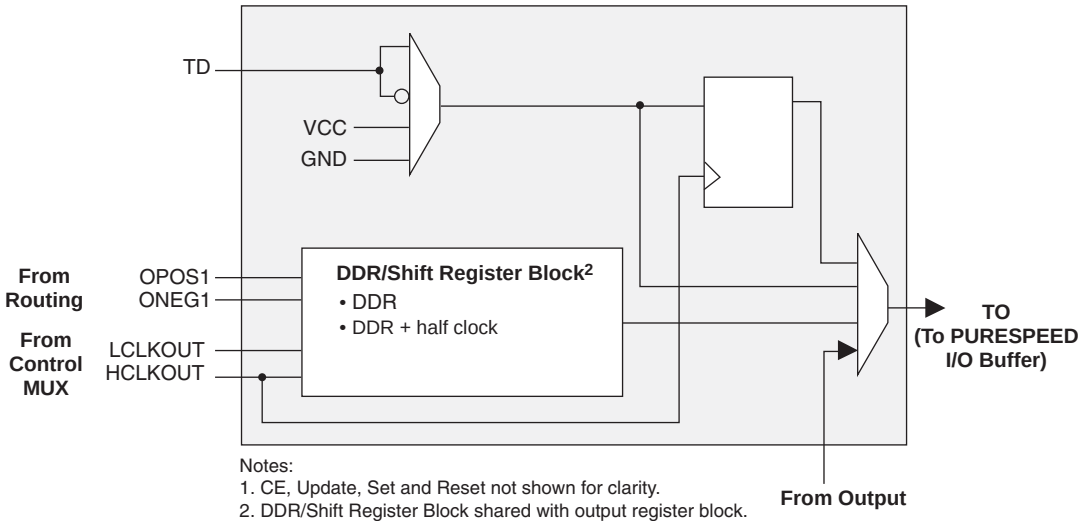
The SDR register operates on the positive edge of the high-speed clock. In it has a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR and Global Set Reset GSR enable or disable. The register LSR input is driven from LSRO, which is generated from the PIO control MUX. The GSR input is driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Tristate DDR/Shift Register Block

The DDR/Shift block is shared with the output block allowing DDR support using the high-speed clock and the associated transfer from the low-speed clock domain. It functions as a gearbox allowing low–speed parallel data from the FPGA fabric to provide a high-speed tri-state control stream.

There is a special mode for DDR-II memory interfaces where the termination is controlled by the output tristate signal. During WRITE cycle when the FPGA is driving the lines, the parallel terminations are turned off. During READ cycle when the FPGA is receiving data, the parallel terminations are turned on.

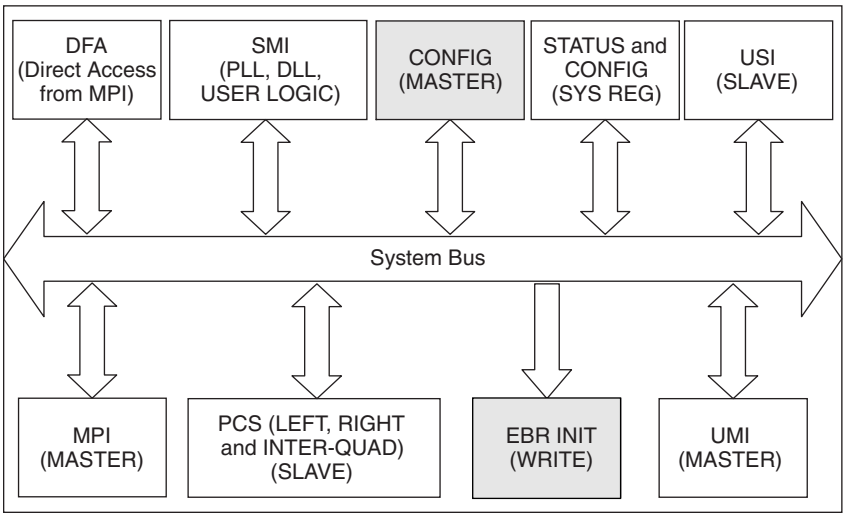
Figure 2-24. Tristate Register Block[1]



I/O Architecture Rules

Table 2-6 shows the PIO usage for x1, x2, x4 gearing. The checkmarks in the columns show the specific PIOs that are used for each gearing mode. When using x2 or x4 gearing, any PIO which is not used for gearing can still be used as an output.

Figure 2-31. LatticeSC System Bus Interfaces



Several interfaces exist between the System Bus and other FPGA elements. The MPI interface acts as a bridge between the external microprocessor bus and System Bus. The MPI may work in an independent clock domain from the System Bus if the System Bus clock is not sourced from the external microprocessor clock. Pipelined operation allows high-speed memory interface to the EBR and peripheral access without the requirement for additional cycles on the bus. Burst transfers allow optimal use of the memory interface by giving advance information of the nature of the transfers.

Details for the majority of the peripherals can be found in the associated technical documentation, see details at the end of this data sheet. Additional details of the MPI are provided below.

Microprocessor Interface (MPI)

The LatticeSC family devices have a dedicated synchronous MPI function block. The MPI is programmable to operate with PowerPC/PowerQUICC MPC860/MPC8260 series microprocessors. The MPI implements an 8-, 16-, or 32-bit interface with 1-bit, 2-bit, or 4-bit parity to the host processor (PowerPC) that can be used for configuration and read-back of the FPGA as well as for user-defined data processing and general monitoring of FPGA functions.

The control portion of the MPI is available following power-up of the FPGA if the mode pins specify MPI mode, even if the FPGA is not yet configured. The width of the data port is selectable among 8-, 16-, or 32-bit and the parity bus can be 1-, 2-, or 4-bit. In configuration mode the data and parity bus width are related to the state of the M[0:3] mode pins. For post-configuration use, the MPI must be included in the configuration bit stream by using an MPI library element in your design from the ispLEVER primitive library, or by setting the bit of the MPI configuration control register prior to the start of configuration. The user can also enable and disable the parity bus through the configuration bit stream. These pads can be used as general I/O when they are not needed for MPI use.

The MPI block also provides the capability to interface directly to the FPGA fabric with a databus after configuration.The bus protocol is still handled by the MPI block but the direct FPGA access allows high-speed block data transfers such as DMA transactions. Figure 2-32 shows one of the ways a PowerPC is connected to MPI.

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
GTLPLUS15	GTLPLUS15	-0.013	-0.017	0.012	0.004	0.037	0.024	ns
GTL12	GTL12	-0.063	-0.071	-0.007	-0.048	0.056	-0.032	ns
Output Adjusters								
LVDS	LVDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
RSDS	RSDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
BLVDS25	BLVDS	-0.129	0.05	-0.136	0.069	-0.136	0.083	ns
MLVDS25	MLVDS	-0.059	0.059	-0.057	0.096	-0.054	0.133	ns
LVPECL33	LVPECL	-0.334	-0.181	-0.325	-1.389	-0.315	-2.598	ns
HSTL18_I	HSTL_18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18_II	HSTL_18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL18D_I	Differential HSTL 18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18D_II	Differential HSTL 18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL15_I	HSTL_15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15_II	HSTL_15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
HSTL15D_I	Differential HSTL 15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15D_II	Differential HSTL 15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
SSTL33_I	SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33_II	SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL33D_I	Differential SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33D_II	Differential SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL25_I	SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25_II	SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL25D_I	Differential SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25D_II	Differential SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL18_I	SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18_II	SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
SSTL18D_I	Differential SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18D_II	Differential SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
LVTTL33_8mA	LVTTL 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVTTL33_16mA	LVTTL 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVTTL33_24mA	LVTTL 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVCMOS33_24mA	LVCMOS 3.3 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	-0.174	0.004	-0.195	0.002	-0.215	0	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	0	0	0	0	0	0	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.094	-0.025	0.107	0.096	0.12	0.216	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive	0.145	-0.054	0.162	0.063	0.181	0.179	ns
LVCMOS25_OD	LVCMOS 2.5 open drain	0.073	-0.125	0.081	-0.081	0.091	-0.09	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	-0.278	-0.099	-0.312	-0.115	-0.345	-0.131	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	-0.073	-0.078	-0.078	-0.084	-0.083	-0.089	ns

sysCLOCK DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		100	—	700	MHz
f_{OUTOP}	Output Clock Frequency (CLKOP)		100	—	700	MHz
f_{OUTOS}	Output Clock Frequency (CLKOS)		25	—	700	MHz
AC Characteristics						
t_{DUTY}	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, 50% duty cycle input clock, duty cycle correction turned off, time reference delay mode)	38	—	62	%
t_{DUTYRD}	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, arbitrary duty cycle input clock, duty cycle correction turned on, time reference delay mode)	45	—	55	%
$t_{DUTYCIR}$	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, arbitrary duty cycle input clock, duty cycle correction turned on, clock injection removal mode)	40	—	60	%
t_{OPJIT}[1]	Output Clock Period Jitter		—	—	200	ps
t_{CPJIT}[1]	Output Clock Cycle-to-Cycle Jitter		—	—	200	ps
t_{SKEW}	Output Clock to Clock Skew (Between Two Outputs with the Same Phase Setting)		—	—	100	ps
t_{LOCK}	DLL Lock-in Time		8	—	18500	cycles
t_{IDUTY}	Input Clock Duty Cycle	Applies to all operating conditions	35	—	65	%
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 250	ps
t_{HI}	Input Clock High Time	At 80% level	500	—	—	ps
t_{LO}	Input Clock Low Time	At 20% level	500	—	—	ps
t_{RSWD}	Reset Signal Pulse Width		3	—	—	ns
t_{FDEL}	Timeshift Delay Step Size		35	45	80	ps
t_{DLL}	Delay Through the DLL when No Delay Taps are Chosen but Not in Bypass Mode.		—	760	—	ps

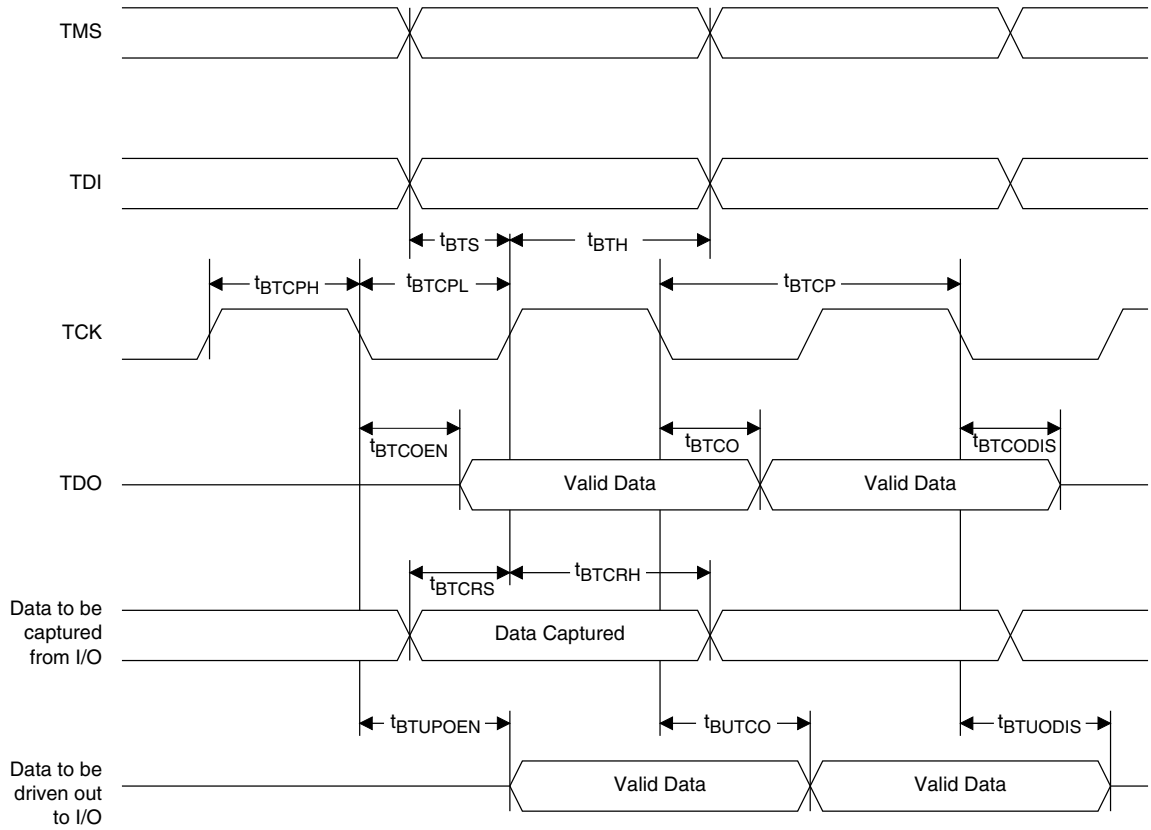
1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps.

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	10	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	10	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	25	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	25	ns

Figure 3-14. JTAG Port Timing Waveforms



Signal Descriptions (Cont.)

Signal Name	I/O	Description
D[n:0]	I/O	In parallel configuration modes, D[7:0] receives configuration data, and each pin is pull-up enabled. For slave serial mode, D0 is the data input. D[7:3] is the output internal status for peripheral mode when RDN is low. D[7:0] is also the first byte of MPI data pins. In MPI configuration mode, MPI selectable data bus width from 8 and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
DP[m:0]	I/O	MPI selectable parity data bus width from 1, 2, and 3-bit DP[0] for D[7:0], DP[1] for D[15:8], and DP[2] for D[23:16].
BUSYN/RCLK/SCK	O	During configuration in peripheral mode, high on BUSYN indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D[7] in asynchronous peripheral mode. During configuration in slave parallel mode, low on BUSYN inhibits the external host from sending new data. The output is used by slave parallel and master serial modes only for decompression. During configuration in master parallel and master byte modes, RCLK is a read clock output signal to an external memory. The RCLK frequency is the same as CCLK when used with uncompressed bitstreams. RCLK will be 1/8 the frequency of CCLK when the bitstream is compressed. During configuration in SPI modes, SCK is generated by the device and connected to the CLK input of the FLASH memory.
MPI Interface (Dedicated pin)		
MPI_IRQ_N	O	MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins.
MPI Interface (User I/O if MPI is not used.)		
MPI_CS0N MPI_CS1	I	MPI chip select pins, active low on MPI_CS0N while active high on MPI_CS1. Both have to be active during the whole transfer data phase. During transfer address phase, both can be inactive so that the decoding for them from address can be slow. If they are active during address phase, one cycle can be saved for sync read.
MPI_CLK	I	This is the PowerPC bus clock. It can be a source of the clock for embedded system bus. If MPI_CLK is used as system bus clock, MPI will be set into sync mode by default. All of the operation on PowerPC side of MPI are synchronized to the rising edge of this clock.
MPI_TSIZ[1:0]	I	Driven by a bus master to indicate the data transfer size for the transaction. 01 for byte, 10 for half-word, and 00 for word.
MPI_WR_N	I	Driven high indicates that a read access is in progress. Driven low indicates that a write access is in process.
MPI_BURST	I	Driven active low indicates that a burst transfer is in progress. Driven high indicates that the current transfer is not a burst.
MPI_BDIP	I	Active low “Burst Data in Process” is driven by a PowerPC processor. Asserted indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.

Pin Information Summary (Cont.)

Pin Type		1152 fcBGA			1704 fcBGA	
		LFSC/M40	LFSC/M80	LFSC/M115	LFSC/M80	LFSC/M115
Single Ended User I/O		604	660	660	904	942
Differential Pair User I/O		302	330	330	452	470
LVDS Output Pairs		78	102	102	114	132
Configuration	Dedicated	11	11	11	11	11
	Muxes/MPI sysBus	72	72	72	72	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		4	4	4	4	4
VCC		44	44	44	76	76
VCC12		52	52	52	88	88
VCCAUX		38	38	38	52	52
VCCIO	Bank 1	10	10	10	10	10
	Bank 2	9	9	9	12	12
	Bank 3	12	12	12	14	14
	Bank 4	12	12	12	14	14
	Bank 5	12	12	12	14	14
	Bank 6	12	12	12	14	14
	Bank 7	9	9	9	12	12
VTT	Bank 2	3	3	3	4	4
	Bank 3	3	3	3	4	4
	Bank 4	3	3	3	5	5
	Bank 5	3	3	3	5	5
	Bank 6	3	3	3	4	4
	Bank 7	3	3	3	4	4
GND		130	130	130	184	184
NC		62	6	6	52	14
Single Ended User / Differential I/O per Bank	Bank 1	80/40	80/40	80/40	80/40	80/40
	Bank 2	60/30	76/38	76/38	96/48	103/51
	Bank 3	96/48	108/54	108/54	132/66	144/72
	Bank 4	106/53	106/53	106/53	184/92	184/92
	Bank 5	106/53	106/53	106/53	184/92	184/92
	Bank 6	96/48	108/54	108/54	132/66	144/72
	Bank 7	60/30	76/38	76/38	96/48	103/51
LVDS Output Pairs Per Bank	Bank 2	15	21	21	24	27
	Bank 3	24	30	30	33	39
	Bank 6	24	30	30	33	39
	Bank 7	15	21	21	24	27
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		108	108	108	212	212
Total		1152	1152	1152	1704	1704

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
C5	A_VDDIB1_L	-	
A5	A_HDINP1_L	-	PCS 360 CH 1 IN P
B5	A_HDINN1_L	-	PCS 360 CH 1 IN N
A4	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B4	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
C4	A_VDDOB1_L	-	
B3	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
C3	A_VDDOB0_L	-	
A3	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
B2	A_HDINN0_L	-	PCS 360 CH 0 IN N
A2	A_HDINP0_L	-	PCS 360 CH 0 IN P
C2	A_VDDIB0_L	-	
A1	GND	-	
A16	GND	-	
B10	GND	-	
C13	GND	-	
D15	GND	-	
D3	GND	-	
E11	GND	-	
F13	GND	-	
G14	GND	-	
G2	GND	-	
G8	GND	-	
H10	GND	-	
J7	GND	-	
K15	GND	-	
K3	GND	-	
K9	GND	-	
M6	GND	-	
N11	GND	-	
N14	GND	-	
N2	GND	-	
P10	GND	-	
P4	GND	-	
R13	GND	-	
R7	GND	-	
G10	VCC	-	
G7	VCC	-	
G9	VCC	-	
H7	VCC	-	
H8	VCC	-	
H9	VCC	-	
J10	VCC	-	
J8	VCC	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C2	VCCJ	-		VCCJ	-	
M9	TDO	-	TDO	TDO	-	TDO
L9	TMS	-		TMS	-	
D1	TCK	-		TCK	-	
C1	TDI	-		TDI	-	
J8	PROGRAMN	1		PROGRAMN	1	
K8	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
B2	CCLK	1		CCLK	1	
H9	RESP_URC	-		RESP_URC	-	
H10	VCC12	-		VCC12	-	
H8	A_REFCLKN_R	-		A_REFCLKN_R	-	
G8	A_REFCLKP_R	-		A_REFCLKP_R	-	
C3	VCC12	-		VCC12	-	
D3	A_VDDIB0_R	-		A_VDDIB0_R	-	
A3	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B3	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E5	VCC12	-		VCC12	-	
A4	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
F6	A_VDDOB0_R	-		A_VDDOB0_R	-	
B4	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
F7	A_VDDOB1_R	-		A_VDDOB1_R	-	
B5	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
E6	VCC12	-		VCC12	-	
A5	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
B6	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
A6	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
C6	VCC12	-		VCC12	-	
D4	A_VDDIB1_R	-		A_VDDIB1_R	-	
C7	VCC12	-		VCC12	-	
D5	A_VDDIB2_R	-		A_VDDIB2_R	-	
A7	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
B7	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
E7	VCC12	-		VCC12	-	
A8	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
F8	A_VDDOB2_R	-		A_VDDOB2_R	-	
B8	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
F9	A_VDDOB3_R	-		A_VDDOB3_R	-	
B9	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
E8	VCC12	-		VCC12	-	
A9	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
B10	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
A10	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
C10	VCC12	-		VCC12	-	
D6	A_VDDIB3_R	-		A_VDDIB3_R	-	
G10	VCC12	-		VCC12	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F15	PT55A	1	D5/MPI_DATA5	PT74A	1	D5/MPI_DATA5
K14	PT54D	1	D4/MPI_DATA4	PT73D	1	D4/MPI_DATA4
K13	PT54C	1	D3/MPI_DATA3	PT73C	1	D3/MPI_DATA3
B15	PT53B	1	D2/MPI_DATA2	PT73B	1	D2/MPI_DATA2
A15	PT53A	1	D1/MPI_DATA1	PT73A	1	D1/MPI_DATA1
J14	PT51D	1	D16/PCLKC1_3/MPI_DATA16	PT71D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT51C	1	D17/PCLKT1_3/MPI_DATA17	PT71C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT51B	1	D0/MPI_DATA0	PT71B	1	D0/MPI_DATA0
B16	PT51A	1	QOUT/CEON	PT71A	1	QOUT/CEON
J13	PT50D	1	VREF2_1	PT70D	1	VREF2_1
H13	PT50C	1	D18/MPI_DATA18	PT70C	1	D18/MPI_DATA18
D15	PT50B	1	DOUT	PT70B	1	DOUT
E15	PT50A	1	MCA_DONE_IN	PT70A	1	MCA_DONE_IN
J16	PT49D	1	D19/PCLKC1_2/MPI_DATA19	PT69D	1	D19/PCLKC1_2/MPI_DATA19
J17	PT49C	1	D20/PCLKT1_2/MPI_DATA20	PT69C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT49B	1	MCA_CLK_P1_OUT	PT69B	1	MCA_CLK_P1_OUT
E16	PT49A	1	MCA_CLK_P1_IN	PT69A	1	MCA_CLK_P1_IN
H15	PT47D	1	D21/PCLKC1_1/MPI_DATA21	PT67D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT47C	1	D22/PCLKT1_1/MPI_DATA22	PT67C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT47B	1	MCA_CLK_P2_OUT	PT67B	1	MCA_CLK_P2_OUT
C16	PT47A	1	MCA_CLK_P2_IN	PT67A	1	MCA_CLK_P2_IN
L17	PT46D	1	MCA_DONE_OUT	PT66D	1	MCA_DONE_OUT
K17	PT46C	1	BUSYN/RCLK/SCK	PT66C	1	BUSYN/RCLK/SCK
E17	PT46B	1	DP0/MPI_PAR0	PT66B	1	DP0/MPI_PAR0
F17	PT46A	1	MPI_TA	PT66A	1	MPI_TA
G17	PT45D	1	D23/MPI_DATA23	PT65D	1	D23/MPI_DATA23
H17	PT45C	1	DP2/MPI_PAR2	PT65C	1	DP2/MPI_PAR2
A17	PT45B	1	PCLKC1_0	PT65B	1	PCLKC1_0
B17	PT45A	1	PCLKT1_0/MPI_CLK	PT65A	1	PCLKT1_0/MPI_CLK
G18	PT43D	1	DP3/PCLKC1_4/MPI_PAR3	PT63D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT43C	1	D24/PCLKT1_4/MPI_DATA24	PT63C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT43B	1	MPI_RETRY	PT63B	1	MPI_RETRY
F18	PT43A	1	A0/MPI_ADDR14	PT63A	1	A0/MPI_ADDR14
J18	PT42D	1	A1/MPI_ADDR15	PT61D	1	A1/MPI_ADDR15
J19	PT42C	1	A2/MPI_ADDR16	PT61C	1	A2/MPI_ADDR16
C20	PT42B	1	A3/MPI_ADDR17	PT61B	1	A3/MPI_ADDR17
C19	PT42A	1	A4/MPI_ADDR18	PT61A	1	A4/MPI_ADDR18
K18	PT41D	1	D25/PCLKC1_5/MPI_DATA25	PT60D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT41C	1	D26/PCLKT1_5/MPI_DATA26	PT60C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT41B	1	A5/MPI_ADDR19	PT60B	1	A5/MPI_ADDR19
E19	PT41A	1	A6/MPI_ADDR20	PT60A	1	A6/MPI_ADDR20
H19	PT39D	1	D27/MPI_DATA27	PT59D	1	D27/MPI_DATA27
H20	PT39C	1	VREF1_1	PT59C	1	VREF1_1
A18	PT39B	1	A7/MPI_ADDR21	PT59B	1	A7/MPI_ADDR21
B18	PT39A	1	A8/MPI_ADDR22	PT59A	1	A8/MPI_ADDR22

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AC19	VTT_5	5		VTT_5	5	
AC20	VTT_5	5		VTT_5	5	
AD22	VTT_5	5		VTT_5	5	
AB24	VTT_6	6		VTT_6	6	
W23	VTT_6	6		VTT_6	6	
Y23	VTT_6	6		VTT_6	6	
N24	VTT_7	7		VTT_7	7	
R23	VTT_7	7		VTT_7	7	
T23	VTT_7	7		VTT_7	7	
M12	VDDAX25_R	-		VDDAX25_R	-	
M23	VDDAX25_L	-		VDDAX25_L	-	
Y16	GND	-		GND	-	
Y14	GND	-		GND	-	
N21	VCC12	-		VCC12	-	
P22	VCC12	-		VCC12	-	
AA22	VCC12	-		VCC12	-	
AB21	VCC12	-		VCC12	-	
AB14	VCC12	-		VCC12	-	
AA13	VCC12	-		VCC12	-	
P13	VCC12	-		VCC12	-	
N14	VCC12	-		VCC12	-	
G26	NC	-		NC	-	
G9	NC	-		NC	-	
J12	NC	-		NC	-	
H12	NC	-		NC	-	
H23	NC	-		NC	-	
J23	NC	-		NC	-	

1. Differential pair grouping within a PCI is A (True) and B (complement) and C (True) and D (Complement).
2. The LatticeSC/M40 and LatticeSC/M80 in an 1152-pin package support a 32-bit MPI interface.

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AJ34	PL98A	6	
AK34	PL98B	6	
AB27	PL98C	6	
AC27	PL98D	6	
AF33	PL99A	6	
AG33	PL99B	6	
AC29	PL99C	6	
AD29	PL99D	6	
AE31	PL103A	6	
AF31	PL103B	6	
AF30	PL103C	6	
AF29	PL103D	6	
AH33	PL104A	6	
AJ33	PL104B	6	
AC28	PL104C	6	
AD28	PL104D	6	
AH32	PL107A	6	
AJ32	PL107B	6	
AD27	PL107C	6	
AE27	PL107D	6	VREF2_6
AG34	PL109A	6	
AH34	PL109B	6	
AC26	PL109C	6	
AB26	PL109D	6	
AK33	PL112A	6	
AL33	PL112B	6	
AG30	PL112C	6	
AH30	PL112D	6	
AL34	PL115A	6	
AM34	PL115B	6	
AJ30	PL115C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL115D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL116A	6	
AH31	PL116B	6	
AD26	PL116C	6	
AD25	PL116D	6	
AL32	PL117A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL117B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL117C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL117D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-	
AF27	TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP27	PB26A	5	
AP26	PB26B	5	
AK25	PB26C	5	
AK24	PB26D	5	
AN25	PB29A	5	
AN24	PB29B	5	
AE22	PB29C	5	
AE21	PB29D	5	
AM26	PB31A	5	
AM25	PB31B	5	
AF22	PB31C	5	
AF21	PB31D	5	
AN23	PB47A	5	
AN22	PB47B	5	
AP23	PB57A	5	
AP22	PB57B	5	
AG21	PB57C	5	
AG20	PB57D	5	
AP25	PB50A	5	PCLKT5_3
AP24	PB50B	5	PCLKC5_3
AD21	PB50C	5	PCLKT5_4
AD20	PB50D	5	PCLKC5_4
AL23	PB51A	5	PCLKT5_5
AL22	PB51B	5	PCLKC5_5
AH24	PB51C	5	
AH23	PB51D	5	
AM23	PB53A	5	PCLKT5_0
AM22	PB53B	5	PCLKC5_0
AJ24	PB53C	5	
AJ23	PB53D	5	VREF2_5
AN21	PB54A	5	PCLKT5_1
AN20	PB54B	5	PCLKC5_1
AE19	PB54C	5	PCLKT5_6
AD19	PB54D	5	PCLKC5_6
AK21	PB55A	5	PCLKT5_2
AK20	PB55B	5	PCLKC5_2
AK23	PB55C	5	PCLKT5_7
AK22	PB55D	5	PCLKC5_7
AL20	PB58A	5	
AL19	PB58B	5	
AG19	PB58C	5	
AF19	PB58D	5	
AP21	PB61A	5	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
L5	PR38B	2	
K5	PR38A	2	
G2	PR34B	2	
F2	PR34A	2	
F1	PR30B	2	
E1	PR30A	2	
A2	GND	-	
A33	GND	-	
AA15	GND	-	
AA20	GND	-	
AA32	GND	-	
AA4	GND	-	
AB28	GND	-	
AB6	GND	-	
AC11	GND	-	
AC18	GND	-	
AC25	GND	-	
AD23	GND	-	
AD3	GND	-	
AD31	GND	-	
AE12	GND	-	
AE15	GND	-	
AE29	GND	-	
AE7	GND	-	
AE9	GND	-	
AF20	GND	-	
AF26	GND	-	
AG32	GND	-	
AG4	GND	-	
AH13	GND	-	
AH19	GND	-	
AH25	GND	-	
AH7	GND	-	
AJ10	GND	-	
AJ16	GND	-	
AJ22	GND	-	
AJ28	GND	-	
AK3	GND	-	
AK31	GND	-	
AL11	GND	-	
AL17	GND	-	
AL21	GND	-	
AL27	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD33	PL59D	6		PL73D	6	
AA38	PL60A	6		PL74A	6	
AB38	PL60B	6		PL74B	6	
AC29	PL60C	6		PL74C	6	
AD29	PL60D	6		PL74D	6	
AA41	PL61A	6		PL75A	6	
AB41	PL61B	6		PL75B	6	
AC34	PL61C	6		PL75C	6	
AD34	PL61D	6		PL75D	6	
AA42	PL63A	6		PL77A	6	
AB42	PL63B	6		PL77B	6	
AC37	PL63C	6		PL77C	6	
AD37	PL63D	6		PL77D	6	
AC38	PL64A	6		PL78A	6	
AD38	PL64B	6		PL78B	6	
AD36	PL64C	6		PL78C	6	
AE36	PL64D	6		PL78D	6	
AC39	PL65A	6		PL79A	6	
AD39	PL65B	6		PL79B	6	
AD35	PL65C	6		PL79C	6	
AE35	PL65D	6		PL79D	6	
AC40	PL67A	6		PL81A	6	
AD40	PL67B	6		PL81B	6	
AE37	PL67C	6		PL81C	6	
AF37	PL67D	6		PL81D	6	
AC41	PL68A	6		PL82A	6	
AD41	PL68B	6		PL82B	6	
AE34	PL68C	6		PL82C	6	
AF34	PL68D	6		PL82D	6	
AC42	PL69A	6		PL83A	6	
AD42	PL69B	6		PL83B	6	
AE33	PL69C	6		PL83C	6	
AF33	PL69D	6		PL83D	6	
AE38	PL72A	6		PL86A	6	
AF38	PL72B	6		PL86B	6	
AE32	PL72C	6		PL86C	6	
AF32	PL72D	6		PL86D	6	
AE41	PL73A	6		PL87A	6	
AF41	PL73B	6		PL87B	6	
AE31	PL73C	6		PL87C	6	
AF31	PL73D	6		PL87D	6	
AE42	PL74A	6		PL88A	6	
AF42	PL74B	6		PL88B	6	
AG37	PL74C	6		PL88C	6	
AH37	PL74D	6		PL88D	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
A26	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N
C34	D_VDDOB2_L	-		D_VDDOB2_L	-	
B26	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P
C32	VCC12	-		VCC12	-	
E27	D_HDINN2_L	-	PCS 363 CH 2 IN N	D_HDINN2_L	-	PCS 363 CH 2 IN N
D27	D_HDINP2_L	-	PCS 363 CH 2 IN P	D_HDINP2_L	-	PCS 363 CH 2 IN P
G25	D_VDDIB2_L	-		D_VDDIB2_L	-	
F29	VCC12	-		VCC12	-	
H26	D_VDDIB1_L	-		D_VDDIB1_L	-	
F30	VCC12	-		VCC12	-	
D28	D_HDINP1_L	-	PCS 363 CH 1 IN P	D_HDINP1_L	-	PCS 363 CH 1 IN P
E28	D_HDINN1_L	-	PCS 363 CH 1 IN N	D_HDINN1_L	-	PCS 363 CH 1 IN N
B27	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P
F36	VCC12	-		VCC12	-	
A27	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N
F35	D_VDDOB1_L	-		D_VDDOB1_L	-	
A28	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N
M30	D_VDDOB0_L	-		D_VDDOB0_L	-	
B28	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P
F37	VCC12	-		VCC12	-	
E29	D_HDINN0_L	-	PCS 363 CH 0 IN N	D_HDINN0_L	-	PCS 363 CH 0 IN N
D29	D_HDINP0_L	-	PCS 363 CH 0 IN P	D_HDINP0_L	-	PCS 363 CH 0 IN P
H27	D_VDDIB0_L	-		D_VDDIB0_L	-	
G28	VCC12	-		VCC12	-	
J28	C_REFCLKP_L	-		C_REFCLKP_L	-	
K28	C_REFCLKN_L	-		C_REFCLKN_L	-	
F32	VCC12	-		VCC12	-	
G29	C_VDDIB3_L	-		C_VDDIB3_L	-	
C31	VCC12	-		VCC12	-	
D30	C_HDINP3_L	-	PCS 362 CH 3 IN P	C_HDINP3_L	-	PCS 362 CH 3 IN P
E30	C_HDINN3_L	-	PCS 362 CH 3 IN N	C_HDINN3_L	-	PCS 362 CH 3 IN N
B29	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P
F38	VCC12	-		VCC12	-	
A29	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N
J33	C_VDDOB3_L	-		C_VDDOB3_L	-	
A30	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N
K33	C_VDDOB2_L	-		C_VDDOB2_L	-	
B30	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P
J34	VCC12	-		VCC12	-	
F31	C_HDINN2_L	-	PCS 362 CH 2 IN N	C_HDINN2_L	-	PCS 362 CH 2 IN N
E31	C_HDINP2_L	-	PCS 362 CH 2 IN P	C_HDINP2_L	-	PCS 362 CH 2 IN P
G30	C_VDDIB2_L	-		C_VDDIB2_L	-	
H28	VCC12	-		VCC12	-	
C37	C_VDDIB1_L	-		C_VDDIB1_L	-	
H30	VCC12	-		VCC12	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB25	VCC	-		VCC	-	
AB26	VCC	-		VCC	-	
AC16	VCC	-		VCC	-	
AC18	VCC	-		VCC	-	
AC20	VCC	-		VCC	-	
AC23	VCC	-		VCC	-	
AC25	VCC	-		VCC	-	
AC27	VCC	-		VCC	-	
AD17	VCC	-		VCC	-	
AD19	VCC	-		VCC	-	
AD21	VCC	-		VCC	-	
AD22	VCC	-		VCC	-	
AD24	VCC	-		VCC	-	
AD26	VCC	-		VCC	-	
AE16	VCC	-		VCC	-	
AE18	VCC	-		VCC	-	
AE20	VCC	-		VCC	-	
AE21	VCC	-		VCC	-	
AE22	VCC	-		VCC	-	
AE23	VCC	-		VCC	-	
AE25	VCC	-		VCC	-	
AE27	VCC	-		VCC	-	
AF17	VCC	-		VCC	-	
AF19	VCC	-		VCC	-	
AF21	VCC	-		VCC	-	
AF22	VCC	-		VCC	-	
AF24	VCC	-		VCC	-	
AF26	VCC	-		VCC	-	
AG18	VCC	-		VCC	-	
AG20	VCC	-		VCC	-	
AG23	VCC	-		VCC	-	
AG25	VCC	-		VCC	-	
T18	VCC	-		VCC	-	
T20	VCC	-		VCC	-	
T23	VCC	-		VCC	-	
T25	VCC	-		VCC	-	
U17	VCC	-		VCC	-	
U19	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
U22	VCC	-		VCC	-	
U24	VCC	-		VCC	-	
U26	VCC	-		VCC	-	
V16	VCC	-		VCC	-	
V18	VCC	-		VCC	-	
V20	VCC	-		VCC	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FC1152C[1]	-7	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FC1152C[1]	-6	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FC1152C[1]	-5	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FC1704C[1]	-7	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FC1704C[1]	-6	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FC1704C[1]	-5	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FC1152C[1]	-7	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FC1152C[1]	-6	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FC1152C[1]	-5	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FC1704C[1]	-7	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FC1704C[1]	-6	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FC1704C[1]	-5	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152C[1]	-6	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FC1152C[1]	-5	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FC1704C[1]	-6	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FC1704C[1]	-5	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.