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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga115e-6fcn1152i

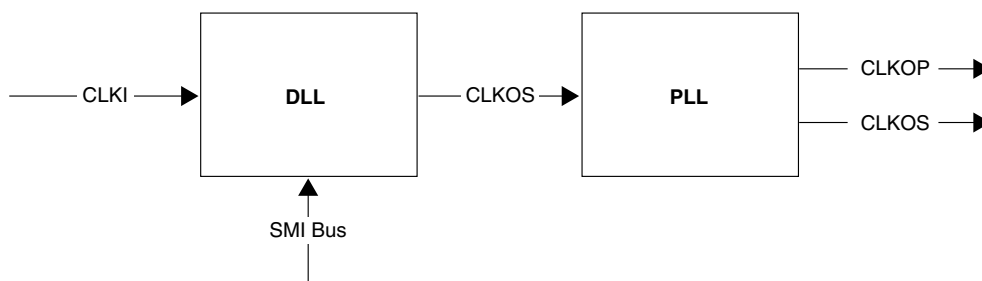
Figure 2-13. DLL to PLL

Figure 2-14 shows a shift of only CLKOP out in time.

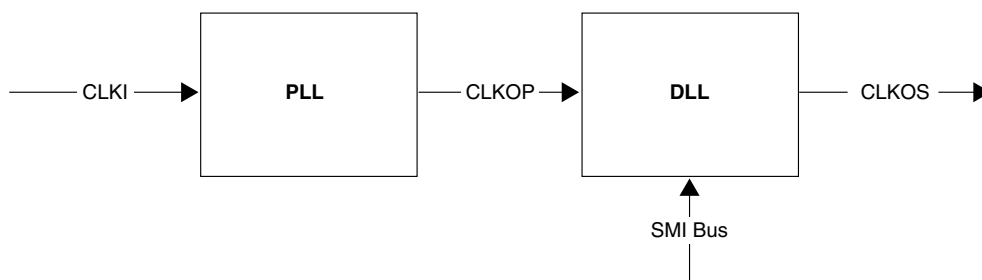
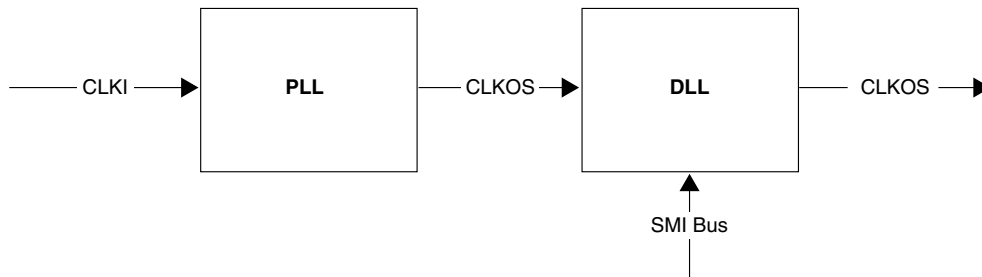
Figure 2-14. PLL to DLL

Figure 2-15 shows a shift of only CLKOS out in time.

Figure 2-15. PLL to DLL

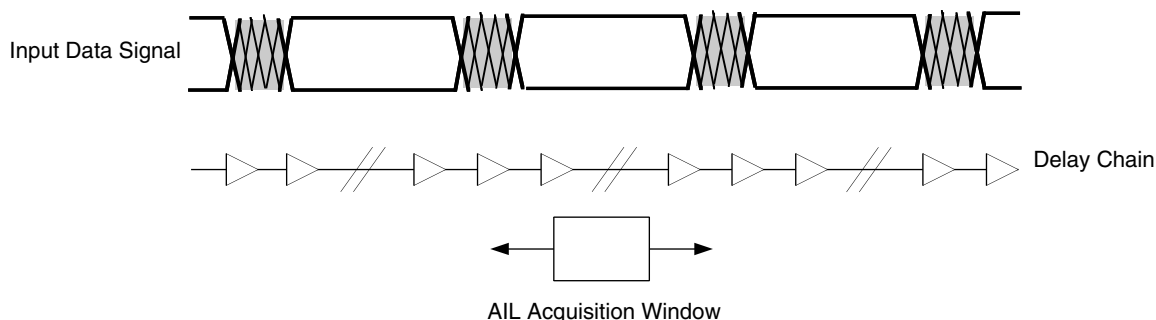
For further information on the DLL, please see details of additional technical documentation at the end of this data sheet.

sysMEM Memory Block

The sysMEM block can implement single port, true dual port, pseudo dual port or FIFO memories. Dedicated FIFO support logic allows the LatticeSC devices to efficiently implement FIFOs without consuming LUTs or routing resources for flag generation. Each block can be used in a variety of depths and widths as shown in Table 2-5. Memory with ranges from x1 to x18 in all modes: single port, pseudo-dual port and FIFO also providing x36.

Adaptive Input Logic (AIL) Overview

The Adaptive Input Logic (AIL) provides the ability of the input logic to dynamically find a solution by monitoring multiple samples of the input data. The input data signal from the input buffer is run through a delay chain. Data, transitions, jitter, noise are all contained inside of the delay chain. The AIL will then search the delay chain for a clean sampling point for data. Once found the AIL will monitor and walk with the data dynamically. This novel approach of using a delay chain to create multiple copies of the data provides a lower power solution than oversampling data with a higher speed clock. Figure 2-19 provides a high level view of the AIL methodology.

Figure 2-19. LatticeSC AIL Delay of Input Data Waveform

The AIL slides the acquisition window through the delay chain searching for stable data based solely on data transitions. A specific training pattern is not required to perform this bit alignment, simply data transitions. The size of the acquisition window is user-selectable allowing the AIL to operate over the full range of the PURESPEED I/O range. Based on dynamic user control the AIL can either continuously adjust the window location based on data edge detection or it can be locked to a specific delay.

The AIL operates on single data and double data rate interfaces and is available on most FPGA input pins on the LatticeSC device and all buffer types. The AIL block is low power using only 0.003 mW/MHz typical (6 mW @ 2 Gbps) for PRBS 2^7 data. Multiple AIL inputs can be used to create a bus with a FPGA circuit to realign the bus to a common clock cycle. The FPGA circuit to realign the bus is required and is provided by Lattice as a reference design.

For more information on the LatticeSC AIL please refer to TN1158 [LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide](#).

Input DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer to the low-speed clock domain. It functions as a gearbox allowing high-speed incoming data to be passed into the FPGA fabric. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. The PIOs A and C on the left, right and bottom of the device also contain an optional Adaptive Input Logic (AIL) element. This logic automatically aligns incoming data with the clock allowing for easy design of high-speed interfaces. Figure 2-21 shows a simplified block diagram of the shift register block. The shift block in conjunction with the update and clock divider blocks automatically handles the hand off between the low-speed and high-speed clock domains.

VDDAX25 needs to be connected independent of the use of the SERDES. This supply is used to control the SERDES CML I/O regardless of the SERDES being used in the design.

Supported Source Synchronous Interfaces

The LatticeSC devices contain a variety of hardware, such as delay elements, DDR registers and PLLs, to simplify the implementation of Source Synchronous interfaces. Table 2-11 lists Source Synchronous and DDR/QDR standards supported in the LatticeSC. For additional detail refer to technical information at the end of the data sheet.

Table 2-11. Source Synchronous Standards Table¹

Source Synchronous Standard	Clocking	Speeds (MHz)	Data Rate (Mbps)
RapidIO	DDR	500	1000
SPI4.2 (POS-PHY4)/NPSI	DDR	500	1000
SFI4/XSBI	DDR SDR	334 667	667
XGMII	DDR	156.25	312
CSIX	SDR	250	250
QDRII/QDRII+ memory interface	DDR	300	600
DDR memory interface	DDR	240	480
DDRII memory interface	DDR	333	667
RLDRAM memory interface	DDR	400	800

1. Memory width is dependent on the system design and limited by the number of I/Os in the device.

flexiPCS™ (Physical Coding Sublayer Block)

flexiPCS Functionality

The LatticeSC family combines a high-performance FPGA fabric, high-performance I/Os and large embedded RAM in a single industry leading architecture. LatticeSC devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES for high-speed, full-duplex serial data transfers at data rates up to 3.8 Gbps. The PCS logic in each channel can be configured to support an array of popular data protocols including SONET (STS-12/STS-12c, STS-48/STS-48c, and TFI-5 support of 10 Gbps or above), Gigabit Ethernet (compliant to the IEEE 100BASE-X specification), 1.02 or 2.04 Gbps Fibre Channel, PCI-Express, and Serial RapidIO. In addition, the protocol based logic can be fully or partially bypassed in a number of configurations to allow users flexibility in designing their own high-speed data interface.

Protocols requiring data rates above 3.8 Gbps can be accommodated by dedicating either one pair or all four channels in one flexiPCS quad block to one data link. One quad can support full-duplex serial data transfers at data rates up to 15.2 Gbps. A single flexiPCS quad can be configured to support 10Gb Ethernet (with a fully compliant XAUI interface), 10Gb Fibre Channel, and x4 PCI-Express and 4x RapidIO.

The flexiPCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic which can also be geared to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Each SERDES pin can be DC coupled independently and can allow for both high-speed and low-speed operation down to DC rates on the same SERDES pin, as required by some Serial Digital Video applications.

The ispLEVER design tools from Lattice support all modes of the flexiPCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow a user to define their own operation. With ispLEVER, the user can define the mode for each quad in a design. Nine modes are currently supported by the ispLEVER design flow:

Absolute Maximum Ratings

Supply Voltage V_{CC} , V_{CC12} , V_{DDIB} , V_{DDOB}	-0.5 to 1.6V
Supply Voltage V_{CCAUX} , V_{DDAX25} , V_{TT}	-0.5 to 2.75V
Supply Voltage V_{CCJ}	-0.5 to 3.6V
Supply Voltage V_{CCIO} (Banks 1, 4, 5)	-0.5 to 3.6V
Supply Voltage V_{CCIO} (Banks 2, 3, 6, 7)	-0.5 to 2.75V
Input or I/O Tristate Voltage Applied (Banks 1, 4, 5)	-0.5 to 3.6V
Input or I/O Tristate Voltage Applied (Banks 2, 3, 6, 7)	-0.5 to 2.75V
Storage Temperature (Ambient)	-65 to 150°C
Junction Temperature Under Bias (Tj)	+125°C

Notes:

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot and overshoot of -2V to (VIHMAX +2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}^5	Core Supply Voltage (Nominal 1.2V Operation)	0.95	1.26	V
V_{CCAUX}^6	Programmable I/O Auxiliary Supply Voltage	2.375	2.625	V
$V_{CCIO}^{1,2,5,6}$	Programmable I/O Driver Supply Voltage (Banks 1, 4, 5)	1.14	3.45	V
$V_{CCIO}^{1,2,5,6}$	Programmable I/O Driver Supply Voltage (Banks 2, 3, 6, 7)	1.14	2.625	V
$V_{CC12}^{4,5}$	Internal 1.2V Power Supply Voltage for Configuration Logic and FPGA PLL, SERDES PLL Power Supply Voltage and SERDES Analog Supply Voltage	1.14	1.26	V
V_{DDIB}	SERDES Input Buffer Supply Voltage	1.14	1.575	V
V_{DDOB}	SERDES Output Buffer Supply Voltage	1.14	1.575	V
V_{DDAX25}	SERDES Termination Auxiliary Supply Voltage	2.375	2.625	V
$V_{CCJ}^{1,5}$	Supply Voltage for IEEE 1149.1 Test Access Port	1.71	3.45	V
$V_{TT}^{2,3}$	Programmable I/O Termination Power Supply	0.5	$V_{CCAUX} - 0.5$	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	+85	C
t_{JIND}	Junction Temperature, Industrial Operation	-40	105	C

1. If V_{CCIO} or V_{CCJ} is set to 2.5V, they must be connected to the same power supply as V_{CCAUX} .
2. See recommended voltages by I/O standard in subsequent table.
3. When V_{TT} termination is not required, or used to provide the common mode termination voltage (V_{CMT}), these pins can be left unconnected on the device.
4. V_{CC12} cannot be lower than V_{CC} at any time. For 1.2V operation, it is recommended that the V_{CC} and V_{CC12} supplies be tied together with proper noise decoupling between the digital VCC and analog VCC12 supplies.
5. V_{CC} , V_{CCIO} (all banks), V_{CC12} and V_{CCJ} must reach their minimum values before configuration will proceed.
6. If V_{CCIO} for a bank is nominally 1.2V/1.5V/1.8V, then V_{CCAUX} must always be higher than V_{CCIO} during power up.

LatticeSC/M Family Timing Adders

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Input Adjusters								
LVDS	LVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
RSDS	RSDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
BLVDS25	BLVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
MLVDS25	MLVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
LVPECL33	LVPECL	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
HSTL18_I	HSTL_18 class I	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL18_II	HSTL_18 class II	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL18_III	HSTL_18 class III	-0.016	-0.018	0.008	0.003	0.032	0.023	ns
HSTL18_IV	HSTL_18 class IV	-0.016	-0.018	0.008	0.003	0.032	0.023	ns
HSTL18D_I	Differential HSTL 18 class I	0.006	0.001	0.029	0.024	0.052	0.046	ns
HSTL18D_II	Differential HSTL 18 class II	0.006	0.001	0.029	0.024	0.052	0.046	ns
HSTL15_I	HSTL_15 class I	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
HSTL15_II	HSTL_15 class II	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
HSTL15_III	HSTL_15 class III	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL15_IV	HSTL_15 class IV	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL15D_I	Differential HSTL 15 class I	-0.021	-0.022	0.001	-0.009	0.022	0.003	ns
HSTL15D_II	Differential HSTL 15 class II	-0.021	-0.022	0.001	-0.009	0.022	0.003	ns
SSTL33_I	SSTL_3 class I	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns
SSTL33_II	SSTL_3 class II	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns
SSTL33D_I	Differential SSTL_3 class I	0.012	0.012	0.034	0.028	0.055	0.043	ns
SSTL33D_II	Differential SSTL_3 class II	0.012	0.012	0.034	0.028	0.055	0.043	ns
SSTL25_I	SSTL_2 class I	0.003	-0.008	0.03	0.011	0.058	0.03	ns
SSTL25_II	SSTL_2 class II	0.003	-0.008	0.03	0.011	0.058	0.03	ns
SSTL25D_I	Differential SSTL_2 class I	0.006	0	0.031	0.023	0.056	0.046	ns
SSTL25D_II	Differential SSTL_2 class II	0.006	0	0.031	0.023	0.056	0.046	ns
SSTL18_I	SSTL_18 class I	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
SSTL18_II	SSTL_18 class II	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
SSTL18D_I	Differential SSTL_18 class I	0.006	0.001	0.029	0.024	0.052	0.046	ns
SSTL18D_II	Differential SSTL_18 class II	0.006	0.001	0.029	0.024	0.052	0.046	ns
LVTTTL33	LVTTTL	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
LVC MOS33	LVC MOS 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
LVC MOS25	LVC MOS 2.5	0	0	0	0	0	0	ns
LVC MOS18	LVC MOS 1.8	-0.068	-0.068	-0.087	-0.087	-0.105	-0.105	ns
LVC MOS15	LVC MOS 1.5	-0.131	-0.131	-0.186	-0.186	-0.241	-0.241	ns
LVC MOS12	LVC MOS 1.2	-0.238	-0.238	-0.364	-0.364	-0.49	-0.49	ns
PCI33	PCI	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
PCIX33	PCI-X 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
PCIX15	PCI-X 1.5	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
AGP1X33	AGP-1X 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
AGP2X33	AGP-2X	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns

Signal Descriptions (Cont.)

Signal Name	I/O	Description
D[n:0]	I/O	In parallel configuration modes, D[7:0] receives configuration data, and each pin is pull-up enabled. For slave serial mode, D0 is the data input. D[7:3] is the output internal status for peripheral mode when RDN is low. D[7:0] is also the first byte of MPI data pins. In MPI configuration mode, MPI selectable data bus width from 8 and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
DP[m:0]	I/O	MPI selectable parity data bus width from 1, 2, and 3-bit DP[0] for D[7:0], DP[1] for D[15:8], and DP[2] for D[23:16].
BUSYN/RCLK/SCK	O	During configuration in peripheral mode, high on BUSYN indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D[7] in asynchronous peripheral mode. During configuration in slave parallel mode, low on BUSYN inhibits the external host from sending new data. The output is used by slave parallel and master serial modes only for decompression. During configuration in master parallel and master byte modes, RCLK is a read clock output signal to an external memory. The RCLK frequency is the same as CCLK when used with uncompressed bit-streams. RCLK will be 1/8 the frequency of CCLK when the bitstream is compressed. During configuration in SPI modes, SCK is generated by the device and connected to the CLK input of the FLASH memory.
MPI Interface (Dedicated pin)		
MPI_IRQ_N	O	MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins.
MPI Interface (User I/O if MPI is not used.)		
MPI_CS0N MPI_CS1	I	MPI chip select pins, active low on MPI_CS0N while active high on MPI_CS1. Both have to be active during the whole transfer data phase. During transfer address phase, both can be inactive so that the decoding for them from address can be slow. If they are active during address phase, one cycle can be saved for sync read.
MPI_CLK	I	This is the PowerPC bus clock. It can be a source of the clock for embedded system bus. If MPI_CLK is used as system bus clock, MPI will be set into sync mode by default. All of the operation on PowerPC side of MPI are synchronized to the rising edge of this clock.
MPI_TSIZE[1:0]	I	Driven by a bus master to indicate the data transfer size for the transaction. 01 for byte, 10 for half-word, and 00 for word.
MPI_WR_N	I	Driven high indicates that a read access is in progress. Driven low indicates that a write access is in process.
MPI_BURST	I	Driven active low indicates that a burst transfer is in progress. Driven high indicates that the current transfer is not a burst.
MPI_BDIP	I	Active low "Burst Data in Process" is driven by a PowerPC processor. Asserted indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
RESP_[ULC/URC]	—	Calibration resistor to be placed between this pin and either ground or RESPN_[ULC/URC]. RESPN_[ULC/URC] is available on select packages. If available, connection of calibration resistor between RESP_[ULC/URC] and RESPN_[ULC/URC] takes precedence over connection of calibration resistor between RESP_[ULC/URC] and ground. Note: only one per side of the device. Value: 4.02K ohm +/- 1% ohm.
RESPN_[ULC/URC]	—	Available on selected packages. If available, calibration resistor should be placed between RESP_[ULC/URC] and RESPN_[ULC/URC] instead of between RESP_[ULC/URC] and ground. Note: only one per side of the device. Value: 4.02K ohm +/- 1% ohm.
[A:D]_VDDIBx_[L/R]	—	Input buffer power supply for channel x (1.2V/1.5V) on left [L] or right [R] side of device.
[A:D]_VDDOBx_[L/R]	—	Output buffer power supply for channel x (1.2V/1.5V) on left [L] or right [R] side of device.
[A:D]_VDDAX25_[L/R]	—	Auxiliary power for input and output termination (2.5V) on left [L] or right [R] side of device.

1. The ispLEVER software tools may specify VDDR_x, VDDT_x, VDDP and VCCL pins. These pins should be considered VCC12 pins.
Note: Signals listed as Signal A / Signal B define the same physical pin that is used for different functions based on configuration mode.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AK14	PB25A	5		PB35A	5	
AK15	PB25B	5		PB35B	5	
AK16	PB27A	4		PB37A	4	
AK17	PB27B	4		PB37B	4	
AJ16	PB28A	4		PB38A	4	
AJ17	PB28B	4		PB38B	4	
AE16	PB28C	4		PB38C	4	
AH16	PB29A	4		PB39A	4	
AG16	PB29B	4		PB39B	4	
AK18	PB31A	4		PB41A	4	
AK19	PB31B	4		PB41B	4	
AH17	PB32A	4		PB42A	4	
AH18	PB32B	4		PB42B	4	
AG17	PB32D	4		PB42D	4	
AJ18	PB33A	4		PB43A	4	
AJ19	PB33B	4		PB43B	4	
AK20	PB35A	4	PCLKT4_2	PB46A	4	PCLKT4_2
AK21	PB35B	4	PCLKC4_2	PB46B	4	PCLKC4_2
AF18	PB36A	4	PCLKT4_1	PB47A	4	PCLKT4_1
AG18	PB36B	4	PCLKC4_1	PB47B	4	PCLKC4_1
AJ20	PB37A	4	PCLKT4_0	PB49A	4	PCLKT4_0
AJ21	PB37B	4	PCLKC4_0	PB49B	4	PCLKC4_0
AG19	PB37C	4	VREF2_4	PB49C	4	VREF2_4
AK22	PB39A	4	PCLKT4_5	PB51A	4	PCLKT4_5
AK23	PB39B	4	PCLKC4_5	PB51B	4	PCLKC4_5
AH19	PB39C	4		PB51C	4	
AK24	PB40A	4	PCLKT4_3	PB52A	4	PCLKT4_3
AK25	PB40B	4	PCLKC4_3	PB52B	4	PCLKC4_3
AE19	PB40C	4	PCLKT4_4	PB52C	4	PCLKT4_4
AE20	PB40D	4	PCLKC4_4	PB52D	4	PCLKC4_4
AE21	PB41A	4		PB53A	4	
AF21	PB41B	4		PB53B	4	
AG21	PB43A	4		PB55A	4	
AG22	PB43B	4		PB55B	4	
AH22	PB44A	4		PB56A	4	
AH23	PB44B	4		PB56B	4	
AH21	PB44C	4		PB56C	4	
AK28	PB45A	4		PB60A	4	
AK29	PB45B	4		PB60B	4	
AE22	PB45C	4		PB60C	4	
AJ28	PB47A	4		PB67A	4	
AH28	PB47B	4		PB67B	4	
AE24	PB47C	4	VREF1_4	PB67C	4	VREF1_4
AE25	PB47D	4		PB67D	4	
AJ29	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G1	NC	-		PL20B	7	
M4	NC	-		NC	-	
J3	NC	-		NC	-	
P5	NC	-		NC	-	
W5	NC	-		PL48C	6	
T6	NC	-		PL35C	6	
U3	NC	-		PL36A	6	
V3	NC	-		PL36B	6	
T5	NC	-		PL39A	6	
T4	NC	-		PL39B	6	
V5	NC	-		PL43C	6	
U6	NC	-		PL42C	6	
U4	NC	-		PL40A	6	
U5	NC	-		PL40B	6	
V4	NC	-		PL43D	6	
Y2	NC	-		PL47A	6	
AA2	NC	-		PL47B	6	
W3	NC	-		PL47D	6	
Y3	NC	-		PL47C	6	
AB3	NC	-		NC	-	
AC4	NC	-		PL53A	6	
AD4	NC	-		PL53B	6	
AE3	NC	-		PL56A	6	
AF3	NC	-		PL56B	6	
AF7	NC	-		PB7A	5	
AF6	NC	-		PB7B	5	
AH4	NC	-		PB8A	5	
AG5	NC	-		PB8B	5	
AF8	NC	-		PB9A	5	
AG8	NC	-		PB9B	5	
AG7	NC	-		NC	-	
AG10	NC	-		NC	-	
AF12	NC	-		NC	-	
AH7	NC	-		PB15A	5	
AE13	NC	-		PB15D	5	
AG13	NC	-		PB23C	5	
AH8	NC	-		PB15B	5	
AJ5	NC	-		PB17A	5	
AJ6	NC	-		PB17B	5	
AF15	NC	-		PB21D	5	
AJ7	NC	-		PB19A	5	
AJ8	NC	-		PB19B	5	
AE12	NC	-		PB15C	5	
AF16	NC	-		PB38D	4	
AF19	NC	-		PB49D	4	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W24	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC18	VCCAUX	-		VCCAUX	-	
AC19	VCCAUX	-		VCCAUX	-	
AD17	VCCAUX	-		VCCAUX	-	
AD18	VCCAUX	-		VCCAUX	-	
AD19	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
AC14	VCCAUX	-		VCCAUX	-	
AD12	VCCAUX	-		VCCAUX	-	
AD13	VCCAUX	-		VCCAUX	-	
AD14	VCCAUX	-		VCCAUX	-	
U7	VCCAUX	-		VCCAUX	-	
U8	VCCAUX	-		VCCAUX	-	
V7	VCCAUX	-		VCCAUX	-	
V8	VCCAUX	-		VCCAUX	-	
W7	VCCAUX	-		VCCAUX	-	
W8	VCCAUX	-		VCCAUX	-	
M7	VCCAUX	-		VCCAUX	-	
M8	VCCAUX	-		VCCAUX	-	
N7	VCCAUX	-		VCCAUX	-	
N8	VCCAUX	-		VCCAUX	-	
H10	VCCIO1	-		VCCIO1	-	
H21	VCCIO1	-		VCCIO1	-	
H22	VCCIO1	-		VCCIO1	-	
H9	VCCIO1	-		VCCIO1	-	
J11	VCCIO1	-		VCCIO1	-	
J12	VCCIO1	-		VCCIO1	-	
J13	VCCIO1	-		VCCIO1	-	
J14	VCCIO1	-		VCCIO1	-	
J15	VCCIO1	-		VCCIO1	-	
J16	VCCIO1	-		VCCIO1	-	
J17	VCCIO1	-		VCCIO1	-	
J18	VCCIO1	-		VCCIO1	-	
J19	VCCIO1	-		VCCIO1	-	
J20	VCCIO1	-		VCCIO1	-	
J23	VCCIO2	-		VCCIO2	-	
J24	VCCIO2	-		VCCIO2	-	
K23	VCCIO2	-		VCCIO2	-	
K24	VCCIO2	-		VCCIO2	-	
L22	VCCIO2	-		VCCIO2	-	
L23	VCCIO2	-		VCCIO2	-	
M22	VCCIO2	-		VCCIO2	-	
N22	VCCIO2	-		VCCIO2	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P22	VCCIO2	-		VCCIO2	-	
R22	VCCIO2	-		VCCIO2	-	
AA23	VCCIO3	-		VCCIO3	-	
AA24	VCCIO3	-		VCCIO3	-	
AB23	VCCIO3	-		VCCIO3	-	
AB24	VCCIO3	-		VCCIO3	-	
T22	VCCIO3	-		VCCIO3	-	
U22	VCCIO3	-		VCCIO3	-	
V22	VCCIO3	-		VCCIO3	-	
W22	VCCIO3	-		VCCIO3	-	
Y22	VCCIO3	-		VCCIO3	-	
Y23	VCCIO3	-		VCCIO3	-	
Y24	VCCIO3	-		VCCIO3	-	
AB16	VCCIO4	-		VCCIO4	-	
AB17	VCCIO4	-		VCCIO4	-	
AB18	VCCIO4	-		VCCIO4	-	
AB19	VCCIO4	-		VCCIO4	-	
AB20	VCCIO4	-		VCCIO4	-	
AC20	VCCIO4	-		VCCIO4	-	
AC21	VCCIO4	-		VCCIO4	-	
AC22	VCCIO4	-		VCCIO4	-	
AD20	VCCIO4	-		VCCIO4	-	
AD21	VCCIO4	-		VCCIO4	-	
AD22	VCCIO4	-		VCCIO4	-	
AB11	VCCIO5	-		VCCIO5	-	
AB12	VCCIO5	-		VCCIO5	-	
AB13	VCCIO5	-		VCCIO5	-	
AB14	VCCIO5	-		VCCIO5	-	
AB15	VCCIO5	-		VCCIO5	-	
AC10	VCCIO5	-		VCCIO5	-	
AC11	VCCIO5	-		VCCIO5	-	
AC9	VCCIO5	-		VCCIO5	-	
AD10	VCCIO5	-		VCCIO5	-	
AD11	VCCIO5	-		VCCIO5	-	
AD9	VCCIO5	-		VCCIO5	-	
AA7	VCCIO6	-		VCCIO6	-	
AA8	VCCIO6	-		VCCIO6	-	
AB7	VCCIO6	-		VCCIO6	-	
AB8	VCCIO6	-		VCCIO6	-	
T9	VCCIO6	-		VCCIO6	-	
U9	VCCIO6	-		VCCIO6	-	
V9	VCCIO6	-		VCCIO6	-	
W9	VCCIO6	-		VCCIO6	-	
Y7	VCCIO6	-		VCCIO6	-	
Y8	VCCIO6	-		VCCIO6	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2}

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C28	A_REFCLKP_L	-		A_REFCLKP_L	-	
D28	A_REFCLKN_L	-		A_REFCLKN_L	-	
B28	VCC12	-		VCC12	-	
F28	RESP_ULC	-		RESP_ULC	-	
J21	RESETN	1		RESETN	1	
J20	TSALLN	1		TSALLN	1	
K20	DONE	1		DONE	1	
K21	INITN	1		INITN	1	
K23	M0	1		M0	1	
J23	M1	1		M1	1	
J24	M2	1		M2	1	
K24	M3	1		M3	1	
K25	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J25	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
K26	PL16C	7		PL16C	7	
K27	PL16D	7		PL16D	7	
D32	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
D31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
M23	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
N23	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
E32	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E31	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
J28	PL18C	7		PL18C	7	
K28	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F32	PL20A	7		PL21A	7	
F31	PL20B	7		PL21B	7	
L25	PL20C	7		PL21C	7	
L26	PL20D	7		PL21D	7	
G31	PL21A	7		PL22A	7	
G32	PL21B	7		PL22B	7	
J29	PL22A	7		PL25A	7	
H29	PL22B	7		PL25B	7	
M25	PL22C	7		PL25C	7	
N25	PL22D	7		PL25D	7	
H31	PL25A	7		PL23A	7	
H32	PL25B	7		PL23B	7	
M24	PL25C	7	VREF1_7	PL23C	7	VREF1_7
N24	PL25D	7	DIFFR_7	PL23D	7	DIFFR_7
L32	PL26A	7	PCLKT7_1	PL35A	7	PCLKT7_1
M32	PL26B	7	PCLKC7_1	PL35B	7	PCLKC7_1
R25	PL26C	7	PCLKT7_3	PL35C	7	PCLKT7_3
R24	PL26D	7	PCLKC7_3	PL35D	7	PCLKC7_3
N31	PL27A	7	PCLKT7_0	PL36A	7	PCLKT7_0
N32	PL27B	7	PCLKC7_0	PL36B	7	PCLKC7_0
P27	PL27C	7	PCLKT7_2	PL36C	7	PCLKT7_2
P28	PL27D	7	PCLKC7_2	PL36D	7	PCLKC7_2
P30	PL29A	6	PCLKT6_0	PL38A	6	PCLKT6_0
P29	PL29B	6	PCLKC6_0	PL38B	6	PCLKC6_0
T23	PL29C	6	PCLKT6_1	PL38C	6	PCLKT6_1
T24	PL29D	6	PCLKC6_1	PL38D	6	PCLKC6_1

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF21	PB26D	5		PB29D	5	
AN23	PB27A	5		PB45A	5	
AN22	PB27B	5		PB45B	5	
AP23	PB29A	5		PB55A	5	
AP22	PB29B	5		PB55B	5	
AG21	PB29C	5		PB55C	5	
AG20	PB29D	5		PB55D	5	
AP25	PB30A	5	PCLKT5_3	PB48A	5	PCLKT5_3
AP24	PB30B	5	PCLKC5_3	PB48B	5	PCLKC5_3
AD21	PB30C	5	PCLKT5_4	PB48C	5	PCLKT5_4
AD20	PB30D	5	PCLKC5_4	PB48D	5	PCLKC5_4
AL23	PB31A	5	PCLKT5_5	PB49A	5	PCLKT5_5
AL22	PB31B	5	PCLKC5_5	PB49B	5	PCLKC5_5
AH24	PB31C	5		PB49C	5	
AH23	PB31D	5		PB49D	5	
AM23	PB33A	5	PCLKT5_0	PB51A	5	PCLKT5_0
AM22	PB33B	5	PCLKC5_0	PB51B	5	PCLKC5_0
AJ24	PB33C	5		PB51C	5	
AJ23	PB33D	5	VREF2_5	PB51D	5	VREF2_5
AN21	PB34A	5	PCLKT5_1	PB52A	5	PCLKT5_1
AN20	PB34B	5	PCLKC5_1	PB52B	5	PCLKC5_1
AE19	PB34C	5	PCLKT5_6	PB52C	5	PCLKT5_6
AD19	PB34D	5	PCLKC5_6	PB52D	5	PCLKC5_6
AK21	PB35A	5	PCLKT5_2	PB53A	5	PCLKT5_2
AK20	PB35B	5	PCLKC5_2	PB53B	5	PCLKC5_2
AK23	PB35C	5	PCLKT5_7	PB53C	5	PCLKT5_7
AK22	PB35D	5	PCLKC5_7	PB53D	5	PCLKC5_7
AL20	PB37A	5		PB56A	5	
AL19	PB37B	5		PB56B	5	
AG19	PB37C	5		PB56C	5	
AF19	PB37D	5		PB56D	5	
AP21	PB38A	5		PB57A	5	
AP20	PB38B	5		PB57B	5	
AH21	PB38C	5		PB57C	5	
AH20	PB38D	5		PB57D	5	
AM20	PB39A	5		PB59A	5	
AM19	PB39B	5		PB59B	5	
AJ21	PB39C	5		PB59C	5	
AJ20	PB39D	5		PB59D	5	
AK19	PB41A	5		PB60A	5	
AK18	PB41B	5		PB60B	5	
AE18	PB41C	5		PB60C	5	
AD18	PB41D	5		PB60D	5	
AN19	PB42A	5		PB61A	5	
AN18	PB42B	5		PB61B	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y4	PR48B	3		PR63B	3	
W4	PR48A	3		PR63A	3	
W11	PR47D	3		PR60D	3	
V11	PR47C	3		PR60C	3	
W2	PR47B	3		PR60B	3	
V2	PR47A	3		PR60A	3	
W9	PR45D	3		PR57D	3	
V9	PR45C	3		PR57C	3	
V1	PR45B	3		PR57B	3	
U1	PR45A	3		PR57A	3	
W10	PR44D	3		PR56D	3	
V10	PR44C	3		PR56C	3	
U2	PR44B	3		PR56B	3	
T2	PR44A	3		PR56A	3	
Y8	PR43D	3		PR55D	3	
W8	PR43C	3	VREF1_3	PR55C	3	VREF1_3
W5	PR43B	3		PR55B	3	
V5	PR43A	3		PR55A	3	
V7	PR40D	3	PCLKC3_2	PR52D	3	PCLKC3_2
U7	PR40C	3	PCLKT3_2	PR52C	3	PCLKT3_2
T1	PR40B	3		PR52B	3	
R1	PR40A	3		PR52A	3	
V8	PR39D	3	PCLKC3_3	PR51D	3	PCLKC3_3
U8	PR39C	3	PCLKT3_3	PR51C	3	PCLKT3_3
U5	PR39B	3		PR51B	3	
T5	PR39A	3		PR51A	3	
V6	PR38D	3	PCLKC3_1	PR50D	3	PCLKC3_1
U6	PR38C	3	PCLKT3_1	PR50C	3	PCLKT3_1
T4	PR38B	3	PCLKC3_0	PR50B	3	PCLKC3_0
T3	PR38A	3	PCLKT3_0	PR50A	3	PCLKT3_0
U9	PR36D	2	PCLKC2_2	PR48D	2	PCLKC2_2
T9	PR36C	2	PCLKT2_2	PR48C	2	PCLKT2_2
R2	PR36B	2	PCLKC2_0	PR48B	2	PCLKC2_0
P2	PR36A	2	PCLKT2_0	PR48A	2	PCLKT2_0
T11	PR35D	2	PCLKC2_3	PR47D	2	PCLKC2_3
U11	PR35C	2	PCLKT2_3	PR47C	2	PCLKT2_3
R4	PR35B	2	PCLKC2_1	PR47B	2	PCLKC2_1
R3	PR35A	2	PCLKT2_1	PR47A	2	PCLKT2_1
T8	PR34D	2		PR46D	2	
R8	PR34C	2		PR46C	2	
P1	PR34B	2		PR46B	2	
N1	PR34A	2		PR46A	2	
R6	PR31D	2		PR43D	2	
P6	PR31C	2		PR43C	2	
M1	PR31B	2		PR43B	2	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
W30	PL69B	6	VREF1_6
W27	PL69C	6	
Y27	PL69D	6	
T33	PL70A	6	
U33	PL70B	6	
V25	PL70C	6	
W25	PL70D	6	
U34	PL71A	6	
V34	PL71B	6	
V26	PL71C	6	
W26	PL71D	6	
V33	PL74A	6	
W33	PL74B	6	
V24	PL74C	6	
W24	PL74D	6	
W31	PL77A	6	
Y31	PL77B	6	
Y29	PL77C	6	
AA29	PL77D	6	
Y33	PL79A	6	
AA33	PL79B	6	
Y28	PL79C	6	
AA28	PL79D	6	
AB32	PL90A	6	
AC32	PL90B	6	
AA26	PL90C	6	
AA27	PL90D	6	
AB31	PL91A	6	DIFFR_6
AC31	PL91B	6	
Y24	PL91C	6	
AA24	PL91D	6	
AE34	PL92A	6	
AF34	PL92B	6	
AB30	PL92C	6	
AC30	PL92D	6	
AD33	PL94A	6	
AE33	PL94B	6	
AD30	PL94C	6	
AE30	PL94D	6	
AE32	PL96A	6	
AF32	PL96B	6	
AA25	PL96C	6	
AB25	PL96D	6	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
D9	B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-	
E9	B_VDDIB3_R	-	
L13	VCC12	-	
J11	B_REFCLKN_R	-	
H11	B_REFCLKP_R	-	
M15	PT93D	1	HDC/SI
M16	PT93C	1	LDCN/SCS
F14	PT93B	1	D8/MPI_DATA8
G14	PT93A	1	CS1/MPI_CS1
L15	PT90D	1	D9/MPI_DATA9
L14	PT90C	1	D10/MPI_DATA10
D14	PT90B	1	CS0N/MPI_CS0N
E14	PT90A	1	RDN/MPI_STRB_N
L16	PT89D	1	WRN/MPI_WR_N
K16	PT89C	1	D7/MPI_DATA7
G15	PT89B	1	D6/MPI_DATA6
F15	PT89A	1	D5/MPI_DATA5
K14	PT87D	1	D4/MPI_DATA4
K13	PT87C	1	D3/MPI_DATA3
B15	PT87B	1	D2/MPI_DATA2
A15	PT87A	1	D1/MPI_DATA1
J14	PT86D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT86C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT86B	1	D0/MPI_DATA0
B16	PT86A	1	QOUT/CEON
J13	PT83D	1	VREF2_1
H13	PT83C	1	D18/MPI_DATA18
D15	PT83B	1	DOUT
E15	PT83A	1	MCA_DONE_IN
J16	PT81D	1	D19/PCLKC1_2/MPI_DATA19

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
T16	GND	-		GND	-	
T19	GND	-		GND	-	
T24	GND	-		GND	-	
T27	GND	-		GND	-	
T32	GND	-		GND	-	
U18	GND	-		GND	-	
U20	GND	-		GND	-	
U23	GND	-		GND	-	
U25	GND	-		GND	-	
U36	GND	-		GND	-	
U7	GND	-		GND	-	
G36	GND	-		GND	-	
G7	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V24	GND	-		GND	-	
V26	GND	-		GND	-	
V4	GND	-		GND	-	
V40	GND	-		GND	-	
W12	GND	-		GND	-	
W16	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W25	GND	-		GND	-	
W27	GND	-		GND	-	
W31	GND	-		GND	-	
Y17	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y22	GND	-		GND	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AA22	VCC	-		VCC	-	
AA24	VCC	-		VCC	-	
AA25	VCC	-		VCC	-	
AA26	VCC	-		VCC	-	
AB17	VCC	-		VCC	-	
AB18	VCC	-		VCC	-	
AB19	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
AB22	VCC	-		VCC	-	
AB24	VCC	-		VCC	-	

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-6FF1020I ¹	-6	Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-5FF1020I ¹	-5	Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-6FFA1020I	-6	Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-5FFA1020I	-5	Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-6FC1152I ²	-6	Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FC1152I ²	-5	Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-6FF1152I	-6	Organic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FF1152I	-5	Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-6FC1152I ¹	-6	Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-5FC1152I ¹	-5	Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-6FF1152I	-6	Organic fcBGA	1152	IND	80.1
LFSC3GA80E-5FF1152I	-5	Organic fcBGA	1152	IND	80.1
LFSC3GA80E-6FC1704I ¹	-6	Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-5FC1704I ¹	-5	Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-6FF1704I	-6	Organic fcBGA	1704	IND	80.1
LFSC3GA80E-5FF1704I	-5	Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-6FC1152I ¹	-6	Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FC1152I ¹	-5	Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FF1152I	-6	Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FF1152I	-5	Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FC1704I ¹	-6	Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FC1704I ¹	-5	Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-6FF1704I	-6	Organic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FF1704I	-5	Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).