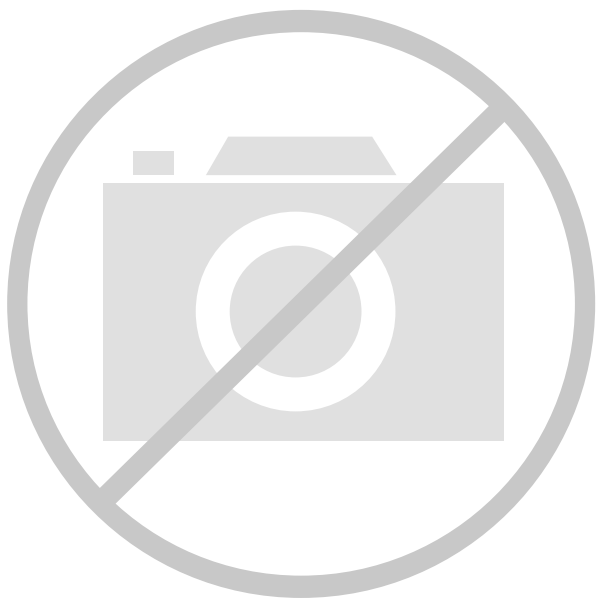




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	942
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1704-BCBGA, FCBGA
Supplier Device Package	1704-CFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga115e-6fcn1704i

Features

■ High Performance FPGA Fabric

- 15K to 115K four input Look-up Tables (LUT4s)
- 139 to 942 I/Os
- 700MHz global clock; 1GHz edge clocks

■ 4 to 32 High Speed SERDES and flexiPCS™ (per Device)

- Performance ranging from 600Mbps to 3.8Gbps
- Excellent Rx jitter tolerance (0.8UI at 3.125Gbps)
- Low Tx jitter (0.25UI typical at 3.125Gbps)
- Built-in Pre-emphasis and equalization
- Low power (typically 105mW per channel)
- Embedded Physical Coding Sublayer (PCS) provides pre-engineered implementation for the following standards:
 - GbE, XAUI, PCI Express, SONET, Serial RapidIO, 1G Fibre Channel, 2G Fibre Channel

■ 2Gbps High Performance PURESPEED™ I/O

- Supports the following performance bandwidths
 - Differential I/O up to 2Gbps DDR (1GHz Clock)
 - Single-ended memory interfaces up to 800Mbps
- 144 Tap programmable Input Delay (INDEL) block on every I/O dynamically aligns data to clock for robust performance
 - Dynamic bit Adaptive Input Logic (AIL) monitoring and control circuitry per pin that automatically ensures proper set-up and hold
 - Dynamic bus: uses control bus from DLL
 - Static per bit
- Electrical standards supported:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2, LVTTTL
 - SSTL 3/2/18 I, II; HSTL 18/15 I, II
 - PCI, PCI-X
 - LVDS, Mini-LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS
- Programmable On Die Termination (ODT)
 - Includes Thevenin Equivalent and low power V_{TT} termination options

■ Memory Intensive FPGA

- sysMEM™ embedded Block RAM

- 1 to 7.8 Mbits memory
- True Dual Port/Pseudo Dual Port/Single Port
- Dedicated FIFO logic for all block RAM
- 500MHz performance
- Additional 240K to 1.8Mbits distributed RAM

■ sysCLOCK™ Network

- Eight analog PLLs per device
 - Frequency range from 15MHz to 1GHz
 - Spread spectrum support
- 12 DLLs per device with direct control of I/O delay
 - Frequency range from 100MHz to 700MHz
- Extensive clocking network
 - 700MHz primary and 325 MHz secondary clocks
 - 1GHz I/O-connected edge clocks
- Precision Clock Divider
 - Phase matched x2 and x4 division of incoming clocks
- Dynamic Clock Select (DCS)
 - Glitch free clock MUX

■ Masked Array for Cost Optimization (MACO™) Blocks

- On-chip structured ASIC Blocks provide pre-engineered IP for low power, low cost system level integration

■ High Performance System Bus

- Ties FPGA elements together with a standard bus framework
 - Connects to peripheral user interfaces for run-time dynamic configuration

■ System Level Support

- IEEE standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer
- IEEE Standard 1532 in-system configuration
- 1.2V and 1.0V operation
- Onboard oscillator for initialization and general use
- Embedded PowerPC microprocessor interface
- Low cost wire-bond and high pin count flip-chip packaging
- Low cost SPI Flash RAM configuration

Table 2-10. Supported Output Standards⁴

Output Standard	Drive	V _{CCIO} (Nom)	On-chip Output Termination
Single-ended Interfaces			
LVTTL/D ¹	8mA, 16mA, 24mA	3.3	None.
LVC MOS33/D ¹	8mA, 16mA, 24mA	3.3	None
LVC MOS25/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	2.5	None, series: 25, 33, 50, 100
LVC MOS18/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	1.8	None, series: 25, 33, 50, 100
LVC MOS15/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	1.5	None, series: 25, 33, 50, 100
LVC MOS12/D ^{1,2}	2mA, 4mA, 8mA, 12mA	1.2	None, series: 25, 33, 50, 100
PCIX15	N/A	1.5	None
PCI33, PCIX33, AGP1X33, AGP2X33	N/A	3.3	None
HSTL18_I	N/A	1.8	None, series: 50
HSTL18_II	N/A	1.8	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
HSTL15_I	N/A	1.5	None, series: 50
HSTL15_II	N/A	1.5	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
SSTL33_I	N/A	3.3	None
SSTL33_II	N/A	3.3	None
SSTL25_I	N/A	2.5	None, series: 50
SSTL25_II	N/A	2.5	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
SSTL18_I	N/A	1.8	None, series: 33
SSTL18_II	N/A	1.8	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
Differential Interfaces			
SSTL18D_I	N/A	1.8	None, series: 33
SSTL25D_I	N/A	2.5	None, series: 50
SSTL18D_II, SSTL25D_II	N/A	1.2/2.5/3.3	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
SSTL33D_I, II	N/A	3.3	None
HSTL15D_I, HSTL18D_I	N/A	1.5/1.8	None, series: 50
HST15D_II, HSTL18D_II	N/A	1.5/1.8	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
LVDS	2mA, 3.5mA, 4mA, 6mA	N/A	None
Mini-LVDS	3.5mA, 4mA, 6mA	N/A	None
BLVDS25	N/A	N/A	None
MLVDS25	N/A	N/A	None
LVPECL33 ³	N/A	3.3	None
RSDS	2mA, 3.5mA, 4mA, 6mA	N/A	None

1. D refers to open drain capability.

2. User can select either drive current or driver impedances but not both.

3. Emulated with external resistors.

4. No GTL or GTL+ support.

PCI Clamp

A programmable PCI clamp is available on the top and bottom banks of the device. The PCI clamp can be turned “ON” or “OFF” on each pin independently. The PCI clamp is used when implementing a 3.3V PCI interface. The

Single Ended Inputs: The SC devices support a number of different termination schemes for single ended inputs:

- Parallel to V_{CCIO} or GND
- Parallel to $V_{CCIO}/2$
- Parallel to V_{TT}

Figure 2-28 shows the single ended input schemes that are supported. The nominal values of the termination resistors are shown in Table 2-9.

Figure 2-28. Input Termination Schemes

Termination Type	Discrete Off-Chip Solution	Lattice On-Chip Solution
Parallel termination to to V_{CCIO} , or parallel to GND receiving end		
Parallel termination to $V_{CCIO}/2$ receiving end		
Parallel termination to V_{TT} at receiving end		

In many situations designers can chose whether to use Thevenin or parallel to V_{TT} termination. The Thevenin approach has the benefit of not requiring a termination voltage to be applied to the device. The parallel to V_{TT} approach consumes less power.

VTT Termination Resources

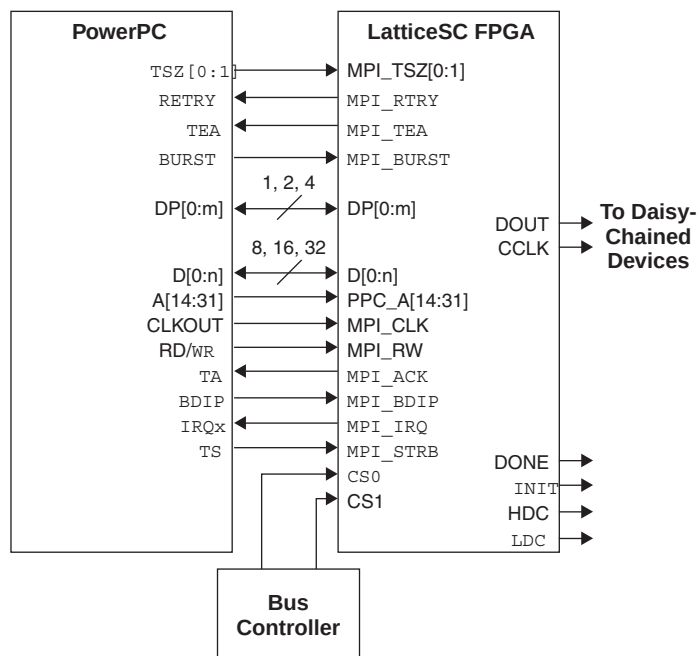
Each I/O bank, except bank 1, has a number of V_{TT} pins that must be connected if V_{TT} is used. Note V_{TT} pins can sink or source current and the power supply they are connected to must be able to handle the relatively high currents associated with the termination circuits. Note: V_{TT} is not available in all package styles.

On-chip parallel termination to V_{TT} is supported at the receiving end only. On-chip parallel output termination to V_{TT} is not supported.

The V_{TT} internal bus is also connected to the internal V_{CMT} node. Thus in one bank designers can implement either V_{TT} termination or V_{CMT} termination for differential inputs.

DDRII/RLDRAMII Termination Support

The DDR II memory and RLDRAMII (in Bidirection Data mode) standards require that the on-chip termination to V_{TT} be turned on when a pin is an input and off when the pin is an output. The LatticeSC devices contain the required circuitry to support this behavior. For additional detail refer to technical information at the end of the data sheet.

Figure 2-32. PowerPCI and MPI Schematic

Configuration and Testing

The following section describes the configuration and testing features of the LatticeSC family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeSC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS33, 25 and 18 standards. For additional detail refer to technical information at the end of the data sheet.

Device Configuration

All LatticeSC devices contain three possible ports that can be used for device configuration. The serial port, which supports bit-wide configuration, and the sysCONFIG port that supports both byte-wide and serial configuration. The MPI port supports 8-bit, 16-bit or 32-bit configuration.

The serial port supports both the IEEE Std. 1149.1 Boundary Scan specification and the IEEE Std. 1532 In-System Configuration specification. The sysCONFIG port is a 20-pin interface with six of the I/Os used as dedicated pins and the rest being dual-use pins. When sysCONFIG mode is not used, these dual-use pins are available for general purpose I/O. All I/Os for the sysCONFIG and MPI ports are in I/O bank #1.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port. Once a configuration port is selected, that port is locked and another configuration port cannot be activated until the next re-initialization sequence. For additional detail refer to technical information at the end of the data sheet.

PURESPEED I/O Recommended Operating Conditions

Standard	V _{CCIO} (V)			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 33	3.135	3.3	3.465	—	—	—
LVC MOS 25	2.375	2.5	2.625	—	—	—
LVC MOS 18	1.71	1.8	1.89	—	—	—
LVC MOS 15	1.425	1.5	1.575	—	—	—
LVC MOS 12	1.14	1.2	1.26	—	—	—
LV TTL	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
PCIX33	3.135	3.3	3.465	—	—	—
PCIX15	1.425	1.5	1.575	0.49V _{CCIO}	0.5V _{CCIO}	0.51V _{CCIO}
AGP1X33	3.135	3.3	3.465	—	—	—
AGP2X33	3.135	3.3	3.465	0.39V _{CCIO}	0.4V _{CCIO}	0.41V _{CCIO}
SSTL18_I, II ³	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II ³	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II ³	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I, II ³	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15_III ^{1,3} and IV ^{1,3}	1.425	1.5	1.575	0.68	0.9	0.9
HSTL 18_I ³ , II ³	1.71	1.8	1.89	0.816	0.9	1.08
HSTL 18_III ^{1,3} , IV ^{1,3}	1.71	1.8	1.89	0.816	1.08	1.08
GTL12 ^{1,3} , GTLPLUS15 ^{1,3}	—	—	—	0.882	1.0	1.122
LVDS	—	—	—	—	—	—
Mini-LVDS	—	—	—	—	—	—
RSDS	—	—	—	—	—	—
LVPECL33 (outputs) ²	3.135	3.3	3.465	—	—	—
LVPECL33 (inputs) ^{2,4}	—	≤ 2.5	—	—	—	—
BLVDS25 ^{2,3}	2.375	2.5	2.625	—	—	—
MLVDS25 ^{2,3}	2.375	2.5	2.625	—	—	—
SSTL18D_I ³ , II ³	1.71	1.8	1.89	—	—	—
SSTL25D_I ³ , II ³	2.375	2.5	2.625	—	—	—
SSTL33D_I ³ , II ³	3.135	3.3	3.465	—	—	—
HSTL15D_I ³ , II ³	1.425	1.5	1.575	—	—	—
HSTL18D_I ³ , II ³	1.71	1.8	1.89	—	—	—

1. Input only.

2. Inputs on chip. Outputs are implemented with the addition of external resistors.

3. Input for this standard does not depend on the value of V_{CCIO}.

4. Inputs for this standard cannot be in 3.3V VCCIO banks (≤ 2.5V only).

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AK14	PB25A	5		PB35A	5	
AK15	PB25B	5		PB35B	5	
AK16	PB27A	4		PB37A	4	
AK17	PB27B	4		PB37B	4	
AJ16	PB28A	4		PB38A	4	
AJ17	PB28B	4		PB38B	4	
AE16	PB28C	4		PB38C	4	
AH16	PB29A	4		PB39A	4	
AG16	PB29B	4		PB39B	4	
AK18	PB31A	4		PB41A	4	
AK19	PB31B	4		PB41B	4	
AH17	PB32A	4		PB42A	4	
AH18	PB32B	4		PB42B	4	
AG17	PB32D	4		PB42D	4	
AJ18	PB33A	4		PB43A	4	
AJ19	PB33B	4		PB43B	4	
AK20	PB35A	4	PCLKT4_2	PB46A	4	PCLKT4_2
AK21	PB35B	4	PCLKC4_2	PB46B	4	PCLKC4_2
AF18	PB36A	4	PCLKT4_1	PB47A	4	PCLKT4_1
AG18	PB36B	4	PCLKC4_1	PB47B	4	PCLKC4_1
AJ20	PB37A	4	PCLKT4_0	PB49A	4	PCLKT4_0
AJ21	PB37B	4	PCLKC4_0	PB49B	4	PCLKC4_0
AG19	PB37C	4	VREF2_4	PB49C	4	VREF2_4
AK22	PB39A	4	PCLKT4_5	PB51A	4	PCLKT4_5
AK23	PB39B	4	PCLKC4_5	PB51B	4	PCLKC4_5
AH19	PB39C	4		PB51C	4	
AK24	PB40A	4	PCLKT4_3	PB52A	4	PCLKT4_3
AK25	PB40B	4	PCLKC4_3	PB52B	4	PCLKC4_3
AE19	PB40C	4	PCLKT4_4	PB52C	4	PCLKT4_4
AE20	PB40D	4	PCLKC4_4	PB52D	4	PCLKC4_4
AE21	PB41A	4		PB53A	4	
AF21	PB41B	4		PB53B	4	
AG21	PB43A	4		PB55A	4	
AG22	PB43B	4		PB55B	4	
AH22	PB44A	4		PB56A	4	
AH23	PB44B	4		PB56B	4	
AH21	PB44C	4		PB56C	4	
AK28	PB45A	4		PB60A	4	
AK29	PB45B	4		PB60B	4	
AE22	PB45C	4		PB60C	4	
AJ28	PB47A	4		PB67A	4	
AH28	PB47B	4		PB67B	4	
AE24	PB47C	4	VREF1_4	PB67C	4	VREF1_4
AE25	PB47D	4		PB67D	4	
AJ29	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G1	NC	-		PL20B	7	
M4	NC	-		NC	-	
J3	NC	-		NC	-	
P5	NC	-		NC	-	
W5	NC	-		PL48C	6	
T6	NC	-		PL35C	6	
U3	NC	-		PL36A	6	
V3	NC	-		PL36B	6	
T5	NC	-		PL39A	6	
T4	NC	-		PL39B	6	
V5	NC	-		PL43C	6	
U6	NC	-		PL42C	6	
U4	NC	-		PL40A	6	
U5	NC	-		PL40B	6	
V4	NC	-		PL43D	6	
Y2	NC	-		PL47A	6	
AA2	NC	-		PL47B	6	
W3	NC	-		PL47D	6	
Y3	NC	-		PL47C	6	
AB3	NC	-		NC	-	
AC4	NC	-		PL53A	6	
AD4	NC	-		PL53B	6	
AE3	NC	-		PL56A	6	
AF3	NC	-		PL56B	6	
AF7	NC	-		PB7A	5	
AF6	NC	-		PB7B	5	
AH4	NC	-		PB8A	5	
AG5	NC	-		PB8B	5	
AF8	NC	-		PB9A	5	
AG8	NC	-		PB9B	5	
AG7	NC	-		NC	-	
AG10	NC	-		NC	-	
AF12	NC	-		NC	-	
AH7	NC	-		PB15A	5	
AE13	NC	-		PB15D	5	
AG13	NC	-		PB23C	5	
AH8	NC	-		PB15B	5	
AJ5	NC	-		PB17A	5	
AJ6	NC	-		PB17B	5	
AF15	NC	-		PB21D	5	
AJ7	NC	-		PB19A	5	
AJ8	NC	-		PB19B	5	
AE12	NC	-		PB15C	5	
AF16	NC	-		PB38D	4	
AF19	NC	-		PB49D	4	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH20	NC	-		PB51D	4	
AK27	NC	-		NC	-	
AJ24	NC	-		NC	-	
AF17	NC	-		PB42C	4	
AH27	NC	-		PB61B	4	
AD23	NC	-		PB57A	4	
AE23	NC	-		PB57B	4	
AH24	NC	-		PB59A	4	
AH25	NC	-		PB59B	4	
AH26	NC	-		PB61A	4	
AF24	NC	-		PB63A	4	
AG24	NC	-		PB63B	4	
AG25	NC	-		PB64A	4	
AF25	NC	-		PB64B	4	
AG26	NC	-		PB65A	4	
AF27	NC	-		PB65B	4	
AD28	NC	-		PR56B	3	
AC27	NC	-		PR56A	3	
AE29	NC	-		PR53B	3	
AD29	NC	-		PR53A	3	
AB30	NC	-		NC	-	
AA28	NC	-		NC	-	
Y27	NC	-		PR47C	3	
W27	NC	-		PR47D	3	
V30	NC	-		PR47A	3	
W30	NC	-		PR47B	3	
W26	NC	-		PR43D	3	
V26	NC	-		PR43C	3	
U25	NC	-		PR42C	3	
T27	NC	-		PR40B	3	
R27	NC	-		PR40A	3	
V27	NC	-		PR39B	3	
U27	NC	-		PR39A	3	
U29	NC	-		PR36B	3	
T29	NC	-		PR36A	3	
T24	NC	-		PR35C	3	
Y25	NC	-		PR48C	3	
P24	NC	-		NC	-	
K28	NC	-		NC	-	
P23	NC	-		NC	-	
L28	NC	-		NC	-	
M27	NC	-		PR21B	2	
L27	NC	-		PR21A	2	
H27	NC	-		PR20B	2	
G27	NC	-		PR20A	2	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ31	PB9A	5		PB9A	5	
AH30	PB9B	5		PB9B	5	
AM30	PB11A	5		PB11A	5	
AM29	PB11B	5		PB11B	5	
AH29	PB11C	5		PB11C	5	
AH28	PB11D	5		PB11D	5	
AJ27	PB12A	5		PB13A	5	
AK27	PB12B	5		PB13B	5	
AE22	PB12C	5		PB13C	5	
AF23	PB12D	5		PB13D	5	
AL28	PB13A	5		PB15A	5	
AL27	PB13B	5		PB15B	5	
AC21	PB13C	5		PB15C	5	
AD21	PB13D	5		PB15D	5	
AM28	PB15A	5		PB17A	5	
AM27	PB15B	5		PB17B	5	
AG23	PB15C	5		PB17C	5	
AF22	PB15D	5		PB17D	5	
AG26	PB16A	5		PB19A	5	
AG25	PB16B	5		PB19B	5	
AL26	PB17A	5		PB22A	5	
AM26	PB17B	5		PB22B	5	
AJ24	PB19A	5		PB25A	5	
AK24	PB19B	5		PB25B	5	
AE21	PB19C	5		PB25C	5	
AE20	PB19D	5		PB25D	5	
AJ22	PB20A	5	PCLKT5_3	PB30A	5	PCLKT5_3
AK22	PB20B	5	PCLKC5_3	PB30B	5	PCLKC5_3
AG22	PB20C	5	PCLKT5_4	PB30C	5	PCLKT5_4
AH22	PB20D	5	PCLKC5_4	PB30D	5	PCLKC5_4
AL23	PB21A	5	PCLKT5_5	PB31A	5	PCLKT5_5
AL22	PB21B	5	PCLKC5_5	PB31B	5	PCLKC5_5
AH23	PB21C	5		PB31C	5	
AH24	PB21D	5		PB31D	5	
AJ21	PB23A	5	PCLKT5_0	PB33A	5	PCLKT5_0
AK21	PB23B	5	PCLKC5_0	PB33B	5	PCLKC5_0
AE19	PB23C	5		PB33C	5	
AF19	PB23D	5	VREF2_5	PB33D	5	VREF2_5
AM23	PB24A	5	PCLKT5_1	PB34A	5	PCLKT5_1
AM22	PB24B	5	PCLKC5_1	PB34B	5	PCLKC5_1
AH25	PB24C	5	PCLKT5_6	PB34C	5	PCLKT5_6
AH26	PB24D	5	PCLKC5_6	PB34D	5	PCLKC5_6
AL21	PB25A	5	PCLKT5_2	PB35A	5	PCLKT5_2
AL20	PB25B	5	PCLKC5_2	PB35B	5	PCLKC5_2
AG20	PB25C	5	PCLKT5_7	PB35C	5	PCLKT5_7
AG19	PB25D	5	PCLKC5_7	PB35D	5	PCLKC5_7
AJ19	PB28A	5		PB37A	5	
AK19	PB28B	5		PB37B	5	
AD18	PB28C	5		PB37C	5	
AE18	PB28D	5		PB37D	5	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P10	GND	-		GND	-	
P13	GND	-		GND	-	
P15	GND	-		GND	-	
P18	GND	-		GND	-	
P20	GND	-		GND	-	
P24	GND	-		GND	-	
R12	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R17	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
R6	GND	-		GND	-	
T15	GND	-		GND	-	
T18	GND	-		GND	-	
T30	GND	-		GND	-	
T4	GND	-		GND	-	
U15	GND	-		GND	-	
U18	GND	-		GND	-	
U29	GND	-		GND	-	
U3	GND	-		GND	-	
V12	GND	-		GND	-	
V14	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V21	GND	-		GND	-	
V27	GND	-		GND	-	
V7	GND	-		GND	-	
W13	GND	-		GND	-	
W15	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W9	GND	-		GND	-	
Y12	GND	-		GND	-	
Y14	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y30	GND	-		GND	-	
Y4	GND	-		GND	-	
N13	VCC	-		VCC	-	
N15	VCC	-		VCC	-	
N16	VCC	-		VCC	-	
N17	VCC	-		VCC	-	
N18	VCC	-		VCC	-	
N20	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN33	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AH29	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AJ29	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AM32	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AM31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AG27	PB4C	5	
AG26	PB4D	5	
AL29	PB5A	5	
AL28	PB5B	5	
AH27	PB5C	5	
AH26	PB5D	5	VREF1_5
AN32	PB7A	5	
AP32	PB7B	5	
AF25	PB7C	5	
AE25	PB7D	5	
AN31	PB11A	5	
AN30	PB11B	5	
AK29	PB11C	5	
AK28	PB11D	5	
AP31	PB12A	5	
AP30	PB12B	5	
AD24	PB12C	5	
AE24	PB12D	5	
AM29	PB15A	5	
AM28	PB15B	5	
AJ27	PB15C	5	
AJ26	PB15D	5	
AP29	PB16A	5	
AP28	PB16B	5	
AK27	PB16C	5	
AK26	PB16D	5	
AN29	PB19A	5	
AN28	PB19B	5	
AG25	PB19C	5	
AG24	PB19D	5	
AL26	PB20A	5	
AL25	PB20B	5	
AG23	PB20C	5	
AG22	PB20D	5	
AN27	PB23A	5	
AN26	PB23B	5	
AF24	PB23C	5	
AF23	PB23D	5	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
Y18	VCC	-	
Y20	VCC	-	
AB15	VCC12	-	
AB20	VCC12	-	
N15	VCC12	-	
N20	VCC12	-	
R13	VCC12	-	
R22	VCC12	-	
Y13	VCC12	-	
Y22	VCC12	-	
AA12	VCCAUX	-	
AA23	VCCAUX	-	
AB12	VCCAUX	-	
AB16	VCCAUX	-	
AB17	VCCAUX	-	
AB18	VCCAUX	-	
AB19	VCCAUX	-	
AB23	VCCAUX	-	
AC12	VCCAUX	-	
AC13	VCCAUX	-	
Y19	GND	-	
AC14	VCCAUX	-	
AC17	VCCAUX	-	
AC21	VCCAUX	-	
AC22	VCCAUX	-	
AC23	VCCAUX	-	
M13	VCCAUX	-	
M14	VCCAUX	-	
M18	VCCAUX	-	
M21	VCCAUX	-	
M22	VCCAUX	-	
N12	VCCAUX	-	
N16	VCCAUX	-	
N17	VCCAUX	-	
N18	VCCAUX	-	
N19	VCCAUX	-	
N23	VCCAUX	-	
P12	VCCAUX	-	
P23	VCCAUX	-	
T13	VCCAUX	-	
T22	VCCAUX	-	
U12	VCCAUX	-	
U13	VCCAUX	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W33	PL42C	7		PL56C	7	
Y33	PL42D	7		PL56D	7	
W37	PL43A	7		PL57A	7	
Y37	PL43B	7		PL57B	7	
Y32	PL43C	7		PL57C	7	
AA32	PL43D	7		PL57D	7	
U38	PL46A	7		PL60A	7	
V38	PL46B	7		PL60B	7	
W34	PL46C	7		PL60C	7	
Y34	PL46D	7		PL60D	7	
T40	PL47A	7	PCLKT7_1	PL61A	7	PCLKT7_1
U40	PL47B	7	PCLKC7_1	PL61B	7	PCLKC7_1
AA33	PL47C	7	PCLKT7_3	PL61C	7	PCLKT7_3
AB33	PL47D	7	PCLKC7_3	PL61D	7	PCLKC7_3
R42	PL48A	7	PCLKT7_0	PL62A	7	PCLKT7_0
T42	PL48B	7	PCLKC7_0	PL62B	7	PCLKC7_0
AA34	PL48C	7	PCLKT7_2	PL62C	7	PCLKT7_2
AB34	PL48D	7	PCLKC7_2	PL62D	7	PCLKC7_2
U41	PL50A	6	PCLKT6_0	PL64A	6	PCLKT6_0
V41	PL50B	6	PCLKC6_0	PL64B	6	PCLKC6_0
V36	PL50C	6	PCLKT6_1	PL64C	6	PCLKT6_1
W36	PL50D	6	PCLKC6_1	PL64D	6	PCLKC6_1
U42	PL51A	6		PL65A	6	
V42	PL51B	6		PL65B	6	
AB31	PL51C	6	PCLKT6_3	PL65C	6	PCLKT6_3
AC31	PL51D	6	PCLKC6_3	PL65D	6	PCLKC6_3
W38	PL52A	6		PL66A	6	
Y38	PL52B	6		PL66B	6	
AA35	PL52C	6	PCLKT6_2	PL66C	6	PCLKT6_2
AB35	PL52D	6	PCLKC6_2	PL66D	6	PCLKC6_2
W39	PL55A	6		PL69A	6	
Y39	PL55B	6		PL69B	6	
AB32	PL55C	6	VREF1_6	PL69C	6	VREF1_6
AC32	PL55D	6		PL69D	6	
W40	PL56A	6		PL70A	6	
Y40	PL56B	6		PL70B	6	
AA36	PL56C	6		PL70C	6	
AB36	PL56D	6		PL70D	6	
W41	PL57A	6		PL71A	6	
Y41	PL57B	6		PL71B	6	
AA37	PL57C	6		PL71C	6	
AB37	PL57D	6		PL71D	6	
W42	PL59A	6		PL73A	6	
Y42	PL59B	6		PL73B	6	
AC33	PL59C	6		PL73C	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AY41	PB12A	5		PB13A	5	
BA41	PB12B	5		PB13B	5	
AT39	PB12C	5		PB13C	5	
AT38	PB12D	5		PB13D	5	
AV37	PB13A	5		PB15A	5	
AV36	PB13B	5		PB15B	5	
AM31	PB13C	5		PB15C	5	
AM32	PB13D	5		PB15D	5	
BA40	PB15A	5		PB16A	5	
BB40	PB15B	5		PB16B	5	
AM29	PB15C	5		PB16C	5	
AL29	PB15D	5		PB16D	5	
AY39	PB16A	5		PB17A	5	
AY38	PB16B	5		PB17B	5	
AN33	PB16C	5		PB17C	5	
AN32	PB16D	5		PB17D	5	
BA39	PB17A	5		PB19A	5	
BA38	PB17B	5		PB19B	5	
AT37	PB17C	5		PB19C	5	
AT36	PB17D	5		PB19D	5	
AW36	PB19A	5		PB20A	5	
AW35	PB19B	5		PB20B	5	
AM28	PB19C	5		PB20C	5	
AL28	PB19D	5		PB20D	5	
BB38	PB20A	5		PB21A	5	
BB39	PB20B	5		PB21B	5	
AR34	PB20C	5		PB21C	5	
AR33	PB20D	5		PB21D	5	
AV35	PB21A	5		PB23A	5	
AV34	PB21B	5		PB23B	5	
AT33	PB21C	5		PB23C	5	
AT34	PB21D	5		PB23D	5	
BA37	PB23A	5		PB25A	5	
BA36	PB23B	5		PB25B	5	
AP33	PB23C	5		PB25C	5	
AP32	PB23D	5		PB25D	5	
AY36	PB24A	5		PB26A	5	
AY35	PB24B	5		PB26B	5	
AN31	PB24C	5		PB26C	5	
AN30	PB24D	5		PB26D	5	
BB37	PB25A	5		PB27A	5	
BB36	PB25B	5		PB27B	5	
AP31	PB25C	5		PB27C	5	
AP30	PB25D	5		PB27D	5	
AV33	PB27A	5		PB29A	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP26	PB41C	5		PB43C	5	
AN26	PB41D	5		PB43D	5	
AY30	PB43A	5		PB45A	5	
AY29	PB43B	5		PB45B	5	
AU30	PB43C	5		PB45C	5	
AU31	PB43D	5		PB45D	5	
AV27	PB44A	5		PB46A	5	
AV26	PB44B	5		PB46B	5	
AT28	PB44C	5		PB46C	5	
AT27	PB44D	5		PB46D	5	
BA29	PB45A	5		PB47A	5	
BA28	PB45B	5		PB47B	5	
AL25	PB45C	5		PB47C	5	
AM25	PB45D	5		PB47D	5	
BB29	PB47A	5		PB49A	5	
BB28	PB47B	5		PB49B	5	
AN25	PB47C	5		PB49C	5	
AP25	PB47D	5		PB49D	5	
AY27	PB48A	5	PCLKT5_3	PB50A	5	PCLKT5_3
AY26	PB48B	5	PCLKC5_3	PB50B	5	PCLKC5_3
AT25	PB48C	5	PCLKT5_4	PB50C	5	PCLKT5_4
AT24	PB48D	5	PCLKC5_4	PB50D	5	PCLKC5_4
AW27	PB49A	5	PCLKT5_5	PB51A	5	PCLKT5_5
AW26	PB49B	5	PCLKC5_5	PB51B	5	PCLKC5_5
AU29	PB49C	5		PB51C	5	
AU28	PB49D	5		PB51D	5	
BB27	PB51A	5	PCLKT5_0	PB53A	5	PCLKT5_0
BB26	PB51B	5	PCLKC5_0	PB53B	5	PCLKC5_0
AR25	PB51C	5		PB53C	5	
AR24	PB51D	5	VREF2_5	PB53D	5	VREF2_5
BA27	PB52A	5	PCLKT5_1	PB54A	5	PCLKT5_1
BA26	PB52B	5	PCLKC5_1	PB54B	5	PCLKC5_1
AP24	PB52C	5	PCLKT5_6	PB54C	5	PCLKT5_6
AN24	PB52D	5	PCLKC5_6	PB54D	5	PCLKC5_6
AV25	PB53A	5	PCLKT5_2	PB55A	5	PCLKT5_2
AV24	PB53B	5	PCLKC5_2	PB55B	5	PCLKC5_2
AU27	PB53C	5	PCLKT5_7	PB55C	5	PCLKT5_7
AU26	PB53D	5	PCLKC5_7	PB55D	5	PCLKC5_7
BA25	PB55A	5		PB57A	5	
BA24	PB55B	5		PB57B	5	
AU24	PB55C	5		PB57C	5	
AU25	PB55D	5		PB57D	5	
BB24	PB56A	5		PB58A	5	
BB25	PB56B	5		PB58B	5	
AM23	PB56C	5		PB58C	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K14	VCC12	-		VCC12	-	
H11	B_VDDIB2_R	-		B_VDDIB2_R	-	
D8	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
E8	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
G5	VCC12	-		VCC12	-	
B9	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
L12	B_VDDOB2_R	-		B_VDDOB2_R	-	
A9	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
C5	B_VDDOB3_R	-		B_VDDOB3_R	-	
A10	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
H5	VCC12	-		VCC12	-	
B10	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
E9	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
D9	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
J13	VCC12	-		VCC12	-	
H12	B_VDDIB3_R	-		B_VDDIB3_R	-	
J12	VCC12	-		VCC12	-	
M14	B_REFCLKN_R	-		B_REFCLKN_R	-	
L14	B_REFCLKP_R	-		B_REFCLKP_R	-	
J14	VCC12	-		VCC12	-	
G12	C_VDDIB0_R	-		C_VDDIB0_R	-	
D10	C_HDINP0_R	-	PCS 3E2 CH 0 IN P	C_HDINP0_R	-	PCS 3E2 CH 0 IN P
E10	C_HDINN0_R	-	PCS 3E2 CH 0 IN N	C_HDINN0_R	-	PCS 3E2 CH 0 IN N
H6	VCC12	-		VCC12	-	
B11	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P
M12	C_VDDOB0_R	-		C_VDDOB0_R	-	
A11	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N
L11	C_VDDOB1_R	-		C_VDDOB1_R	-	
A12	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N
K11	VCC12	-		VCC12	-	
B12	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P
E11	C_HDINN1_R	-	PCS 3E2 CH 1 IN N	C_HDINN1_R	-	PCS 3E2 CH 1 IN N
D11	C_HDINP1_R	-	PCS 3E2 CH 1 IN P	C_HDINP1_R	-	PCS 3E2 CH 1 IN P
H13	VCC12	-		VCC12	-	
C6	C_VDDIB1_R	-		C_VDDIB1_R	-	
H15	VCC12	-		VCC12	-	
G13	C_VDDIB2_R	-		C_VDDIB2_R	-	
D12	C_HDINP2_R	-	PCS 3E2 CH 2 IN P	C_HDINP2_R	-	PCS 3E2 CH 2 IN P
E12	C_HDINN2_R	-	PCS 3E2 CH 2 IN N	C_HDINN2_R	-	PCS 3E2 CH 2 IN N
J9	VCC12	-		VCC12	-	
B13	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P
K10	C_VDDOB2_R	-		C_VDDOB2_R	-	
A13	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N
J10	C_VDDOB3_R	-		C_VDDOB3_R	-	
A14	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FCN1152C ¹	-7	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FCN1704C ¹	-7	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FFN1704C	-7	Lead-Free Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FCN1152C ¹	-7	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FCN1704C ¹	-7	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FFN1704C	-7	Lead-Free Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

For Further Information

For further information about the flexiPCS, see the [LatticeSC/M Family flexiPCS Data Sheet](#).

A variety of technical notes for the LatticeSC/M family are also available on the Lattice Semiconductor website at www.latticesemi.com.

- [LatticeSC PURESPEED I/O Usage Guide](#) (TN1088)
- [LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide](#) (TN1158)
- [LatticeSC sysCLOCK PLL/DLL User's Guide](#) (TN1098)
- [On-Chip Memory Usage Guide for LatticeSC Devices](#) (TN1094)
- [LatticeSC/M DDR/DDR2 SDRAM Memory Interface User's Guide](#) (TN1099)
- [LatticeSC QDRII/II+ SRAM Memory Interface User's Guide](#) (TN1096)
- [LatticeSC sysCONFIG Usage Guide](#) (TN1080)
- [LatticeSC MPI/System Bus](#) (TN1085)
- [SPI Serial Flash Programming Using ispJTAG in LatticeSC Devices](#) (TN1100)
- [Power Estimation and Management for LatticeSC Devices](#) (TN1101)
- [LatticeSC SERDES Jitter](#) (TN1084)
- [LatticeSC FPGAs: Implementing 3.3V Interfaces in 2.5V VCCIO Banks](#) (TN1110)
- [Lattice PCI Express Basic Demo User's Guide](#) (UG08)
- [LatticeSC flexiPCS/SERDES Design Guide](#) (TN1145)
- [Temperature Sensing Diode in LatticeSC Devices](#) (TN1115)
- [SPI4.2 Interoperability Between ORSPI4 and LatticeSC Devices](#) (TN1116)

For further information on Interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- Optical Interface (SPI-4.2, XSBI, CSIX and XGMII): www.oiforum.com
- RAPIDIO: www.rapidio.org
- PCI/PCIX: www.pcisig.com

Date	Version	Section	Change Summary
June 2006 (cont.)	01.2 (cont.)	DC and Switching Characteristics (cont.)	Updated Typical Building Block Performance with ispLEVER 6.0 values.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.0 values.
			Updated Lattice SC Internal Timing Parameters with ispLEVER 6.0 values.
			Updated Lattice SC Family Timing Adders with ispLEVER 6.0 values
			Changed % spread from 1 to 0.5 min and from 3 to 1.5 max.
			Changed conditions to refer to “with multiplication” and “without multiplication”.
			Changed the formula for t_{OPJIT} with multiplication (same result, different representation).
		Pinout Information	Expanded definition of NC.
			Expanded definition of GND.
			Expanded definition of VTT_x.
			Expanded definition of VCC12.
			Added accuracy of TEMP pin.
			Added RESPN_[ULC/URC].
			Updated Pin Information Summary with additional devices and packages.
			Added additional devices and packages pinouts.
			Removed Power Supply and NC connections table
			Removed VTT table
			Removed LFSC25 Logic Signal Connections: 900-Ball fBGA1 table
			Changed all VDDP, VDDTX and VDDR _X to VCC12.
		Ordering Information	Added dual marking.
			Added lead free packaging information to part number description.
August 2006	01.3	Introduction	Added SC40 1152 information to Table 1-1.
			Updated Table 1-3 with ispLEVER 6.0 SP1 results.
		Architecture	Added SSTL18 II to Table 2-8.
			Changed Table 2-10 VCCIO column to “N/A” for LVDS, mini-LVDS, BLVDS25, MLVDS25, HYPT and RSDS.
			Changed Hypertransport performance to 700 MHz (1400 Mbps) in Table 2-11.
			Changed SPI4.2 performance to 500 MHz (1000 Mbps) in Table 2-11
			Added “On packages that include PROBE_GND, the most accurate measurements will occur between the TEMP pin and the PROBE_GND pin. On packages that do not include PROBE_GND, measurements should be made between the TEMP pin and board ground.”
			Added VCCIO of 2.5 V for LVPECL33 in table 2-9.
		DC and Switching Characteristics	Updated Typical Building Block Performance with ispLEVER 6.0 SP1 results.
			Updated Initialization and Standby Supply Current table to break out ICC and ICC12.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.0 SP1 results.
			Updated LatticeSC Internal Timing Parameters with ispLEVER 6.0 SP1 results.

Date	Version	Section	Change Summary
December 2011	02.4	DC and Switching Characteristics	Updated JTAG Port Timing Specifications table.