Lattice Semiconductor Corporation - LFSC3GA115E-6FF1704I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	942
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1704-BBGA, FCBGA
Supplier Device Package	1704-OFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga115e-6ff1704i

Table 1-1. LatticeSC Family Selection Guide[1]

Device	SC15	SC25	SC40	SC80	SC115
LUT4s (K)	15	25	40	80	115
sysMEM Blocks (18Kb)	56	104	216	308	424
Embedded Memory (Mbits)	1.03	1.92	3.98	5.68	7.8
Max. Distributed Memory (Mbits)	0.24	0.41	0.65	1.28	1.84
Number of 3.8Gbps SERDES (Max.)	8	16	16	32	32
DLLs	12	12	12	12	12
Analog PLLs	8	8	8	8	8
MACO Blocks	4	6	10	10	12
Package I/O/SERDES Combinations (1mm ball pitch)					
256-ball fpBGA (17 x 17mm)	139/4				
900-ball fpBGA (31 x 31mm)	300/8	378/8			
1020-ball fcBGA (33 x 33mm)[2]		476/16	562/16		
1152-ball fcBGA (35 x 35mm)[3]			604/16	660/16	660/16
1704-ball fcBGA (42.5 x 42.5mm)[3]				904/32	942/32

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per PCN #02A-10.
3. Ceramic fcBGA converted to organic fcBGA per PCN #01A-10.

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

Table 1-2. LatticeSCM Family

Device	SCM15	SCM25	SCM40	SCM80	SCM115
flexiMAC Blocks • 1GbE Mode • 10GbE Mode • PCI Express Mode	1	2	2	2	4
SPI4.2 Blocks	1	2	2	2	2
Memory Controller Blocks • DDR/DDR2 DRAM Mode • QDR II/II+ SRAM Mode • RLDRAM I • RLDRAM II CIO/SIO	1	2	2	2	2
Low-Speed CDR Blocks	0	0	2	2	2
PCI Express LTSSM (PHY) Blocks	1	0	2	2	2

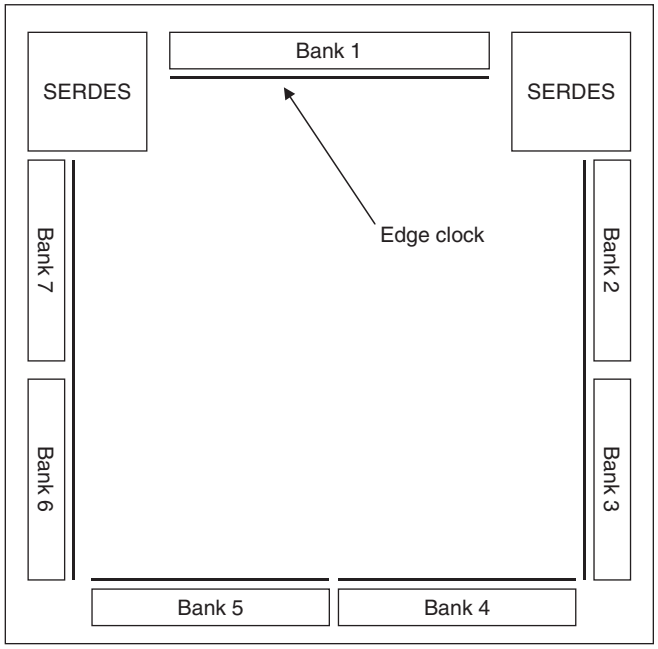
Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

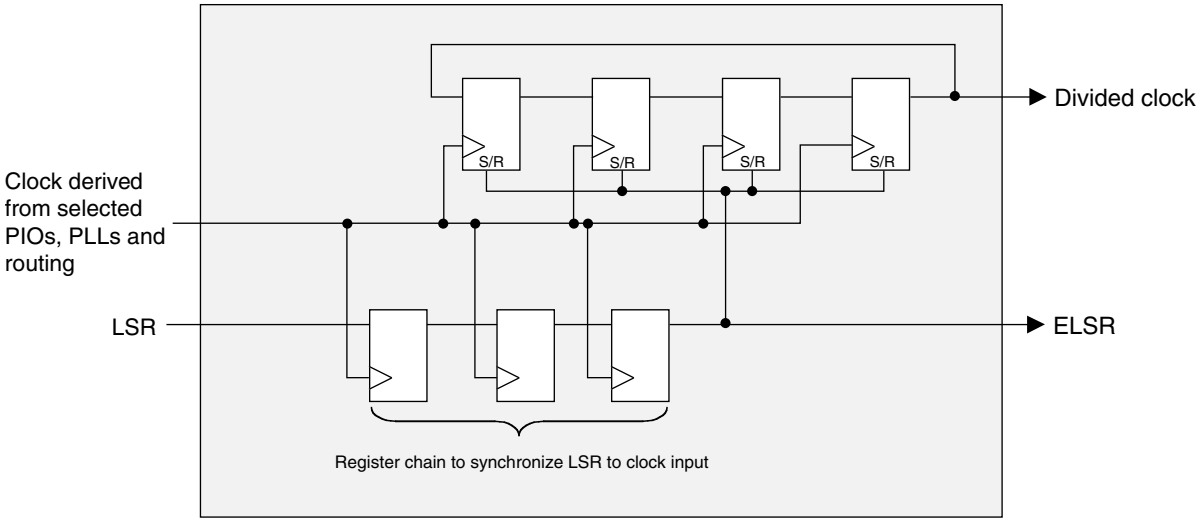
Figure 2-7. Edge Clock Resources



Precision Clock Divider

Each set of edge clocks has four high-speed dividers associated with it. These are intended for generating a slower speed system clock from the high-speed edge clock. The block operates in a DIV2 or DIV4 mode and maintains a known phase relationship between the divided down clock and high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PIOs, PLLs and routing. The clock divider outputs serve as primary clock sources. This circuit also generates an edge local set/reset (ELSR) signal which is fed to the PIOs via the edge clock network and is used for the rest of the I/O gearing logic.

Figure 2-8. Clock Divider Circuit



Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is

toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-9 illustrates the DCS Block diagram.

Figure 2-9. DCS Block Diagram

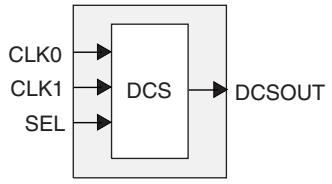
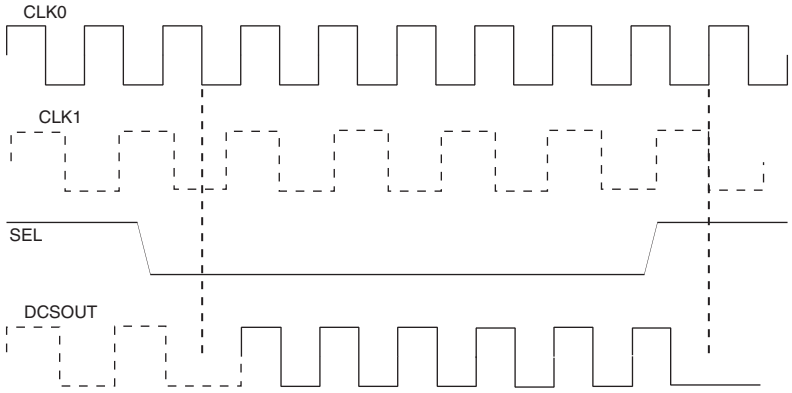


Figure 2-10 shows timing waveforms for one of the DCS operating modes. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-10. DCS Waveforms



Clock Boosting

There are programmable delays available in the clock signal paths in the PFU, PIC and EBR blocks. These allow setup and clock-to-output times to be traded to meet critical timing without slowing the system clock. If this feature is enabled then the design tool automatically uses these delays to improve timing performance.

Global Set/Reset

There is a global set/reset (GSR) network on the device that is distributed to all FFs, PLLs, DLLs and other blocks on the device. This GSR network can operate in two modes:

a) asynchronous - no clock is required to get into or out of the reset state.

b) synchronous - The global GSR net is synchronized to a user selected clock. In this mode it continues to be asynchronous to get into the reset state, but is synchronous to get out of the reset state. This allows all registers on the device to become operational in the same clock period. The synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met (not from the GSR being released).

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider and two clock output dividers. The input divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal.

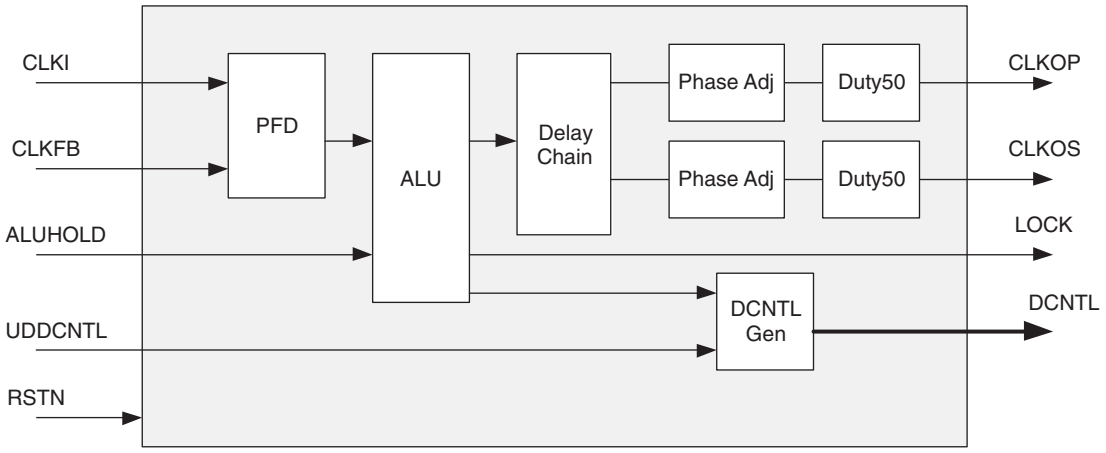
There is a Digital Control (DCNTL) bus available from the DLL block. This Digital Control bus is available to the delay lines in the PIC blocks in the adjacent banks. The UDDCNTL signal allows the user to latch the current value on the digital control bus.

Figure 2-12 shows the DLL block diagram of the DLL inputs and outputs. The output of the phase frequency detector controls an arithmetic logic unit (ALU) to add or subtract one delay tap. The digital output of this ALU is used to control the delay value of the delay chain and this digital code is transmitted via the DCNTL bus.

The sysCLOCK DLL can be configured at power-up, then, if desired, reconfigured dynamically through the Serial Memory Interface bus which interfaces with the on-chip Microprocessor Interface (MPI) bus. In addition, users can drive the SMI interface from routing if desired.

The user can configure the DLL for many common functions such as clock injection match and single delay cell. Lattice provides primitives in its design for time reference delay (DDR memory) and clock injection delay removal.

Figure 2-12. DLL Diagram



PLL/DLL Cascading

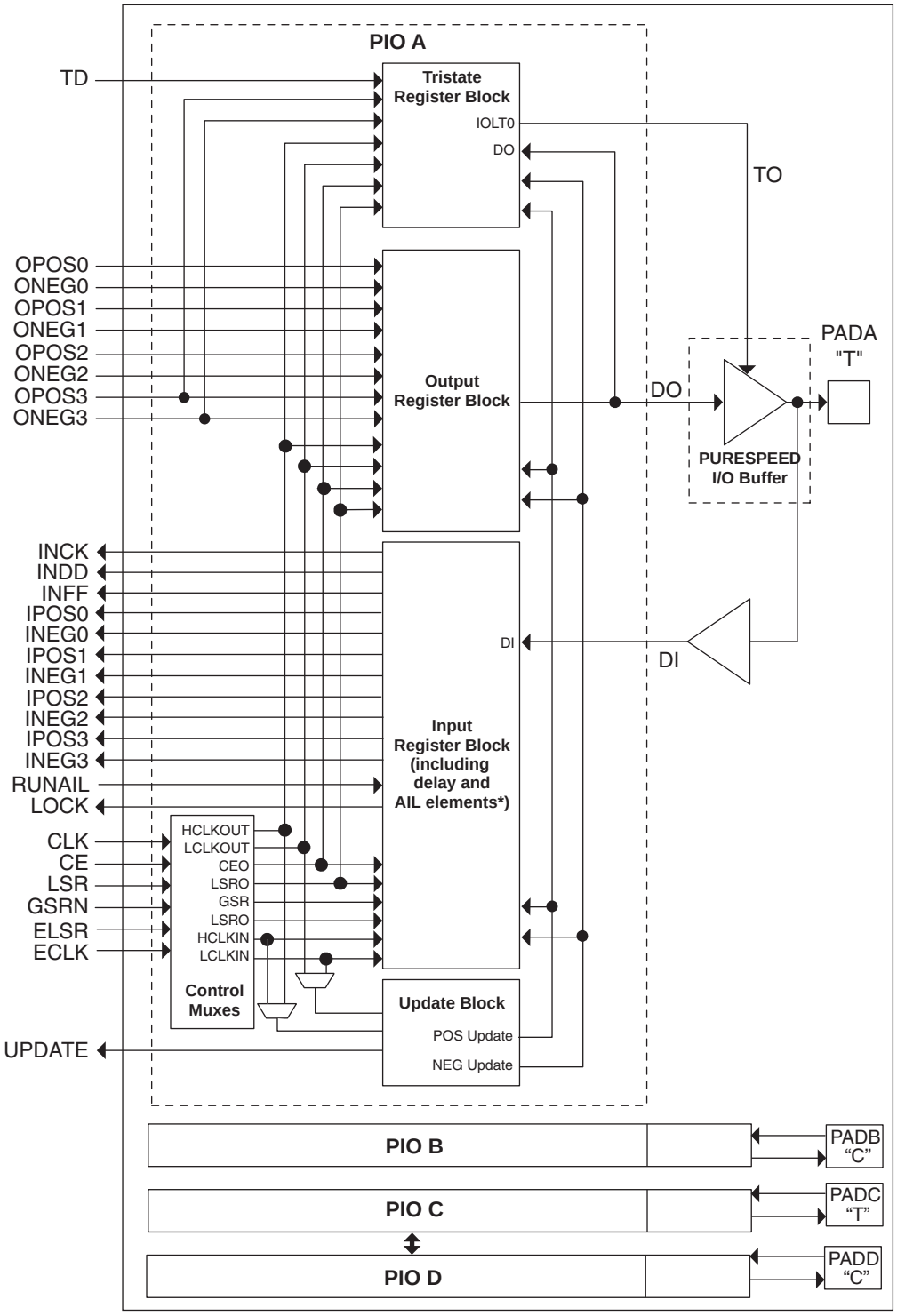
The LatticeSC devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are as follows:

- PLL to PLL
- PLL to DLL
- DLL to DLL
- DLL to PLL

DLLs are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLL and PLLs.

When cascading the DLL to the PLL, the DLL can be used to drive the PLL to create fine phase shifts of an input clock signal. Figure 2-13 shows a shift of all outputs for CLKOP and CLKOS out in time.

Figure 2-17. PIC Diagram



*AIL only on A or C pads located on the left, right and bottom of the device.

The A/B PIOs on the left and the right of the device can be paired to form a differentiated driver. The A/B and C/D PIOs on all sides of the device can be paired to form differential receivers. Either A or C PIOs on all sides except the one on top also provide a connection to an adaptive input logic capability that facilitates the implementation of

- 8-bit SERDES Only
- 10-bit SERDES Only
- SONET (STS-12/STS-48)
- Gigabit Ethernet
- Fibre Channel
- XAUI
- Serial RapidIO
- PCI-Express
- Generic 8b10b

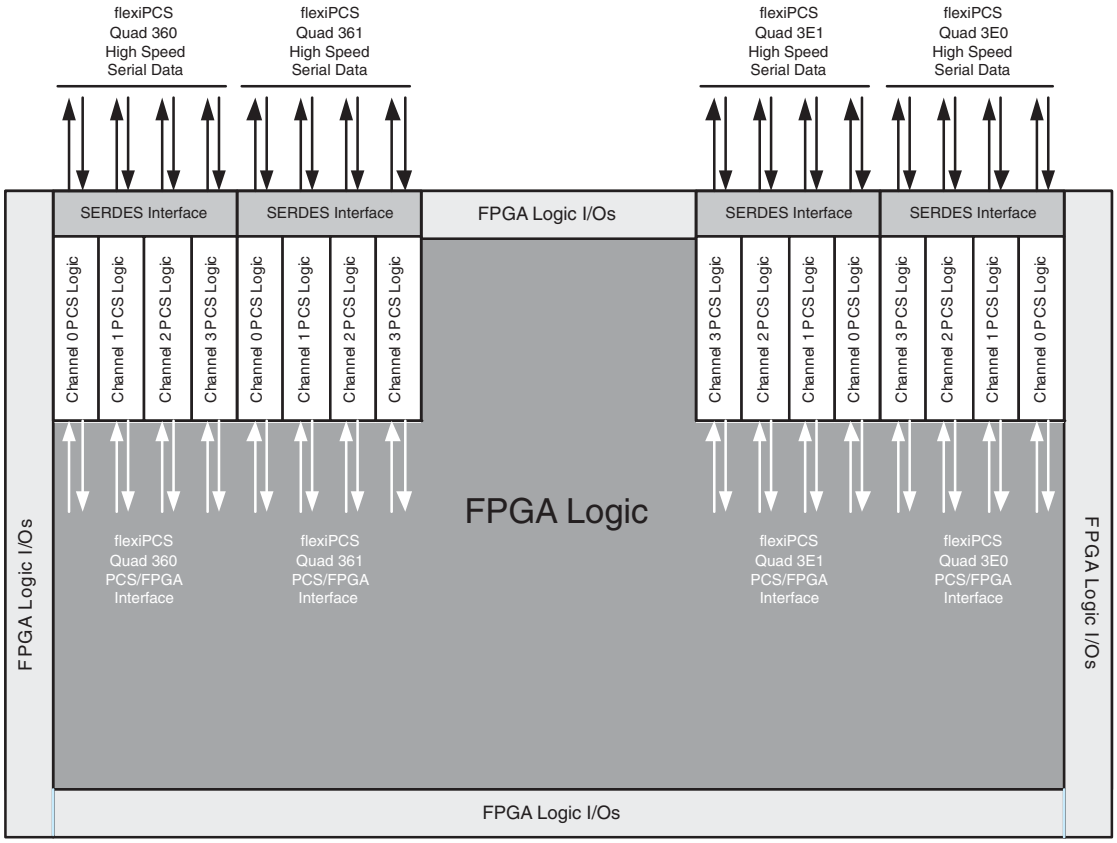
flexiPCS Quad

The flexiPCS logic is arranged in quads containing logic for four independent full-duplex data channels. Each device in the LatticeSC family has up to eight quads of flexiPCS logic. The LatticeSC Family Selection Guide table on the first page of this data sheet contains the number of flexiPCS channels present on the chip. Note that in some packages (particularly lower pin count packages), not all channels from all quads on a given device may be bonded to package pins.

Each quad supports up to four channels of full-duplex data and can be programmed into any one of several protocol based modes. Each quad requires its own reference clock which can be sourced externally or from the FPGA logic. The user can utilize between one and four channels in a quad, depending on the application.

Figure 2-30 shows an example of four flexiPCS quads in a LatticeSC device. Quads are labeled according to the address of their software controlled registers.

Figure 2-30. LatticeSC flexiPCS



Since each quad has its own reference clock, different quads can support different standards on the same chip. This feature makes the LatticeSC family of devices ideal for bridging between different standards.

Input Delay Block/AIL Timing

Parameter	Description	Min.	Typ.	Max.	Units
t_{FDEL}	Fine delay time	35	45	80	ps
t_{CDEL}	Coarse delay time	1120	1440	2560	ps
jt_{AIL}	AIL jitter tolerance	1- ((N^1 * t_{FDEL}) / (Clock Period))			UI

1. N = number of fine delays used in a particular AIL setting

GSR Timing

Parameter	Description	VCC	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{SYNC\_GSR\_MAX}$	Maximum operating frequency for synchronous GSR	1.14V	—	438	—	417	—	398	MHz
		0.95V	—	378	—	355	—	337	MHz
$t_{ASYNC\_GSR\_MPW}$	Minimum pulse width of asynchronous input	—	—	—	—	—	3.3	—	ns

Note: Synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met.

Internal System Bus Timing

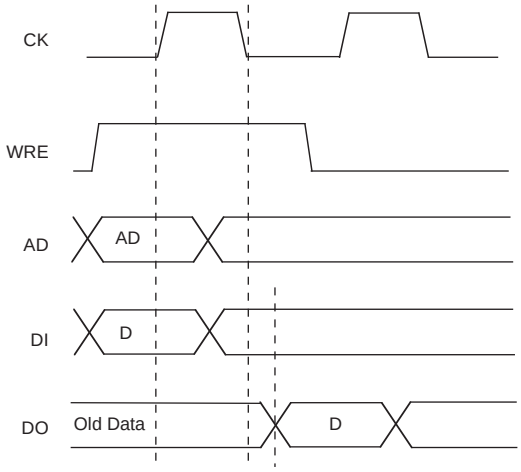
Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HCLK}	Maximum operating frequency for internal system bus HCLK.	—	200	—	200	—	200	MHz

Note: There is no minimum frequency. If HCLK is sourced from the embedded oscillator, the minimum frequency limitation of the oscillator/ divider is about 0.3 MHz. Refer to the osciallator data for missing configuration modes.

Timing Diagrams

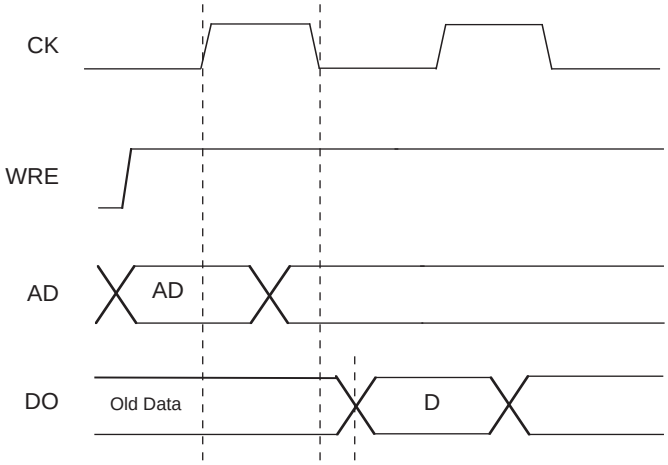
PFU Timing Diagrams

Figure 3-4. Slice Single/Dual Port Write Cycle Timing



Notes:
- Rising Edge for latching WREN, WAD and DATAIN.
- WREN must continue past falling edge clock.
- Data output occurs on negative edge.

Figure 3-5. Slice Single/Dual Port Read Cycle Timing



LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
R29	PR28B	3		PR31B	3	
P29	PR28A	3		PR31A	3	
P27	PR27C	3	PCLKT3_3	PR30C	3	PCLKT3_3
N29	PR27B	3		PR30B	3	
N28	PR27A	3		PR30A	3	
R25	PR26D	3	PCLKC3_1	PR29D	3	PCLKC3_1
R26	PR26C	3	PCLKT3_1	PR29C	3	PCLKT3_1
R28	PR26B	3	PCLKC3_0	PR29B	3	PCLKC3_0
P28	PR26A	3	PCLKT3_0	PR29A	3	PCLKT3_0
N27	PR24D	2	PCLKC2_2	PR27D	2	PCLKC2_2
P26	PR24C	2	PCLKT2_2	PR27C	2	PCLKT2_2
L30	PR24B	2	PCLKC2_0	PR27B	2	PCLKC2_0
K30	PR24A	2	PCLKT2_0	PR27A	2	PCLKT2_0
J30	PR23B	2	PCLKC2_1	PR26B	2	PCLKC2_1
H30	PR23A	2	PCLKT2_1	PR26A	2	PCLKT2_1
M26	PR22D	2	DIFFR_2	PR25D	2	DIFFR_2
M25	PR22C	2	VREF1_2	PR25C	2	VREF1_2
G29	PR22B	2		PR25B	2	
F29	PR22A	2		PR25A	2	
H28	PR19D	2		PR22D	2	
J28	PR19C	2		PR22C	2	
E30	PR19B	2		PR22B	2	
E29	PR19A	2		PR22A	2	
L26	PR18D	2	VREF2_2	PR18D	2	VREF2_2
L25	PR18C	2		PR18C	2	
F28	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G28	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
K26	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
K25	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
D30	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
D29	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
G26	PR15D	2		PR16D	2	
H26	PR15C	2		PR16C	2	
E28	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
D28	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
J25	VCCJ	-		VCCJ	-	
H25	TDO	-	TDO	TDO	-	TDO
J26	TMS	-		TMS	-	
G25	TCK	-		TCK	-	
G24	TDI	-		TDI	-	
F26	PROGRAMN	1		PROGRAMN	1	
H24	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
F25	CCLK	1		CCLK	1	
D27	VCC12	-		VCC12	-	
E26	VCC12	-		VCC12	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT37D	1	WRN/MPI_WR_N	PT46D	1	WRN/MPI_WR_N
F18	PT37C	1	D7/MPI_DATA7	PT46C	1	D7/MPI_DATA7
C18	PT37B	1	D6/MPI_DATA6	PT46B	1	D6/MPI_DATA6
C17	PT37A	1	D5/MPI_DATA5	PT46A	1	D5/MPI_DATA5
E17	PT36D	1	D4/MPI_DATA4	PT45D	1	D4/MPI_DATA4
E16	PT36C	1	D3/MPI_DATA3	PT45C	1	D3/MPI_DATA3
G18	PT35B	1	D2/MPI_DATA2	PT45B	1	D2/MPI_DATA2
G17	PT35A	1	D1/MPI_DATA1	PT45A	1	D1/MPI_DATA1
B18	PT33B	1	D0/MPI_DATA0	PT43B	1	D0/MPI_DATA0
B17	PT33A	1	QOUT/CEON	PT43A	1	QOUT/CEON
G16	PT32D	1	VREF2_1	PT42D	1	VREF2_1
A18	PT32B	1	DOUT	PT42B	1	DOUT
A17	PT32A	1	MCA_DONE_IN	PT42A	1	MCA_DONE_IN
H18	PT31B	1	MCA_CLK_P1_OUT	PT41B	1	MCA_CLK_P1_OUT
H17	PT31A	1	MCA_CLK_P1_IN	PT41A	1	MCA_CLK_P1_IN
D17	PT29B	1	MCA_CLK_P2_OUT	PT39B	1	MCA_CLK_P2_OUT
D16	PT29A	1	MCA_CLK_P2_IN	PT39A	1	MCA_CLK_P2_IN
F17	PT28D	1	MCA_DONE_OUT	PT38D	1	MCA_DONE_OUT
F16	PT28C	1	BUSYN/RCLK/SCK	PT38C	1	BUSYN/RCLK/SCK
C16	PT28B	1	DP0/MPI_PAR0	PT38B	1	DP0/MPI_PAR0
C15	PT28A	1	MPI_TA	PT38A	1	MPI_TA
B16	PT27B	1	PCLKC1_0	PT37B	1	PCLKC1_0
B15	PT27A	1	PCLKT1_0/MPI_CLK	PT37A	1	PCLKT1_0/MPI_CLK
H16	PT25D	1	DP3/PCLKC1_4/MPI_PAR3	PT35D	1	DP3/PCLKC1_4/MPI_PAR3
A16	PT25B	1	MPI_RETRY	PT35B	1	MPI_RETRY
A15	PT25A	1	A0/MPI_ADDR14	PT35A	1	A0/MPI_ADDR14
G15	PT24D	1	A1/MPI_ADDR15	PT33D	1	A1/MPI_ADDR15
F15	PT24C	1	A2/MPI_ADDR16	PT33C	1	A2/MPI_ADDR16
E15	PT24B	1	A3/MPI_ADDR17	PT33B	1	A3/MPI_ADDR17
D15	PT24A	1	A4/MPI_ADDR18	PT33A	1	A4/MPI_ADDR18
C14	PT23B	1	A5/MPI_ADDR19	PT32B	1	A5/MPI_ADDR19
C13	PT23A	1	A6/MPI_ADDR20	PT32A	1	A6/MPI_ADDR20
H14	PT21C	1	VREF1_1	PT31C	1	VREF1_1
B14	PT21B	1	A7/MPI_ADDR21	PT31B	1	A7/MPI_ADDR21
B13	PT21A	1	A8/MPI_ADDR22	PT31A	1	A8/MPI_ADDR22
G14	PT20B	1	A9/MPI_ADDR23	PT29B	1	A9/MPI_ADDR23
F14	PT20A	1	A10/MPI_ADDR24	PT29A	1	A10/MPI_ADDR24
A14	PT19B	1	A11/MPI_ADDR25	PT28B	1	A11/MPI_ADDR25
A13	PT19A	1	A12/MPI_ADDR26	PT28A	1	A12/MPI_ADDR26
G13	PT17D	1	D11/MPI_DATA11	PT27D	1	D11/MPI_DATA11
H13	PT17C	1	D12/MPI_DATA12	PT27C	1	D12/MPI_DATA12
E14	PT17B	1	A13/MPI_ADDR27	PT27B	1	A13/MPI_ADDR27
E13	PT17A	1	A14/MPI_ADDR28	PT27A	1	A14/MPI_ADDR28
G12	PT15D	1	A16/MPI_ADDR30	PT25D	1	A16/MPI_ADDR30
G11	PT15C	1	D13/MPI_DATA13	PT25C	1	D13/MPI_DATA13

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G1	NC	-		PL20B	7	
M4	NC	-		NC	-	
J3	NC	-		NC	-	
P5	NC	-		NC	-	
W5	NC	-		PL48C	6	
T6	NC	-		PL35C	6	
U3	NC	-		PL36A	6	
V3	NC	-		PL36B	6	
T5	NC	-		PL39A	6	
T4	NC	-		PL39B	6	
V5	NC	-		PL43C	6	
U6	NC	-		PL42C	6	
U4	NC	-		PL40A	6	
U5	NC	-		PL40B	6	
V4	NC	-		PL43D	6	
Y2	NC	-		PL47A	6	
AA2	NC	-		PL47B	6	
W3	NC	-		PL47D	6	
Y3	NC	-		PL47C	6	
AB3	NC	-		NC	-	
AC4	NC	-		PL53A	6	
AD4	NC	-		PL53B	6	
AE3	NC	-		PL56A	6	
AF3	NC	-		PL56B	6	
AF7	NC	-		PB7A	5	
AF6	NC	-		PB7B	5	
AH4	NC	-		PB8A	5	
AG5	NC	-		PB8B	5	
AF8	NC	-		PB9A	5	
AG8	NC	-		PB9B	5	
AG7	NC	-		NC	-	
AG10	NC	-		NC	-	
AF12	NC	-		NC	-	
AH7	NC	-		PB15A	5	
AE13	NC	-		PB15D	5	
AG13	NC	-		PB23C	5	
AH8	NC	-		PB15B	5	
AJ5	NC	-		PB17A	5	
AJ6	NC	-		PB17B	5	
AF15	NC	-		PB21D	5	
AJ7	NC	-		PB19A	5	
AJ8	NC	-		PB19B	5	
AE12	NC	-		PB15C	5	
AF16	NC	-		PB38D	4	
AF19	NC	-		PB49D	4	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L33	PL27B	7		PL35B	7	
M30	PL27C	7		PL35C	7	
N30	PL27D	7		PL35D	7	
M31	PL29A	7		PL37A	7	
N31	PL29B	7		PL37B	7	
P24	PL29C	7		PL37C	7	
R24	PL29D	7		PL37D	7	
M33	PL30A	7		PL42A	7	
N33	PL30B	7		PL42B	7	
U25	PL30C	7		PL42C	7	
T25	PL30D	7		PL42D	7	
L34	PL31A	7		PL43A	7	
M34	PL31B	7		PL43B	7	
P29	PL31C	7		PL43C	7	
R29	PL31D	7		PL43D	7	
N34	PL34A	7		PL46A	7	
P34	PL34B	7		PL46B	7	
R27	PL34C	7		PL46C	7	
T27	PL34D	7		PL46D	7	
R32	PL35A	7	PCLKT7_1	PL47A	7	PCLKT7_1
R31	PL35B	7	PCLKC7_1	PL47B	7	PCLKC7_1
U24	PL35C	7	PCLKT7_3	PL47C	7	PCLKT7_3
T24	PL35D	7	PCLKC7_3	PL47D	7	PCLKC7_3
P33	PL36A	7	PCLKT7_0	PL48A	7	PCLKT7_0
R33	PL36B	7	PCLKC7_0	PL48B	7	PCLKC7_0
T26	PL36C	7	PCLKT7_2	PL48C	7	PCLKT7_2
U26	PL36D	7	PCLKC7_2	PL48D	7	PCLKC7_2
T32	PL38A	6	PCLKT6_0	PL50A	6	PCLKT6_0
T31	PL38B	6	PCLKC6_0	PL50B	6	PCLKC6_0
U29	PL38C	6	PCLKT6_1	PL50C	6	PCLKT6_1
V29	PL38D	6	PCLKC6_1	PL50D	6	PCLKC6_1
T30	PL39A	6		PL51A	6	
U30	PL39B	6		PL51B	6	
U27	PL39C	6	PCLKT6_3	PL51C	6	PCLKT6_3
V27	PL39D	6	PCLKC6_3	PL51D	6	PCLKC6_3
R34	PL40A	6		PL52A	6	
T34	PL40B	6		PL52B	6	
U28	PL40C	6	PCLKT6_2	PL52C	6	PCLKT6_2
V28	PL40D	6	PCLKC6_2	PL52D	6	PCLKC6_2
V30	PL43A	6		PL55A	6	
W30	PL43B	6		PL55B	6	
W27	PL43C	6	VREF1_6	PL55C	6	VREF1_6
Y27	PL43D	6		PL55D	6	
T33	PL44A	6		PL56A	6	
U33	PL44B	6		PL56B	6	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y4	PR48B	3		PR63B	3	
W4	PR48A	3		PR63A	3	
W11	PR47D	3		PR60D	3	
V11	PR47C	3		PR60C	3	
W2	PR47B	3		PR60B	3	
V2	PR47A	3		PR60A	3	
W9	PR45D	3		PR57D	3	
V9	PR45C	3		PR57C	3	
V1	PR45B	3		PR57B	3	
U1	PR45A	3		PR57A	3	
W10	PR44D	3		PR56D	3	
V10	PR44C	3		PR56C	3	
U2	PR44B	3		PR56B	3	
T2	PR44A	3		PR56A	3	
Y8	PR43D	3		PR55D	3	
W8	PR43C	3	VREF1_3	PR55C	3	VREF1_3
W5	PR43B	3		PR55B	3	
V5	PR43A	3		PR55A	3	
V7	PR40D	3	PCLKC3_2	PR52D	3	PCLKC3_2
U7	PR40C	3	PCLKT3_2	PR52C	3	PCLKT3_2
T1	PR40B	3		PR52B	3	
R1	PR40A	3		PR52A	3	
V8	PR39D	3	PCLKC3_3	PR51D	3	PCLKC3_3
U8	PR39C	3	PCLKT3_3	PR51C	3	PCLKT3_3
U5	PR39B	3		PR51B	3	
T5	PR39A	3		PR51A	3	
V6	PR38D	3	PCLKC3_1	PR50D	3	PCLKC3_1
U6	PR38C	3	PCLKT3_1	PR50C	3	PCLKT3_1
T4	PR38B	3	PCLKC3_0	PR50B	3	PCLKC3_0
T3	PR38A	3	PCLKT3_0	PR50A	3	PCLKT3_0
U9	PR36D	2	PCLKC2_2	PR48D	2	PCLKC2_2
T9	PR36C	2	PCLKT2_2	PR48C	2	PCLKT2_2
R2	PR36B	2	PCLKC2_0	PR48B	2	PCLKC2_0
P2	PR36A	2	PCLKT2_0	PR48A	2	PCLKT2_0
T11	PR35D	2	PCLKC2_3	PR47D	2	PCLKC2_3
U11	PR35C	2	PCLKT2_3	PR47C	2	PCLKT2_3
R4	PR35B	2	PCLKC2_1	PR47B	2	PCLKC2_1
R3	PR35A	2	PCLKT2_1	PR47A	2	PCLKT2_1
T8	PR34D	2		PR46D	2	
R8	PR34C	2		PR46C	2	
P1	PR34B	2		PR46B	2	
N1	PR34A	2		PR46A	2	
R6	PR31D	2		PR43D	2	
P6	PR31C	2		PR43C	2	
M1	PR31B	2		PR43B	2	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E24	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
F24	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
A23	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L25	VCC12	-		VCC12	-	
B23	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-		B_VDDOB1_L	-	
B24	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-		B_VDDOB0_L	-	
A24	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
K25	VCC12	-		VCC12	-	
F25	B_HDINN0_L	-	PCS 361 CH 0 IN N	B_HDINN0_L	-	PCS 361 CH 0 IN N
E25	B_HDINP0_L	-	PCS 361 CH 0 IN P	B_HDINP0_L	-	PCS 361 CH 0 IN P
D28	B_VDDIB0_L	-		B_VDDIB0_L	-	
G25	VCC12	-		VCC12	-	
D29	A_VDDIB3_L	-		A_VDDIB3_L	-	
C25	VCC12	-		VCC12	-	
A25	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
B25	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
E27	VCC12	-		VCC12	-	
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
F26	A_VDDOB3_L	-		A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
F27	A_VDDOB2_L	-		A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E28	VCC12	-		VCC12	-	
B28	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
A28	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
D30	A_VDDIB2_L	-		A_VDDIB2_L	-	
C28	VCC12	-		VCC12	-	
D31	A_VDDIB1_L	-		A_VDDIB1_L	-	
C29	VCC12	-		VCC12	-	
A29	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
B29	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A30	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
E29	VCC12	-		VCC12	-	
B30	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
F28	A_VDDOB1_L	-		A_VDDOB1_L	-	
B31	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
F29	A_VDDOB0_L	-		A_VDDOB0_L	-	
A31	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E30	VCC12	-		VCC12	-	
B32	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
A32	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
D32	A_VDDIB0_L	-		A_VDDIB0_L	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP20	PB61B	5	
AH21	PB61C	5	
AH20	PB61D	5	
AM20	PB63A	5	
AM19	PB63B	5	
AJ21	PB63C	5	
AJ20	PB63D	5	
AK19	PB66A	5	
AK18	PB66B	5	
AE18	PB66C	5	
AD18	PB66D	5	
AN19	PB69A	5	
AN18	PB69B	5	
AG18	PB69C	5	
AF18	PB69D	5	
AP19	PB71A	5	
AP18	PB71B	5	
AJ18	PB71C	5	
AH18	PB71D	5	
AP17	PB73A	4	
AP16	PB73B	4	
AJ17	PB73C	4	
AH17	PB73D	4	
AN17	PB75A	4	
AN16	PB75B	4	
AE17	PB75C	4	
AD17	PB75D	4	
AK17	PB78A	4	
AK16	PB78B	4	
AG17	PB78C	4	
AF17	PB78D	4	
AM16	PB81A	4	
AM15	PB81B	4	
AJ15	PB81C	4	
AJ14	PB81D	4	
AL16	PB83A	4	
AL15	PB83B	4	
AG16	PB83C	4	
AF16	PB83D	4	
AP15	PB86A	4	
AP14	PB86B	4	
AH15	PB86C	4	
AH14	PB86D	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AE1	PR74A	3		PR88A	3	
AF12	PR73D	3		PR87D	3	
AE12	PR73C	3		PR87C	3	
AF2	PR73B	3		PR87B	3	
AE2	PR73A	3		PR87A	3	
AF11	PR72D	3		PR86D	3	
AE11	PR72C	3		PR86C	3	
AF5	PR72B	3		PR86B	3	
AE5	PR72A	3		PR86A	3	
AF10	PR69D	3		PR83D	3	
AE10	PR69C	3		PR83C	3	
AD1	PR69B	3		PR83B	3	
AC1	PR69A	3		PR83A	3	
AF9	PR68D	3		PR82D	3	
AE9	PR68C	3		PR82C	3	
AD2	PR68B	3		PR82B	3	
AC2	PR68A	3		PR82A	3	
AF6	PR67D	3		PR81D	3	
AE6	PR67C	3		PR81C	3	
AD3	PR67B	3		PR81B	3	
AC3	PR67A	3		PR81A	3	
AE8	PR65D	3		PR79D	3	
AD8	PR65C	3		PR79C	3	
AD4	PR65B	3		PR79B	3	
AC4	PR65A	3		PR79A	3	
AE7	PR64D	3		PR78D	3	
AD7	PR64C	3		PR78C	3	
AD5	PR64B	3		PR78B	3	
AC5	PR64A	3		PR78A	3	
AD6	PR63D	3		PR77D	3	
AC6	PR63C	3		PR77C	3	
AB1	PR63B	3		PR77B	3	
AA1	PR63A	3		PR77A	3	
AD9	PR61D	3		PR75D	3	
AC9	PR61C	3		PR75C	3	
AB2	PR61B	3		PR75B	3	
AA2	PR61A	3		PR75A	3	
AD14	PR60D	3		PR74D	3	
AC14	PR60C	3		PR74C	3	
AB5	PR60B	3		PR74B	3	
AA5	PR60A	3		PR74A	3	
AD10	PR59D	3		PR73D	3	
AC10	PR59C	3		PR73C	3	
Y1	PR59B	3		PR73B	3	
W1	PR59A	3		PR73A	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C3	GND	-		GND	-	
C30	GND	-		GND	-	
C33	GND	-		GND	-	
C35	GND	-		GND	-	
C36	GND	-		GND	-	
C39	GND	-		GND	-	
C4	GND	-		GND	-	
C40	GND	-		GND	-	
C7	GND	-		GND	-	
C8	GND	-		GND	-	
D15	GND	-		GND	-	
D21	GND	-		GND	-	
D25	GND	-		GND	-	
D31	GND	-		GND	-	
F4	GND	-		GND	-	
F40	GND	-		GND	-	
G11	GND	-		GND	-	
G17	GND	-		GND	-	
G26	GND	-		GND	-	
G32	GND	-		GND	-	
H14	GND	-		GND	-	
H20	GND	-		GND	-	
H23	GND	-		GND	-	
H29	GND	-		GND	-	
H35	GND	-		GND	-	
H8	GND	-		GND	-	
J3	GND	-		GND	-	
J39	GND	-		GND	-	
L16	GND	-		GND	-	
L27	GND	-		GND	-	
L36	GND	-		GND	-	
L7	GND	-		GND	-	
M19	GND	-		GND	-	
M24	GND	-		GND	-	
M4	GND	-		GND	-	
M40	GND	-		GND	-	
N12	GND	-		GND	-	
N31	GND	-		GND	-	
P35	GND	-		GND	-	
P8	GND	-		GND	-	
R15	GND	-		GND	-	
R28	GND	-		GND	-	
R3	GND	-		GND	-	
R39	GND	-		GND	-	
T11	GND	-		GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
V21	VCC	-		VCC	-	
V22	VCC	-		VCC	-	
V23	VCC	-		VCC	-	
V25	VCC	-		VCC	-	
V27	VCC	-		VCC	-	
W17	VCC	-		VCC	-	
W19	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
W22	VCC	-		VCC	-	
W24	VCC	-		VCC	-	
W26	VCC	-		VCC	-	
Y16	VCC	-		VCC	-	
Y18	VCC	-		VCC	-	
Y20	VCC	-		VCC	-	
Y23	VCC	-		VCC	-	
Y25	VCC	-		VCC	-	
Y27	VCC	-		VCC	-	
AG22	VCC12	-		VCC12	-	
AG26	VCC12	-		VCC12	-	
T17	VCC12	-		VCC12	-	
T21	VCC12	-		VCC12	-	
T22	VCC12	-		VCC12	-	
T26	VCC12	-		VCC12	-	
U16	VCC12	-		VCC12	-	
U27	VCC12	-		VCC12	-	
AC15	VCCAUX	-		VCCAUX	-	
AC28	VCCAUX	-		VCCAUX	-	
AD15	VCCAUX	-		VCCAUX	-	
AD28	VCCAUX	-		VCCAUX	-	
AE15	VCCAUX	-		VCCAUX	-	
AE28	VCCAUX	-		VCCAUX	-	
AF15	VCCAUX	-		VCCAUX	-	
AF28	VCCAUX	-		VCCAUX	-	
AG15	VCCAUX	-		VCCAUX	-	
AG28	VCCAUX	-		VCCAUX	-	
AH14	VCCAUX	-		VCCAUX	-	
AH16	VCCAUX	-		VCCAUX	-	
AH17	VCCAUX	-		VCCAUX	-	
AH18	VCCAUX	-		VCCAUX	-	
AH19	VCCAUX	-		VCCAUX	-	
AH20	VCCAUX	-		VCCAUX	-	
AH23	VCCAUX	-		VCCAUX	-	
AH24	VCCAUX	-		VCCAUX	-	
AH25	VCCAUX	-		VCCAUX	-	
AH26	VCCAUX	-		VCCAUX	-	

Date	Version	Section	Change Summary
September 2007	01.7	Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.
November 2007	01.8	Ordering Information	Removed -7 speed grade information for 115K LUT devices in the Ordering Information tables.
January 2008	01.9	Introduction	Corrections/Additions to memory controller list (Tables 1-2).
		Architecture	AIL Overview – Modified power used by AIL block.
			PURESPEED I/O Buffer Banks – Modified VTT termination info. Added info about complimentary drivers for all banks.
			Supported Source Synchronous Interfaces – Modified data for DDRII in Table 2-11.
		DC and Switching Characteristics	Recommended Operating Conditions – Changed footnote 3.
			Initialization and Standby Supply Current – Inserted a paragraph with info regarding the table. Also updated the table.
			Typical Building Block Function Performance – Added VCC=1.2V=1.2V+/-5% above Pin to Pin Performance table.
			LatticeSC External Switching Characteristics – Added VCC=1.2V=1.2V+/-5% above table. Reworded footnote 3.
			LatticeSC Family Timing Adders – Added VCC=1.2V=1.2V+/-5% above table.
			LatticeSC Internal Timing Parameters – Added VCC=1.2V=1.2V+/-5% above table. Reworded footnote 1.
			GSR Timing – Added a new table for Internal System Bus Timing after GSR Timing.
			LatticeSC sysCONFIG Port Timing – Corrected sysCONFIG SPI Port information.
		Pinout Information	Signal Descriptions – Modified info for VTT_x, PROBE_VCC, and PROBE_GND. Modified info for [LOC]_DLL[T,C]_IN[C,D,E,F].
		Supplemental Information	Updated list of technical notes, added reference to LatticeSC/M flexiPCS Data Sheet.
March 2008	02.0	DC and Switching Characteristics	Updated Internal Timing Parameters table.
			Updated Read Mode timing diagram.
			Updated Read Mode with Input Registers Only timing diagram.
June 2008	02.1	—	Data sheet status changed from preliminary to final.
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
		DC and Switching Characteristics	Updated LatticeSC/M External Switching Characteristics table.
			Updated LatticeSC/M Internal Timing Parameters table.
			Removed Read-Before-Write sysMEM EBR mode.
December 2008	02.2	Architecture	Output/Tristate DDR/Shift Register Block Diagram - corrected connection to POS.
		DC and Switching Characteristics	DC and Switching Characteristics table - updated data for $t_{SUI\_PIO.}$
			Added $T_{R,}$ T_F parameter to PURESPEED I/O Differential Electrical Characteristics (LVDS) table.
		Multiple	Removed references to HyperTransport throughout the data sheet.
January 2010	02.3	Introduction	Updated per PCN #01A-10 (ceramic fcBGA conversion to organic fcBGA for the 1152-ball and 1704-ball fcBGA packages) and PCN #02A-10 (1020-ball organic fcBGA conversion to 1020-ball organic fcBGA revision 2 package).
		Ordering Information	