Lattice Semiconductor Corporation - LFSC3GA15E-5F256C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3750
Number of Logic Elements/Cells	15000
Total RAM Bits	1054720
Number of I/O	139
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga15e-5f256c

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR 16x2 x 4 DPR 16x2 x 2	ROM 16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR 16x4 x 2 DPR 16x4 x 1	ROM 16x2 x 4
LUT 6x2 or MUX 8x1 x 2	2-bit Counter x 4	SPR 16x8 x 1	ROM 16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM 16x8 x1

Routing

There are many resources provided in the LatticeSC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

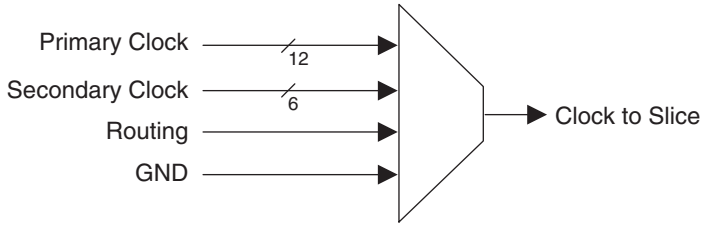
The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU) resources. The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. All connections are buffered to ensure high-speed operation even with long high-fanout connections.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Network

The LatticeSC devices have three distinct clock networks for use in distributing high-performance clocks within the device: primary clocks, secondary clocks and edge clocks. In addition to these dedicated clock networks, users are free to route clocks within the device using the general purpose routing. Figure 2-4 shows the clock resources available to each slice.

Figure 2-4. Slice Clock Selection



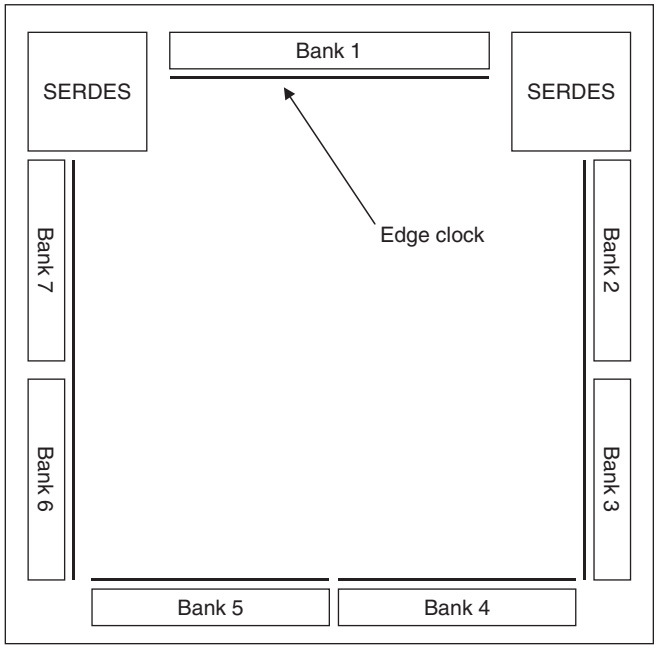
Note: GND is available to switch off the network.

Primary Clock Sources

LatticeSC devices have a wide variety of primary clock sources available. Primary clocks sources consists of the following:

- Primary clock input pins
- Edge clock input pins
- Two outputs per DLL

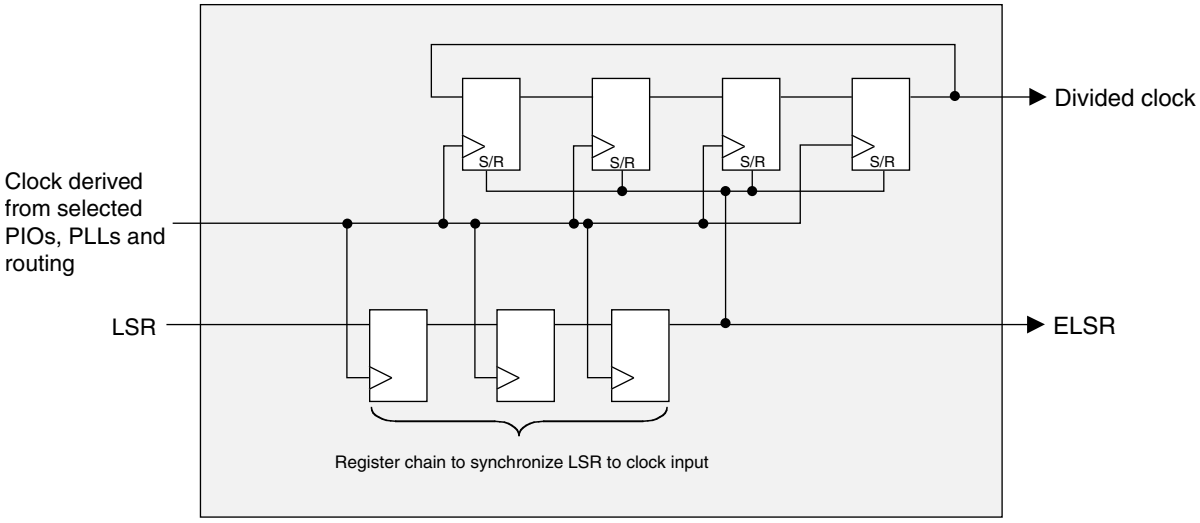
Figure 2-7. Edge Clock Resources



Precision Clock Divider

Each set of edge clocks has four high-speed dividers associated with it. These are intended for generating a slower speed system clock from the high-speed edge clock. The block operates in a DIV2 or DIV4 mode and maintains a known phase relationship between the divided down clock and high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PIOs, PLLs and routing. The clock divider outputs serve as primary clock sources. This circuit also generates an edge local set/reset (ELSR) signal which is fed to the PIOs via the edge clock network and is used for the rest of the I/O gearing logic.

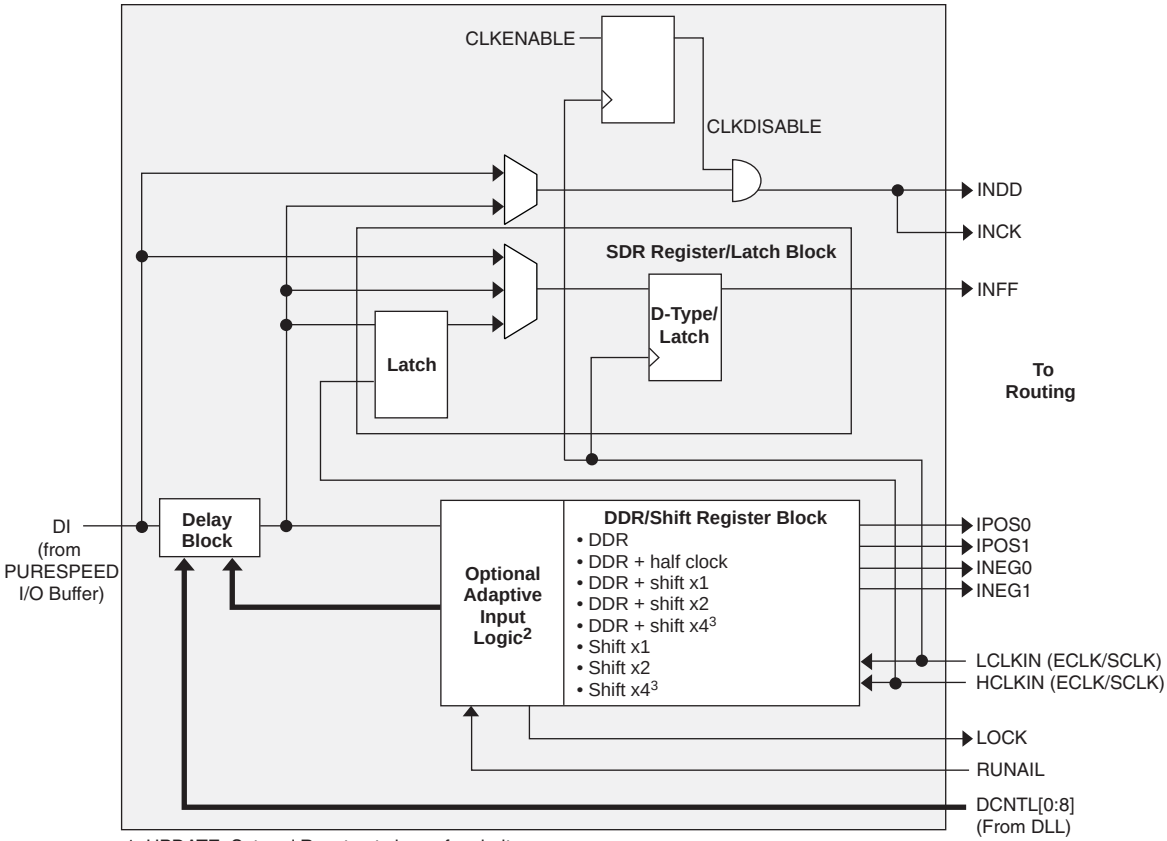
Figure 2-8. Clock Divider Circuit



Dynamic Clock Select (DCS)

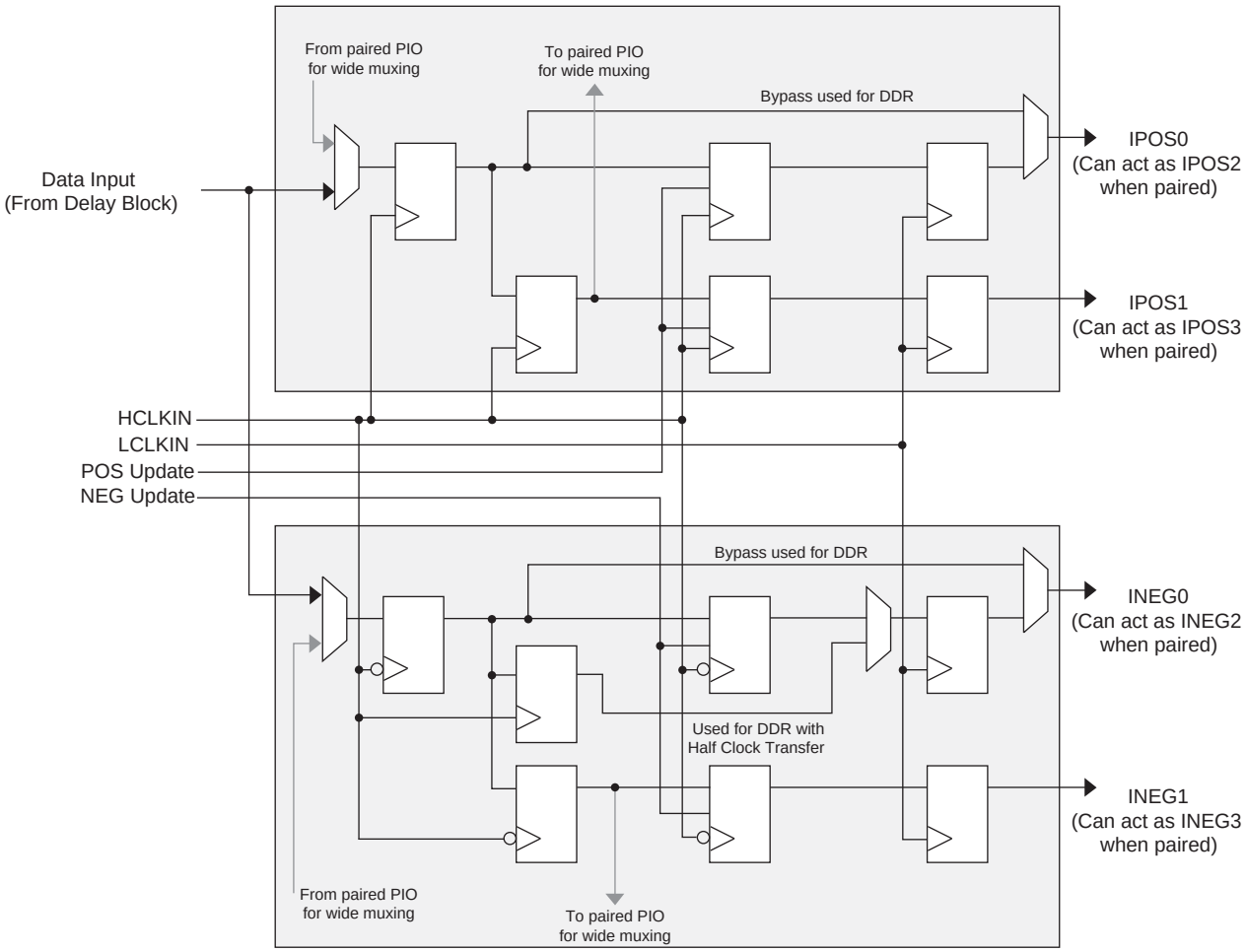
The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is

Figure 2-20. Input Register Block[1]



1. UPDATE, Set and Reset not shown for clarity
2. Adaptive input logic is only available in selected PIO
3. By four shift modes utilize DDR/shift register block from paired PIO.
4. CLKDISABLE is used to block the transitions on the DQS pin during post-amble. Its main use is to disable DQS (typically found in DDR memory interfaces) or other clock signals. It can also be used to disable any/all input signals to save power.

Figure 2-21. Input DDR/Shift Register Block



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the PURESPEED I/O buffers. The block contains a register for SDR operation and a group of registers for DDR and shift register operation. The output signal (DO) can be derived directly from one of the inputs (bypass mode), the SDR register or the DDR/shift register block. Figure 2-22 shows the diagram of the Output Register Block.

Output SDR Register/Latch Block

The SDR register operates on the positive edge of the high-speed clock. It has clock enable that is driven by the clock enable output signal generated by the control MUX. In addition it has a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register LSR input is driven from LSRO, which is generated from the PIO control MUX. The GSR inputs is driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Output DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer from the low-speed clock domain. It functions as a gearbox allowing low-speed parallel data from the FPGA fabric be output as a higher speed serial stream. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. Figure 2-22 shows a simplified block diagram of the shift register block.

3. **Bottom Side (Banks 4 and 5)**
   These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but true HLVDS and RSDS differential drivers are not available. Adaptive input logic is available on PIOs A or C.

Table 2-8 lists the standards supported by each side.

Table 2-8. I/O Standards Supported by Different Banks

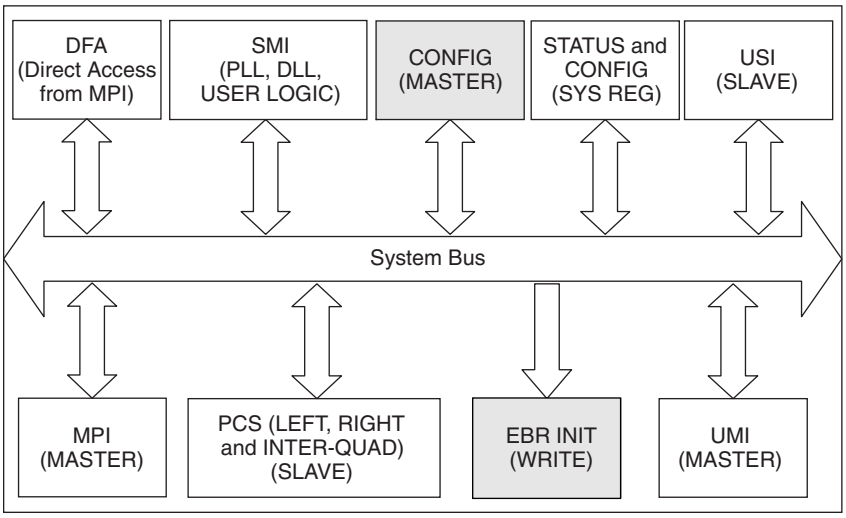
Description	Top Side Banks 1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
I/O Buffer Type	Single-ended, Differential Receiver	Single-ended, Differential Receiver and Driver	Single-ended, Differential Receiver	Single-ended, Differential Receiver and Driver
Output Standards Supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II SSTL33_ I, II HSTL15_I, II, III[1], IV[1] HSTL18_I, II,III[1], IV[1] SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL[2], GTL+[2]	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II HSTL15_I,III HSTL18_I,II,III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL[2], GTL+[2]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II SSTL33_ I, II HSTL15_I, II, III[1], IV[1] HSTL18_I, II,III[1], IV[1] SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL[2], GTL+[2]	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II HSTL15_I,III HSTL18_I,II,III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL[2], GTL+[2]
Input Standards Supported	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Clock Inputs	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Differential Output Support via Emulation	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL
AIL Support	No	Yes	Yes	Yes

1. Input only.
2. Input only. Outputs supported by bussing multiple outputs together.

Supported Standards

The LatticeSC PURESPEED I/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 12, 15, 18, 25 and 33 standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, termination resistance, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL, HSTL, GTL (input only), GTL+ (input only), PCI33, PCIX33, PCIX15, AGP-1X33 and AGP-2X33. Differential standards supported include LVDS, RSDS, BLVDS, MLVDS, LVPECL, differential SSTL and differential HSTL. Tables 12 and 13 show the I/O standards (together with their supply and reference voltages) supported by the LatticeSC devices. The tables also provide the available internal termination schemes. For further information on utilizing the PURESPEED I/O buffer to support a variety of standards please see details of additional technical documentation at the end of this data sheet.

Figure 2-31. LatticeSC System Bus Interfaces



Several interfaces exist between the System Bus and other FPGA elements. The MPI interface acts as a bridge between the external microprocessor bus and System Bus. The MPI may work in an independent clock domain from the System Bus if the System Bus clock is not sourced from the external microprocessor clock. Pipelined operation allows high-speed memory interface to the EBR and peripheral access without the requirement for additional cycles on the bus. Burst transfers allow optimal use of the memory interface by giving advance information of the nature of the transfers.

Details for the majority of the peripherals can be found in the associated technical documentation, see details at the end of this data sheet. Additional details of the MPI are provided below.

Microprocessor Interface (MPI)

The LatticeSC family devices have a dedicated synchronous MPI function block. The MPI is programmable to operate with PowerPC/PowerQUICC MPC860/MPC8260 series microprocessors. The MPI implements an 8-, 16-, or 32-bit interface with 1-bit, 2-bit, or 4-bit parity to the host processor (PowerPC) that can be used for configuration and read-back of the FPGA as well as for user-defined data processing and general monitoring of FPGA functions.

The control portion of the MPI is available following power-up of the FPGA if the mode pins specify MPI mode, even if the FPGA is not yet configured. The width of the data port is selectable among 8-, 16-, or 32-bit and the parity bus can be 1-, 2-, or 4-bit. In configuration mode the data and parity bus width are related to the state of the M[0:3] mode pins. For post-configuration use, the MPI must be included in the configuration bit stream by using an MPI library element in your design from the ispLEVER primitive library, or by setting the bit of the MPI configuration control register prior to the start of configuration. The user can also enable and disable the parity bus through the configuration bit stream. These pads can be used as general I/O when they are not needed for MPI use.

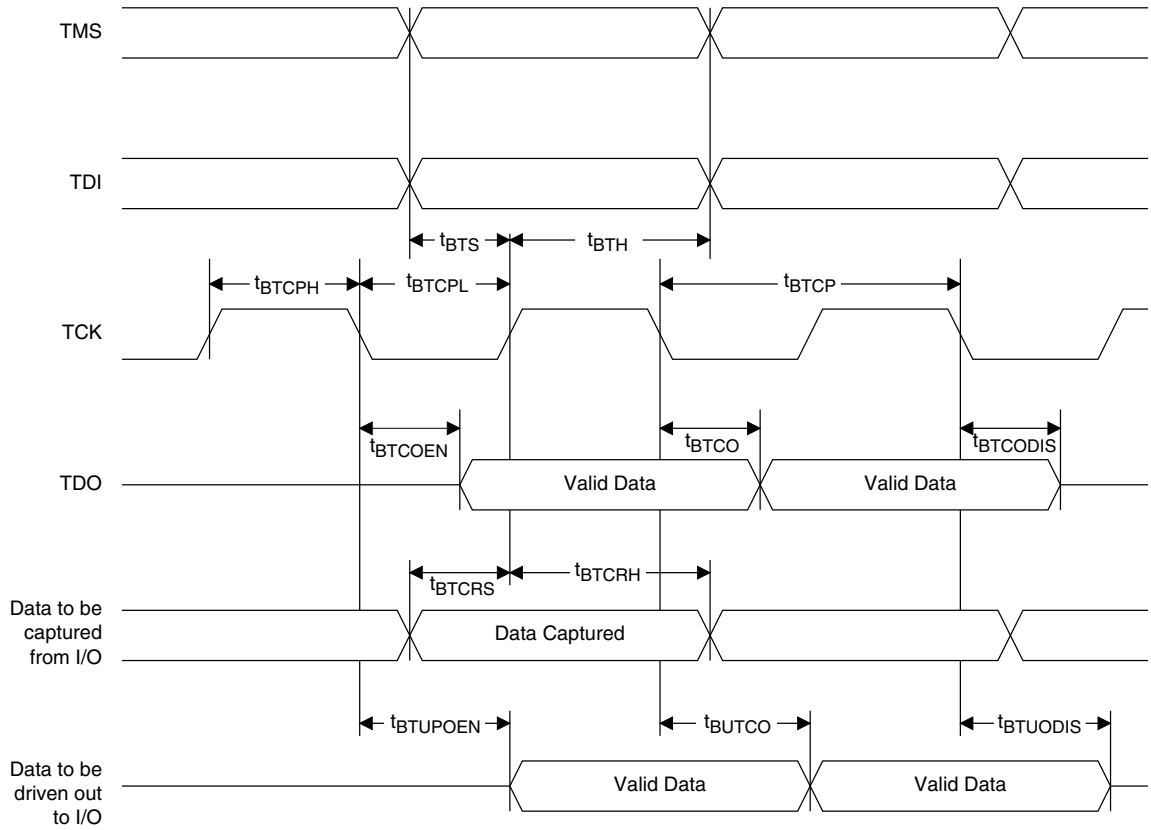
The MPI block also provides the capability to interface directly to the FPGA fabric with a databus after configuration.The bus protocol is still handled by the MPI block but the direct FPGA access allows high-speed block data transfers such as DMA transactions. Figure 2-32 shows one of the ways a PowerPC is connected to MPI.

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	10	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	10	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	25	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	25	ns

Figure 3-14. JTAG Port Timing Waveforms



Signal Descriptions (Cont.)

Signal Name	I/O	Description
PROBE_GND	—	GND signal - Connected to internal VSS node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.
PLL and Clock Functions (Used as user-programmable I/O pins when not in use for PLL, DLL or clock pins.)		
[LOC]_PLL[T, C]_FB_[A/B]	I	PLL feedback input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the PLL is located in: ULC (upper left), URC (upper right), LLC (lower left) and LRC (lower right). [T, C] indicates whether input is true or complement. [A, B] indicates PLL reference within the corner.
[LOC]_DLL[T, C]_FB_[C, D, E, F]	I	DLL feedback input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the DLL is located in: ULC (upper left), URC (upper right), LLC (lower left) and LRC (lower right). [T/C] indicates whether input is true or complement. [C, D, E, F] indicates DLL reference within a corner. Note: E and F are only available on the lower corners.
[LOC]_PLL[T, C]_IN[A/B]	I	PLL reference clock input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the PLL is located in: ULC (upper left corner), URC (upper right corner), LLC (lower left corner) and LRC (lower right corner). [T, C] indicates whether input is true or complement.[A, B] indicates PLL reference within the corner.
[LOC]_DLL[T, C]_IN[C, D, E, F]		DLL reference clock inputs. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the DLL is located in: ULC (upper left corner), URC (upper right corner), LLC (lower left corner) and LRC (lower right corner). [T/C] indicates whether input is true or complement. [C, D, E, F] indicates DLL reference within a corner. Note: E and F are only available on the lower corners. PCKLxy_[0:3] can drive primary clocks, edge clocks, and CLKDIVs. PCLKxy_[4:7] can only drive edge clocks.
PCLKxy_z		General clock inputs. x indicates whether T (true) or C (complement). y indicates the I/O bank the clock is associated with. z indicates the clock number within a bank.
Test and Programming (Dedicated pins. Pull-up is enabled on input pins during configuration.)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence).
TDO	O	Output pin -Test Data out pin used to shift data out of device using 1149.1.
Configuration Pads (Dedicated pins. Used during sysCONFIG.)		
M[3:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN.
INITN	I/O	Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled that will pull the I/O above 1.5V.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G1	NC	-		PL20B	7	
M4	NC	-		NC	-	
J3	NC	-		NC	-	
P5	NC	-		NC	-	
W5	NC	-		PL48C	6	
T6	NC	-		PL35C	6	
U3	NC	-		PL36A	6	
V3	NC	-		PL36B	6	
T5	NC	-		PL39A	6	
T4	NC	-		PL39B	6	
V5	NC	-		PL43C	6	
U6	NC	-		PL42C	6	
U4	NC	-		PL40A	6	
U5	NC	-		PL40B	6	
V4	NC	-		PL43D	6	
Y2	NC	-		PL47A	6	
AA2	NC	-		PL47B	6	
W3	NC	-		PL47D	6	
Y3	NC	-		PL47C	6	
AB3	NC	-		NC	-	
AC4	NC	-		PL53A	6	
AD4	NC	-		PL53B	6	
AE3	NC	-		PL56A	6	
AF3	NC	-		PL56B	6	
AF7	NC	-		PB7A	5	
AF6	NC	-		PB7B	5	
AH4	NC	-		PB8A	5	
AG5	NC	-		PB8B	5	
AF8	NC	-		PB9A	5	
AG8	NC	-		PB9B	5	
AG7	NC	-		NC	-	
AG10	NC	-		NC	-	
AF12	NC	-		NC	-	
AH7	NC	-		PB15A	5	
AE13	NC	-		PB15D	5	
AG13	NC	-		PB23C	5	
AH8	NC	-		PB15B	5	
AJ5	NC	-		PB17A	5	
AJ6	NC	-		PB17B	5	
AF15	NC	-		PB21D	5	
AJ7	NC	-		PB19A	5	
AJ8	NC	-		PB19B	5	
AE12	NC	-		PB15C	5	
AF16	NC	-		PB38D	4	
AF19	NC	-		PB49D	4	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB10	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
J10	VCC	-		VCC	-	
J21	VCC	-		VCC	-	
K10	VCC	-		VCC	-	
K11	VCC	-		VCC	-	
K12	VCC	-		VCC	-	
K13	VCC	-		VCC	-	
K14	VCC	-		VCC	-	
K17	VCC	-		VCC	-	
K18	VCC	-		VCC	-	
K19	VCC	-		VCC	-	
K20	VCC	-		VCC	-	
K21	VCC	-		VCC	-	
K22	VCC	-		VCC	-	
K9	VCC	-		VCC	-	
L10	VCC	-		VCC	-	
L21	VCC	-		VCC	-	
M10	VCC	-		VCC	-	
M21	VCC	-		VCC	-	
N10	VCC	-		VCC	-	
N21	VCC	-		VCC	-	
P10	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
U10	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V10	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W10	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y10	VCC	-		VCC	-	
Y21	VCC	-		VCC	-	
H11	VCCAUX	-		VCCAUX	-	
H12	VCCAUX	-		VCCAUX	-	
H19	VCCAUX	-		VCCAUX	-	
H20	VCCAUX	-		VCCAUX	-	
M23	VCCAUX	-		VCCAUX	-	
M24	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
N24	VCCAUX	-		VCCAUX	-	
U23	VCCAUX	-		VCCAUX	-	
U24	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	
V24	VCCAUX	-		VCCAUX	-	
W23	VCCAUX	-		VCCAUX	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P22	VCCIO2	-		VCCIO2	-	
R22	VCCIO2	-		VCCIO2	-	
AA23	VCCIO3	-		VCCIO3	-	
AA24	VCCIO3	-		VCCIO3	-	
AB23	VCCIO3	-		VCCIO3	-	
AB24	VCCIO3	-		VCCIO3	-	
T22	VCCIO3	-		VCCIO3	-	
U22	VCCIO3	-		VCCIO3	-	
V22	VCCIO3	-		VCCIO3	-	
W22	VCCIO3	-		VCCIO3	-	
Y22	VCCIO3	-		VCCIO3	-	
Y23	VCCIO3	-		VCCIO3	-	
Y24	VCCIO3	-		VCCIO3	-	
AB16	VCCIO4	-		VCCIO4	-	
AB17	VCCIO4	-		VCCIO4	-	
AB18	VCCIO4	-		VCCIO4	-	
AB19	VCCIO4	-		VCCIO4	-	
AB20	VCCIO4	-		VCCIO4	-	
AC20	VCCIO4	-		VCCIO4	-	
AC21	VCCIO4	-		VCCIO4	-	
AC22	VCCIO4	-		VCCIO4	-	
AD20	VCCIO4	-		VCCIO4	-	
AD21	VCCIO4	-		VCCIO4	-	
AD22	VCCIO4	-		VCCIO4	-	
AB11	VCCIO5	-		VCCIO5	-	
AB12	VCCIO5	-		VCCIO5	-	
AB13	VCCIO5	-		VCCIO5	-	
AB14	VCCIO5	-		VCCIO5	-	
AB15	VCCIO5	-		VCCIO5	-	
AC10	VCCIO5	-		VCCIO5	-	
AC11	VCCIO5	-		VCCIO5	-	
AC9	VCCIO5	-		VCCIO5	-	
AD10	VCCIO5	-		VCCIO5	-	
AD11	VCCIO5	-		VCCIO5	-	
AD9	VCCIO5	-		VCCIO5	-	
AA7	VCCIO6	-		VCCIO6	-	
AA8	VCCIO6	-		VCCIO6	-	
AB7	VCCIO6	-		VCCIO6	-	
AB8	VCCIO6	-		VCCIO6	-	
T9	VCCIO6	-		VCCIO6	-	
U9	VCCIO6	-		VCCIO6	-	
V9	VCCIO6	-		VCCIO6	-	
W9	VCCIO6	-		VCCIO6	-	
Y7	VCCIO6	-		VCCIO6	-	
Y8	VCCIO6	-		VCCIO6	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y24	PL48C	6		PL61C	6	
Y23	PL48D	6		PL61D	6	
AD29	PL49A	6		PL62A	6	
AD30	PL49B	6		PL62B	6	
AF28	PL49C	6		PL62C	6	
AE28	PL49D	6		PL62D	6	
AC28	PL51A	6		PL65A	6	
AD28	PL51B	6		PL65B	6	
AB26	PL51C	6		PL65C	6	
AC26	PL51D	6	VREF2_6	PL65D	6	VREF2_6
AC32	PL52A	6		PL66A	6	
AD32	PL52B	6		PL66B	6	
AA24	PL52C	6		PL66C	6	
AA23	PL52D	6		PL66D	6	
AE30	PL53A	6		PL67A	6	
AE29	PL53B	6		PL67B	6	
AC25	PL53C	6		PL67C	6	
AB25	PL53D	6		PL67D	6	
AE31	PL55A	6		PL69A	6	
AE32	PL55B	6		PL69B	6	
AE26	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AE27	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF32	PL56A	6		PL70A	6	
AF31	PL56B	6		PL70B	6	
AC24	PL56C	6		PL70C	6	
AD25	PL56D	6		PL70D	6	
AG32	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG31	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC23	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AD24	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AH32	XRES	-		XRES	-	
AH31	TEMP	6		TEMP	6	
AJ32	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AK32	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AF27	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AG28	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AK31	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AL31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AE25	PB4C	5		PB4C	5	
AE24	PB4D	5		PB4D	5	
AK30	PB5A	5		PB5A	5	
AL30	PB5B	5		PB5B	5	
AD23	PB5C	5		PB5C	5	
AE23	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AK29	PB7A	5		PB7A	5	
AL29	PB7B	5		PB7B	5	
AF26	PB7C	5		PB7C	5	
AF25	PB7D	5		PB7D	5	
AJ28	PB8A	5		PB8A	5	
AK28	PB8B	5		PB8B	5	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM21	PB29A	5		PB38A	5	
AM20	PB29B	5		PB38B	5	
AH21	PB29C	5		PB38C	5	
AH20	PB29D	5		PB38D	5	
AJ18	PB31A	5		PB39A	5	
AK18	PB31B	5		PB39B	5	
AH19	PB31C	5		PB39C	5	
AH18	PB31D	5		PB39D	5	
AL19	PB32A	5		PB41A	5	
AM19	PB32B	5		PB41B	5	
AH17	PB32C	5		PB41C	5	
AG17	PB32D	5		PB41D	5	
AL18	PB33A	5		PB42A	5	
AM18	PB33B	5		PB42B	5	
AC17	PB33C	5		PB42C	5	
AD17	PB33D	5		PB42D	5	
AL17	PB35A	5		PB43A	5	
AM17	PB35B	5		PB43B	5	
AE17	PB35C	5		PB43C	5	
AF17	PB35D	5		PB43D	5	
AM16	PB37A	4		PB45A	4	
AL16	PB37B	4		PB45B	4	
AF16	PB37C	4		PB45C	4	
AE16	PB37D	4		PB45D	4	
AM15	PB38A	4		PB46A	4	
AL15	PB38B	4		PB46B	4	
AD16	PB38C	4		PB46C	4	
AC16	PB38D	4		PB46D	4	
AM14	PB39A	4		PB47A	4	
AL14	PB39B	4		PB47B	4	
AG16	PB39C	4		PB47C	4	
AH16	PB39D	4		PB47D	4	
AK15	PB41A	4		PB49A	4	
AJ15	PB41B	4		PB49B	4	
AH15	PB41C	4		PB49C	4	
AH14	PB41D	4		PB49D	4	
AM13	PB42A	4		PB50A	4	
AM12	PB42B	4		PB50B	4	
AH13	PB42C	4		PB50C	4	
AH12	PB42D	4		PB50D	4	
AK14	PB43A	4		PB51A	4	
AJ14	PB43B	4		PB51B	4	
AE15	PB43C	4		PB51C	4	
AD15	PB43D	4		PB51D	4	
AL13	PB46A	4	PCLKT4_2	PB53A	4	PCLKT4_2
AL12	PB46B	4	PCLKC4_2	PB53B	4	PCLKC4_2
AG14	PB46C	4	PCLKT4_7	PB53C	4	PCLKT4_7
AG13	PB46D	4	PCLKC4_7	PB53D	4	PCLKC4_7
AM11	PB47A	4	PCLKT4_1	PB54A	4	PCLKT4_1
AM10	PB47B	4	PCLKC4_1	PB54B	4	PCLKC4_1

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G6	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
A6	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
D6	A_VDDOB2_R	-		A_VDDOB2_R	-	
B6	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
D7	A_VDDOB3_R	-		A_VDDOB3_R	-	
B7	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
A7	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
G7	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
F7	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
H7	A_VDDIB3_R	-		A_VDDIB3_R	-	
H8	B_VDDIB0_R	-		B_VDDIB0_R	-	
F8	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
G8	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
A8	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D8	B_VDDOB0_R	-		B_VDDOB0_R	-	
B8	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D9	B_VDDOB1_R	-		B_VDDOB1_R	-	
B9	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
A9	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
H10	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
G10	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
H9	B_VDDIB1_R	-		B_VDDIB1_R	-	
H11	B_VDDIB2_R	-		B_VDDIB2_R	-	
F11	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
G11	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
A11	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D11	B_VDDOB2_R	-		B_VDDOB2_R	-	
B11	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D12	B_VDDOB3_R	-		B_VDDOB3_R	-	
B12	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
A12	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
G12	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
F12	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
H12	B_VDDIB3_R	-		B_VDDIB3_R	-	
B10	VCC12	-		VCC12	-	
D10	B_REFCLKN_R	-		B_REFCLKN_R	-	
C10	B_REFCLKP_R	-		B_REFCLKP_R	-	
J15	PT49D	1	HDC/SI	PT61D	1	HDC/SI
K15	PT49C	1	LDCN/SCS	PT61C	1	LDCN/SCS
E13	PT49B	1	D8/MPI_DATA8	PT59B	1	D8/MPI_DATA8
F13	PT49A	1	CS1/MPI_CS1	PT59A	1	CS1/MPI_CS1
H13	PT47D	1	D9/MPI_DATA9	PT58D	1	D9/MPI_DATA9
G13	PT47C	1	D10/MPI_DATA10	PT58C	1	D10/MPI_DATA10
E14	PT47B	1	CS0N/MPI_CS0N	PT57B	1	CS0N/MPI_CS0N
F14	PT47A	1	RDN/MPI_STRB_N	PT57A	1	RDN/MPI_STRB_N
H14	PT46D	1	WRN/MPI_WR_N	PT55D	1	WRN/MPI_WR_N
G14	PT46C	1	D7/MPI_DATA7	PT55C	1	D7/MPI_DATA7
D13	PT46B	1	D6/MPI_DATA6	PT55B	1	D6/MPI_DATA6
D14	PT46A	1	D5/MPI_DATA5	PT55A	1	D5/MPI_DATA5
E15	PT45D	1	D4/MPI_DATA4	PT54D	1	D4/MPI_DATA4

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B30	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
D30	A_VDDOB0_L	-		A_VDDOB0_L	-	
A30	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
C31	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
C32	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
B31	A_VDDIB0_L	-		A_VDDIB0_L	-	
AL25	NC	-		PB26A	5	
AL24	NC	-		PB26B	5	
AG27	NC	-		PB26C	5	
AH27	NC	-		PB26D	5	
AM25	NC	-		PB27A	5	
AM24	NC	-		PB27B	5	
AL9	NC	-		PB62A	4	
AL8	NC	-		PB62B	4	
AK9	NC	-		PB63A	4	
AJ9	NC	-		PB63B	4	
AG10	NC	-		PB63C	4	
AG11	NC	-		PB63D	4	
J30	NC	-		PL26A	7	
H30	NC	-		PL26B	7	
M28	NC	-		PL26C	7	
N28	NC	-		PL26D	7	
J32	NC	-		PL27A	7	
J31	NC	-		PL27B	7	
N26	NC	-		PL27C	7	
N27	NC	-		PL27D	7	
K31	NC	-		PL29A	7	
K32	NC	-		PL29B	7	
P25	NC	-		PL29C	7	
P26	NC	-		PL29D	7	
L27	NC	-		PL22C	7	
L28	NC	-		PL22D	7	
M29	NC	-		PL30A	7	
L29	NC	-		PL30B	7	
M30	NC	-		PL31A	7	
L30	NC	-		PL31B	7	
L31	NC	-		PL34A	7	
M31	NC	-		PL34B	7	
AA29	NC	-		PL56A	6	
AA30	NC	-		PL56B	6	
AB31	NC	-		PL57A	6	
AA31	NC	-		PL57B	6	
AG30	NC	-		PL57C	6	
AG29	NC	-		PL57D	6	
AB29	NC	-		PL58A	6	
AB30	NC	-		PL58B	6	
Y25	NC	-		PL58C	6	
AA25	NC	-		PL58D	6	
AA8	NC	-		PR58D	3	
Y8	NC	-		PR58C	3	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG18	PB42C	5		PB61C	5	
AF18	PB42D	5		PB61D	5	
AP19	PB43A	5		PB63A	5	
AP18	PB43B	5		PB63B	5	
AJ18	PB43C	5		PB63C	5	
AH18	PB43D	5		PB63D	5	
AP17	PB45A	4		PB65A	4	
AP16	PB45B	4		PB65B	4	
AJ17	PB45C	4		PB65C	4	
AH17	PB45D	4		PB65D	4	
AN17	PB46A	4		PB66A	4	
AN16	PB46B	4		PB66B	4	
AE17	PB46C	4		PB66C	4	
AD17	PB46D	4		PB66D	4	
AK17	PB47A	4		PB67A	4	
AK16	PB47B	4		PB67B	4	
AG17	PB47C	4		PB67C	4	
AF17	PB47D	4		PB67D	4	
AM16	PB49A	4		PB69A	4	
AM15	PB49B	4		PB69B	4	
AJ15	PB49C	4		PB69C	4	
AJ14	PB49D	4		PB69D	4	
AL16	PB50A	4		PB70A	4	
AL15	PB50B	4		PB70B	4	
AG16	PB50C	4		PB70C	4	
AF16	PB50D	4		PB70D	4	
AP15	PB51A	4		PB71A	4	
AP14	PB51B	4		PB71B	4	
AH15	PB51C	4		PB71C	4	
AH14	PB51D	4		PB71D	4	
AN15	PB53A	4	PCLKT4_2	PB74A	4	PCLKT4_2
AN14	PB53B	4	PCLKC4_2	PB74B	4	PCLKC4_2
AE16	PB53C	4	PCLKT4_7	PB74C	4	PCLKT4_7
AD16	PB53D	4	PCLKC4_7	PB74D	4	PCLKC4_7
AK15	PB54A	4	PCLKT4_1	PB75A	4	PCLKT4_1
AK14	PB54B	4	PCLKC4_1	PB75B	4	PCLKC4_1
AG15	PB54C	4	PCLKT4_6	PB75C	4	PCLKT4_6
AG14	PB54D	4	PCLKC4_6	PB75D	4	PCLKC4_6
AM13	PB55A	4	PCLKT4_0	PB77A	4	PCLKT4_0
AM12	PB55B	4	PCLKC4_0	PB77B	4	PCLKC4_0
AJ12	PB55C	4	VREF2_4	PB77C	4	VREF2_4
AJ11	PB55D	4		PB77D	4	
AL13	PB57A	4	PCLKT4_5	PB79A	4	PCLKT4_5
AL12	PB57B	4	PCLKC4_5	PB79B	4	PCLKC4_5
AH12	PB57C	4		PB79C	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL4	PR117B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR117A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR116D	3	
AD9	PR116C	3	
AH4	PR116B	3	
AJ4	PR116A	3	
AK5	PR115D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR115C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR115B	3	
AL1	PR115A	3	
AH5	PR112D	3	
AG5	PR112C	3	
AL2	PR112B	3	
AK2	PR112A	3	
AB9	PR109D	3	
AC9	PR109C	3	
AH1	PR109B	3	
AG1	PR109A	3	
AE8	PR107D	3	VREF2_3
AD8	PR107C	3	
AJ3	PR107B	3	
AH3	PR107A	3	
AD7	PR104D	3	
AC7	PR104C	3	
AJ2	PR104B	3	
AH2	PR104A	3	
AF6	PR103D	3	
AF5	PR103C	3	
AF4	PR103B	3	
AE4	PR103A	3	
AD6	PR99D	3	
AC6	PR99C	3	
AG2	PR99B	3	
AF2	PR99A	3	
AC8	PR98D	3	
AB8	PR98C	3	
AK1	PR98B	3	
AJ1	PR98A	3	
AB10	PR96D	3	
AA10	PR96C	3	
AF3	PR96B	3	
AE3	PR96A	3	
AE5	PR94D	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W33	PL42C	7		PL56C	7	
Y33	PL42D	7		PL56D	7	
W37	PL43A	7		PL57A	7	
Y37	PL43B	7		PL57B	7	
Y32	PL43C	7		PL57C	7	
AA32	PL43D	7		PL57D	7	
U38	PL46A	7		PL60A	7	
V38	PL46B	7		PL60B	7	
W34	PL46C	7		PL60C	7	
Y34	PL46D	7		PL60D	7	
T40	PL47A	7	PCLKT7_1	PL61A	7	PCLKT7_1
U40	PL47B	7	PCLKC7_1	PL61B	7	PCLKC7_1
AA33	PL47C	7	PCLKT7_3	PL61C	7	PCLKT7_3
AB33	PL47D	7	PCLKC7_3	PL61D	7	PCLKC7_3
R42	PL48A	7	PCLKT7_0	PL62A	7	PCLKT7_0
T42	PL48B	7	PCLKC7_0	PL62B	7	PCLKC7_0
AA34	PL48C	7	PCLKT7_2	PL62C	7	PCLKT7_2
AB34	PL48D	7	PCLKC7_2	PL62D	7	PCLKC7_2
U41	PL50A	6	PCLKT6_0	PL64A	6	PCLKT6_0
V41	PL50B	6	PCLKC6_0	PL64B	6	PCLKC6_0
V36	PL50C	6	PCLKT6_1	PL64C	6	PCLKT6_1
W36	PL50D	6	PCLKC6_1	PL64D	6	PCLKC6_1
U42	PL51A	6		PL65A	6	
V42	PL51B	6		PL65B	6	
AB31	PL51C	6	PCLKT6_3	PL65C	6	PCLKT6_3
AC31	PL51D	6	PCLKC6_3	PL65D	6	PCLKC6_3
W38	PL52A	6		PL66A	6	
Y38	PL52B	6		PL66B	6	
AA35	PL52C	6	PCLKT6_2	PL66C	6	PCLKT6_2
AB35	PL52D	6	PCLKC6_2	PL66D	6	PCLKC6_2
W39	PL55A	6		PL69A	6	
Y39	PL55B	6		PL69B	6	
AB32	PL55C	6	VREF1_6	PL69C	6	VREF1_6
AC32	PL55D	6		PL69D	6	
W40	PL56A	6		PL70A	6	
Y40	PL56B	6		PL70B	6	
AA36	PL56C	6		PL70C	6	
AB36	PL56D	6		PL70D	6	
W41	PL57A	6		PL71A	6	
Y41	PL57B	6		PL71B	6	
AA37	PL57C	6		PL71C	6	
AB37	PL57D	6		PL71D	6	
W42	PL59A	6		PL73A	6	
Y42	PL59B	6		PL73B	6	
AC33	PL59C	6		PL73C	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F5	VCC12	-		VCC12	-	
B14	C_HDOUTP3_R	-	PCS 3E2 CH 3 OUT P	C_HDOUTP3_R	-	PCS 3E2 CH 3 OUT P
E13	C_HDINN3_R	-	PCS 3E2 CH 3 IN N	C_HDINN3_R	-	PCS 3E2 CH 3 IN N
D13	C_HDINP3_R	-	PCS 3E2 CH 3 IN P	C_HDINP3_R	-	PCS 3E2 CH 3 IN P
F12	VCC12	-		VCC12	-	
G14	C_VDDIB3_R	-		C_VDDIB3_R	-	
F11	VCC12	-		VCC12	-	
K15	C_REFCLKN_R	-		C_REFCLKN_R	-	
J15	C_REFCLKP_R	-		C_REFCLKP_R	-	
G15	VCC12	-		VCC12	-	
H16	D_VDDIB0_R	-		D_VDDIB0_R	-	
D14	D_HDINP0_R	-	PCS 3E3 CH 0 IN P	D_HDINP0_R	-	PCS 3E3 CH 0 IN P
E14	D_HDINN0_R	-	PCS 3E3 CH 0 IN N	D_HDINN0_R	-	PCS 3E3 CH 0 IN N
F6	VCC12	-		VCC12	-	
B15	D_HDOUTP0_R	-	PCS 3E3 CH 0 OUT P	D_HDOUTP0_R	-	PCS 3E3 CH 0 OUT P
M13	D_VDDOB0_R	-		D_VDDOB0_R	-	
A15	D_HDOUTN0_R	-	PCS 3E3 CH 0 OUT N	D_HDOUTN0_R	-	PCS 3E3 CH 0 OUT N
F8	D_VDDOB1_R	-		D_VDDOB1_R	-	
A16	D_HDOUTN1_R	-	PCS 3E3 CH 1 OUT N	D_HDOUTN1_R	-	PCS 3E3 CH 1 OUT N
F7	VCC12	-		VCC12	-	
B16	D_HDOUTP1_R	-	PCS 3E3 CH 1 OUT P	D_HDOUTP1_R	-	PCS 3E3 CH 1 OUT P
F15	D_HDINN1_R	-	PCS 3E3 CH 1 IN N	D_HDINN1_R	-	PCS 3E3 CH 1 IN N
E15	D_HDINP1_R	-	PCS 3E3 CH 1 IN P	D_HDINP1_R	-	PCS 3E3 CH 1 IN P
K17	VCC12	-		VCC12	-	
F13	D_VDDIB1_R	-		D_VDDIB1_R	-	
C14	VCC12	-		VCC12	-	
C15	D_VDDIB2_R	-		D_VDDIB2_R	-	
D16	D_HDINP2_R	-	PCS 3E3 CH 2 IN P	D_HDINP2_R	-	PCS 3E3 CH 2 IN P
E16	D_HDINN2_R	-	PCS 3E3 CH 2 IN N	D_HDINN2_R	-	PCS 3E3 CH 2 IN N
C11	VCC12	-		VCC12	-	
B17	D_HDOUTP2_R	-	PCS 3E3 CH 2 OUT P	D_HDOUTP2_R	-	PCS 3E3 CH 2 OUT P
C9	D_VDDOB2_R	-		D_VDDOB2_R	-	
A17	D_HDOUTN2_R	-	PCS 3E3 CH 2 OUT N	D_HDOUTN2_R	-	PCS 3E3 CH 2 OUT N
D17	D_VDDOB3_R	-		D_VDDOB3_R	-	
A18	D_HDOUTN3_R	-	PCS 3E3 CH 3 OUT N	D_HDOUTN3_R	-	PCS 3E3 CH 3 OUT N
C17	VCC12	-		VCC12	-	
B18	D_HDOUTP3_R	-	PCS 3E3 CH 3 OUT P	D_HDOUTP3_R	-	PCS 3E3 CH 3 OUT P
F17	D_HDINN3_R	-	PCS 3E3 CH 3 IN N	D_HDINN3_R	-	PCS 3E3 CH 3 IN N
E17	D_HDINP3_R	-	PCS 3E3 CH 3 IN P	D_HDINP3_R	-	PCS 3E3 CH 3 IN P
F14	VCC12	-		VCC12	-	
F16	D_VDDIB3_R	-		D_VDDIB3_R	-	
G16	VCC12	-		VCC12	-	
M17	D_REFCLKN_R	-		D_REFCLKN_R	-	
L17	D_REFCLKP_R	-		D_REFCLKP_R	-	
G18	PT77D	1	HDC/SI	PT93D	1	HDC/SI

Conventional Packaging

Commercial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7F256C	-7	fpBGA	256	COM	15.2
LFSC3GA15E-6F256C	-6	fpBGA	256	COM	15.2
LFSC3GA15E-5F256C	-5	fpBGA	256	COM	15.2
LFSC3GA15E-7F900C	-7	fpBGA	900	COM	15.2
LFSC3GA15E-6F900C	-6	fpBGA	900	COM	15.2
LFSC3GA15E-5F900C	-5	fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7F256C	-7	fpBGA	256	COM	15.2
LFSCM3GA15EP1-6F256C	-6	fpBGA	256	COM	15.2
LFSCM3GA15EP1-5F256C	-5	fpBGA	256	COM	15.2
LFSCM3GA15EP1-7F900C	-7	fpBGA	900	COM	15.2
LFSCM3GA15EP1-6F900C	-6	fpBGA	900	COM	15.2
LFSCM3GA15EP1-5F900C	-5	fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7F900C	-7	fpBGA	900	COM	25.4
LFSC3GA25E-6F900C	-6	fpBGA	900	COM	25.4
LFSC3GA25E-5F900C	-5	fpBGA	900	COM	25.4
LFSC3GA25E-7FF1020C[1]	-7	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FF1020C[1]	-6	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FF1020C[1]	-5	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7F900C	-7	fpBGA	900	COM	25.4
LFSCM3GA25EP1-6F900C	-6	fpBGA	900	COM	25.4
LFSCM3GA25EP1-5F900C	-5	fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FF1020C[1]	-7	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FF1020C[1]	-6	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FF1020C[1]	-5	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.