



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

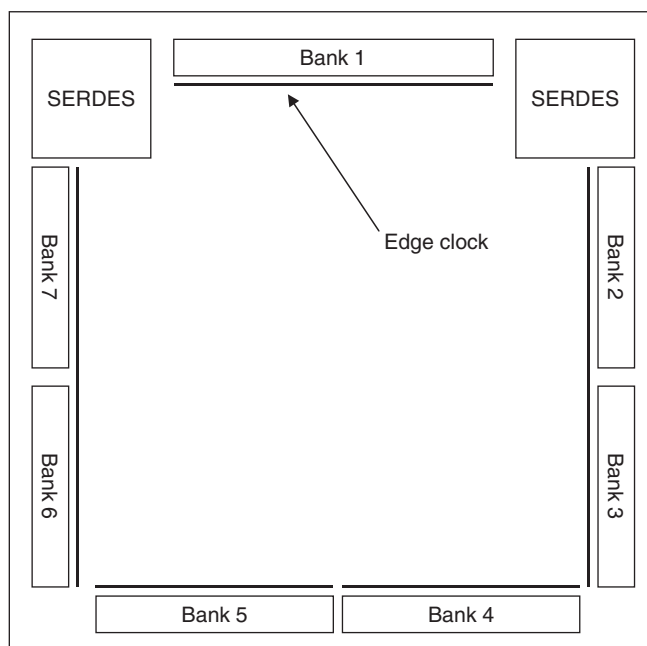
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

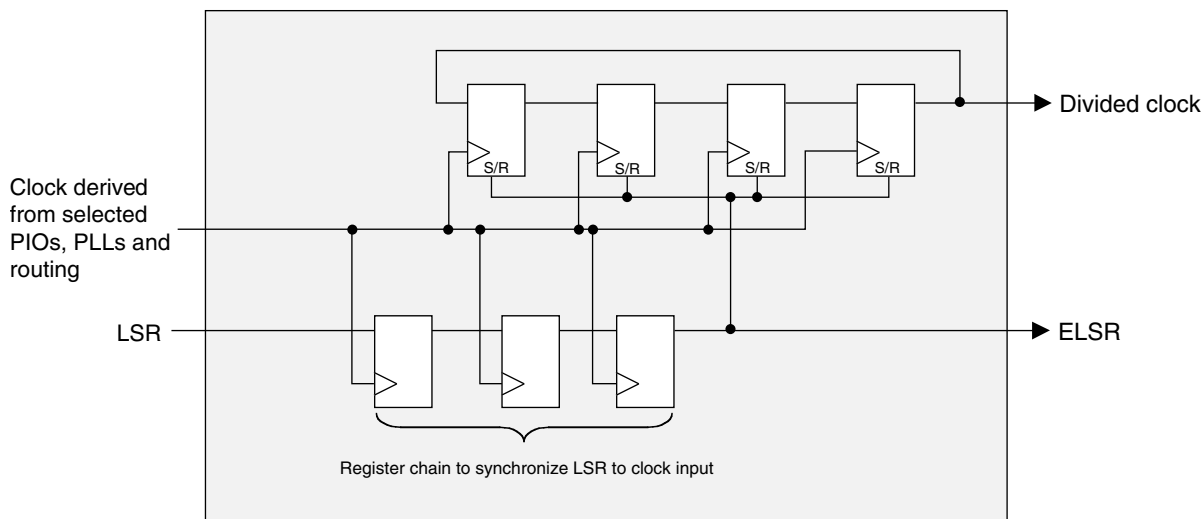
Details

Product Status	Obsolete
Number of LABs/CLBs	3750
Number of Logic Elements/Cells	15000
Total RAM Bits	1054720
Number of I/O	139
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga15e-5f256i

Figure 2-7. Edge Clock Resources

Precision Clock Divider

Each set of edge clocks has four high-speed dividers associated with it. These are intended for generating a slower speed system clock from the high-speed edge clock. The block operates in a DIV2 or DIV4 mode and maintains a known phase relationship between the divided down clock and high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PIOs, PLLs and routing. The clock divider outputs serve as primary clock sources. This circuit also generates an edge local set/reset (ELSR) signal which is fed to the PIOs via the edge clock network and is used for the rest of the I/O gearing logic.

Figure 2-8. Clock Divider Circuit

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is

PURESPEED I/O Buffer Banks

LatticeSC devices have seven PURESPEED I/O buffer banks; each is capable of supporting multiple I/O standards. Each PURESPEED I/O bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-26 shows the seven banks and their associated supplies. Table 2-7 lists the maximum number of I/Os per bank for the whole LatticeSC family.

In the LatticeSC devices, single-ended output buffers and ratioed input buffers (LVTTTL, LVCMOS, PCI33 and PCIX33) are powered using V_{CCIO} . In addition to the bank V_{CCIO} supplies, the LatticeSC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers. V_{CCAUX} also powers a predriver of single-ended output buffers to enhance buffer performance.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeSC devices any I/O pin in a bank can be configured to be a dedicated reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Differential drivers have user selectable internal or external bias. External bias is brought in by the VREF1 pin in the bank. External bias for differential buffers is needed for applications that requires tighter than standard output common mode range.

Since a bank can have only one external bias circuit for differential drivers, LVDS and RSDS differential outputs can be mixed in a bank.

If a differential driver is configured in a bank, one pin in that bank becomes a DIFFR pin. This DIFFR pin must be connected to ground via an external 1K +/-1% ohm resistor. Note that differential drivers are not supported in banks 1, 4 and 5.

In addition, there are dedicated Terminating Supply (V_{TT}) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These V_{TT} pins are available in banks 2-7, these pins are not available in some packages. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.

There are further restrictions on the use of V_{TT} pins, for additional details refer to technical information at the end of this data sheet.

Figure 2-27. Output Termination Schemes

Termination Type	Discrete Off-Chip Solution	Lattice On-Chip Solution
Series termination (controlled output impedance)		
Parallel termination to V_{CCIO} , or parallel driving end		
Parallel termination to $V_{CCIO}/2$ driving end		
Combined series + parallel termination to $V_{CCIO}/2$ at driving end (only series termination moved on-chip)		
Combined series + parallel to $V_{CCIO}/2$ driving end		

Single Ended Inputs: The SC devices support a number of different termination schemes for single ended inputs:

- Parallel to V_{CCIO} or GND
- Parallel to $V_{CCIO}/2$
- Parallel to V_{TT}

Figure 2-28 shows the single ended input schemes that are supported. The nominal values of the termination resistors are shown in Table 2-9.

Figure 2-28. Input Termination Schemes

Termination Type	Discrete Off-Chip Solution	Lattice On-Chip Solution
Parallel termination to to V_{CCIO} , or parallel to GND receiving end		
Parallel termination to $V_{CCIO}/2$ receiving end		
Parallel termination to V_{TT} at receiving end		

In many situations designers can chose whether to use Thevenin or parallel to V_{TT} termination. The Thevenin approach has the benefit of not requiring a termination voltage to be applied to the device. The parallel to V_{TT} approach consumes less power.

VTT Termination Resources

Each I/O bank, except bank 1, has a number of V_{TT} pins that must be connected if V_{TT} is used. Note V_{TT} pins can sink or source current and the power supply they are connected to must be able to handle the relatively high currents associated with the termination circuits. Note: V_{TT} is not available in all package styles.

On-chip parallel termination to V_{TT} is supported at the receiving end only. On-chip parallel output termination to V_{TT} is not supported.

The V_{TT} internal bus is also connected to the internal V_{CMT} node. Thus in one bank designers can implement either V_{TT} termination or V_{CMT} termination for differential inputs.

DDRII/RLDRAMII Termination Support

The DDR II memory and RLDRAMII (in Bidirection Data mode) standards require that the on-chip termination to V_{TT} be turned on when a pin is an input and off when the pin is an output. The LatticeSC devices contain the required circuitry to support this behavior. For additional detail refer to technical information at the end of the data sheet.

Absolute Maximum Ratings

Supply Voltage V_{CC} , V_{CC12} , V_{DDIB} , V_{DDOB}	-0.5 to 1.6V
Supply Voltage V_{CCAUX} , V_{DDAX25} , V_{TT}	-0.5 to 2.75V
Supply Voltage V_{CCJ}	-0.5 to 3.6V
Supply Voltage V_{CCIO} (Banks 1, 4, 5)	-0.5 to 3.6V
Supply Voltage V_{CCIO} (Banks 2, 3, 6, 7)	-0.5 to 2.75V
Input or I/O Tristate Voltage Applied (Banks 1, 4, 5)	-0.5 to 3.6V
Input or I/O Tristate Voltage Applied (Banks 2, 3, 6, 7)	-0.5 to 2.75V
Storage Temperature (Ambient)	-65 to 150°C
Junction Temperature Under Bias (Tj)	+125°C

Notes:

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot and overshoot of -2V to (VIHMAX +2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}^5	Core Supply Voltage (Nominal 1.2V Operation)	0.95	1.26	V
V_{CCAUX}^6	Programmable I/O Auxiliary Supply Voltage	2.375	2.625	V
$V_{CCIO}^{1,2,5,6}$	Programmable I/O Driver Supply Voltage (Banks 1, 4, 5)	1.14	3.45	V
$V_{CCIO}^{1,2,5,6}$	Programmable I/O Driver Supply Voltage (Banks 2, 3, 6, 7)	1.14	2.625	V
$V_{CC12}^{4,5}$	Internal 1.2V Power Supply Voltage for Configuration Logic and FPGA PLL, SERDES PLL Power Supply Voltage and SERDES Analog Supply Voltage	1.14	1.26	V
V_{DDIB}	SERDES Input Buffer Supply Voltage	1.14	1.575	V
V_{DDOB}	SERDES Output Buffer Supply Voltage	1.14	1.575	V
V_{DDAX25}	SERDES Termination Auxiliary Supply Voltage	2.375	2.625	V
$V_{CCJ}^{1,5}$	Supply Voltage for IEEE 1149.1 Test Access Port	1.71	3.45	V
$V_{TT}^{2,3}$	Programmable I/O Termination Power Supply	0.5	$V_{CCAUX} - 0.5$	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	+85	C
t_{JIND}	Junction Temperature, Industrial Operation	-40	105	C

1. If V_{CCIO} or V_{CCJ} is set to 2.5V, they must be connected to the same power supply as V_{CCAUX} .
2. See recommended voltages by I/O standard in subsequent table.
3. When V_{TT} termination is not required, or used to provide the common mode termination voltage (V_{CMT}), these pins can be left unconnected on the device.
4. V_{CC12} cannot be lower than V_{CC} at any time. For 1.2V operation, it is recommended that the V_{CC} and V_{CC12} supplies be tied together with proper noise decoupling between the digital VCC and analog VCC12 supplies.
5. V_{CC} , V_{CCIO} (all banks), V_{CC12} and V_{CCJ} must reach their minimum values before configuration will proceed.
6. If V_{CCIO} for a bank is nominally 1.2V/1.5V/1.8V, then V_{CCAUX} must always be higher than V_{CCIO} during power up.

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
GTLPLUS15	GTLPLUS15	-0.013	-0.017	0.012	0.004	0.037	0.024	ns
GTL12	GTL12	-0.063	-0.071	-0.007	-0.048	0.056	-0.032	ns
Output Adjusters								
LVDS	LVDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
RSDS	RSDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
BLVDS25	BLVDS	-0.129	0.05	-0.136	0.069	-0.136	0.083	ns
MLVDS25	MLVDS	-0.059	0.059	-0.057	0.096	-0.054	0.133	ns
LVPECL33	LVPECL	-0.334	-0.181	-0.325	-1.389	-0.315	-2.598	ns
HSTL18_I	HSTL_18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18_II	HSTL_18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL18D_I	Differential HSTL 18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18D_II	Differential HSTL 18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL15_I	HSTL_15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15_II	HSTL_15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
HSTL15D_I	Differential HSTL 15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15D_II	Differential HSTL 15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
SSTL33_I	SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33_II	SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL33D_I	Differential SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33D_II	Differential SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL25_I	SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25_II	SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL25D_I	Differential SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25D_II	Differential SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL18_I	SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18_II	SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
SSTL18D_I	Differential SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18D_II	Differential SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
LVTTTL33_8mA	LVTTTL 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVTTTL33_16mA	LVTTTL 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVTTTL33_24mA	LVTTTL 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVC MOS33_24mA	LVC MOS 3.3 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive	-0.174	0.004	-0.195	0.002	-0.215	0	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive	0	0	0	0	0	0	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive	0.094	-0.025	0.107	0.096	0.12	0.216	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive	0.145	-0.054	0.162	0.063	0.181	0.179	ns
LVC MOS25_OD	LVC MOS 2.5 open drain	0.073	-0.125	0.081	-0.081	0.091	-0.09	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive	-0.278	-0.099	-0.312	-0.115	-0.345	-0.131	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive	-0.073	-0.078	-0.078	-0.084	-0.083	-0.089	ns

Signal Descriptions (Cont.)

Signal Name	I/O	Description
RESP_[ULC/URC]	—	Calibration resistor to be placed between this pin and either ground or RESPN_[ULC/URC]. RESPN_[ULC/URC] is available on select packages. If available, connection of calibration resistor between RESP_[ULC/URC] and RESPN_[ULC/URC] takes precedence over connection of calibration resistor between RESP_[ULC/URC] and ground. Note: only one per side of the device. Value: 4.02K ohm +/- 1% ohm.
RESPN_[ULC/URC]	—	Available on selected packages. If available, calibration resistor should be placed between RESP_[ULC/URC] and RESPN_[ULC/URC] instead of between RESP_[ULC/URC] and ground. Note: only one per side of the device. Value: 4.02K ohm +/- 1% ohm.
[A:D]_VDDIBx_[L/R]	—	Input buffer power supply for channel x (1.2V/1.5V) on left [L] or right [R] side of device.
[A:D]_VDDOBx_[L/R]	—	Output buffer power supply for channel x (1.2V/1.5V) on left [L] or right [R] side of device.
[A:D]_VDDAX25_[L/R]	—	Auxiliary power for input and output termination (2.5V) on left [L] or right [R] side of device.

1. The ispLEVER software tools may specify VDDR_x, VDDT_x, VDDP and VCCL pins. These pins should be considered VCC12 pins.
Note: Signals listed as Signal A / Signal B define the same physical pin that is used for different functions based on configuration mode.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG11	VCCIO5	-		VCCIO5	-	
AJ9	VCCIO5	-		VCCIO5	-	
AJ23	VCCIO4	-		VCCIO4	-	
AG20	VCCIO4	-		VCCIO4	-	
AJ26	VCCIO4	-		VCCIO4	-	
AG23	VCCIO4	-		VCCIO4	-	
AC29	VCCIO3	-		VCCIO3	-	
AA26	VCCIO3	-		VCCIO3	-	
Y28	VCCIO3	-		VCCIO3	-	
AA29	VCCIO3	-		VCCIO3	-	
G30	VCCIO2	-		VCCIO2	-	
J29	VCCIO2	-		VCCIO2	-	
K27	VCCIO2	-		VCCIO2	-	
N25	VCCIO2	-		VCCIO2	-	
F20	VCCIO1	-		VCCIO1	-	
C19	VCCIO1	-		VCCIO1	-	
C12	VCCIO1	-		VCCIO1	-	
F11	VCCIO1	-		VCCIO1	-	
H1	GND	-		GND	-	
L4	GND	-		GND	-	
M3	GND	-		GND	-	
N5	GND	-		GND	-	
K2	GND	-		GND	-	
M2	GND	-		GND	-	
P6	GND	-		GND	-	
G4	GND	-		GND	-	
H3	GND	-		GND	-	
AC2	GND	-		GND	-	
AA3	GND	-		GND	-	
AE1	GND	-		GND	-	
Y4	GND	-		GND	-	
AB4	GND	-		GND	-	
AA5	GND	-		GND	-	
AE6	GND	-		GND	-	
AE8	GND	-		GND	-	
AH5	GND	-		GND	-	
AG9	GND	-		GND	-	
AG6	GND	-		GND	-	
AF11	GND	-		GND	-	
AG12	GND	-		GND	-	
AJ10	GND	-		GND	-	
AK26	GND	-		GND	-	
AJ22	GND	-		GND	-	
AF20	GND	-		GND	-	
AJ25	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y6	PR42D	3	DIFFR_3	PR51D	3	DIFFR_3
W6	PR42C	3		PR51C	3	
Y2	PR42B	3		PR51B	3	
W2	PR42A	3		PR51A	3	
W7	PR40D	3		PR49D	3	
V8	PR40C	3		PR49C	3	
W4	PR40B	3		PR49B	3	
W3	PR40A	3		PR49A	3	
V5	PR39D	3		PR48D	3	
U6	PR39C	3		PR48C	3	
V3	PR39B	3		PR48B	3	
V4	PR39A	3		PR48A	3	
V10	PR38D	3		PR47D	3	
V9	PR38C	3		PR47C	3	
V2	PR38B	3		PR47B	3	
V1	PR38A	3		PR47A	3	
U8	PR36D	3		PR45D	3	
U7	PR36C	3		PR45C	3	
U2	PR36B	3		PR45B	3	
U1	PR36A	3		PR45A	3	
U5	PR35D	3		PR44D	3	
T6	PR35C	3		PR44C	3	
T1	PR35B	3		PR44B	3	
T2	PR35A	3		PR44A	3	
U9	PR34D	3		PR43D	3	
U10	PR34C	3	VREF1_3	PR43C	3	VREF1_3
R1	PR34B	3		PR43B	3	
R2	PR34A	3		PR43A	3	
T7	PR31D	3	PCLKC3_2	PR40D	3	PCLKC3_2
T8	PR31C	3	PCLKT3_2	PR40C	3	PCLKT3_2
R4	PR31B	3		PR40B	3	
R3	PR31A	3		PR40A	3	
T5	PR30D	3	PCLKC3_3	PR39D	3	PCLKC3_3
R5	PR30C	3	PCLKT3_3	PR39C	3	PCLKT3_3
P2	PR30B	3		PR39B	3	
P1	PR30A	3		PR39A	3	
T9	PR29D	3	PCLKC3_1	PR38D	3	PCLKC3_1
T10	PR29C	3	PCLKT3_1	PR38C	3	PCLKT3_1
P4	PR29B	3	PCLKC3_0	PR38B	3	PCLKC3_0
P3	PR29A	3	PCLKT3_0	PR38A	3	PCLKT3_0
P5	PR27D	2	PCLKC2_2	PR36D	2	PCLKC2_2
P6	PR27C	2	PCLKT2_2	PR36C	2	PCLKT2_2
N1	PR27B	2	PCLKC2_0	PR36B	2	PCLKC2_0
N2	PR27A	2	PCLKT2_0	PR36A	2	PCLKT2_0
R9	PR26D	2	PCLKC2_3	PR35D	2	PCLKC2_3
R8	PR26C	2	PCLKT2_3	PR35C	2	PCLKT2_3
M1	PR26B	2	PCLKC2_1	PR35B	2	PCLKC2_1
L1	PR26A	2	PCLKT2_1	PR35A	2	PCLKT2_1
N9	PR25D	2	DIFFR_2	PR23D	2	DIFFR_2
M9	PR25C	2	VREF1_2	PR23C	2	VREF1_2

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AA7	VCCIO3	-		VCCIO3	-	
AB9	VCCIO3	-		VCCIO3	-	
AC4	VCCIO3	-		VCCIO3	-	
AD6	VCCIO3	-		VCCIO3	-	
AF3	VCCIO3	-		VCCIO3	-	
T3	VCCIO3	-		VCCIO3	-	
U4	VCCIO3	-		VCCIO3	-	
V6	VCCIO3	-		VCCIO3	-	
W10	VCCIO3	-		VCCIO3	-	
Y3	VCCIO3	-		VCCIO3	-	
AC11	VCCIO4	-		VCCIO4	-	
AD14	VCCIO4	-		VCCIO4	-	
AF15	VCCIO4	-		VCCIO4	-	
AF9	VCCIO4	-		VCCIO4	-	
AG12	VCCIO4	-		VCCIO4	-	
AJ13	VCCIO4	-		VCCIO4	-	
AJ7	VCCIO4	-		VCCIO4	-	
AK10	VCCIO4	-		VCCIO4	-	
AK16	VCCIO4	-		VCCIO4	-	
AK4	VCCIO4	-		VCCIO4	-	
AC19	VCCIO5	-		VCCIO5	-	
AD22	VCCIO5	-		VCCIO5	-	
AF21	VCCIO5	-		VCCIO5	-	
AG18	VCCIO5	-		VCCIO5	-	
AG24	VCCIO5	-		VCCIO5	-	
AJ17	VCCIO5	-		VCCIO5	-	
AJ23	VCCIO5	-		VCCIO5	-	
AJ30	VCCIO5	-		VCCIO5	-	
AK20	VCCIO5	-		VCCIO5	-	
AK26	VCCIO5	-		VCCIO5	-	
AA27	VCCIO6	-		VCCIO6	-	
AB23	VCCIO6	-		VCCIO6	-	
AC30	VCCIO6	-		VCCIO6	-	
AD26	VCCIO6	-		VCCIO6	-	
AF29	VCCIO6	-		VCCIO6	-	
T29	VCCIO6	-		VCCIO6	-	
U30	VCCIO6	-		VCCIO6	-	
V26	VCCIO6	-		VCCIO6	-	
W24	VCCIO6	-		VCCIO6	-	
Y29	VCCIO6	-		VCCIO6	-	
G30	VCCIO7	-		VCCIO7	-	
J27	VCCIO7	-		VCCIO7	-	
K29	VCCIO7	-		VCCIO7	-	
L24	VCCIO7	-		VCCIO7	-	
M26	VCCIO7	-		VCCIO7	-	
N30	VCCIO7	-		VCCIO7	-	
P23	VCCIO7	-		VCCIO7	-	
R27	VCCIO7	-		VCCIO7	-	
AA11	VCCAUX	-		VCCAUX	-	
AA12	VCCAUX	-		VCCAUX	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
R7	NC	-		PR39D	2	
P7	NC	-		PR39C	2	
N3	NC	-		PR39B	2	
M3	NC	-		PR39A	2	
H1	NC	-		PR26B	2	
G1	NC	-		PR26A	2	
L5	NC	-		PR25B	2	
K5	NC	-		PR25A	2	
G2	NC	-		PR24B	2	
F2	NC	-		PR24A	2	
F1	NC	-		PR22B	2	
E1	NC	-		PR22A	2	
A2	GND	-		GND	-	
A33	GND	-		GND	-	
AA15	GND	-		GND	-	
AA20	GND	-		GND	-	
AA32	GND	-		GND	-	
AA4	GND	-		GND	-	
AB28	GND	-		GND	-	
AB6	GND	-		GND	-	
AC11	GND	-		GND	-	
AC18	GND	-		GND	-	
AC25	GND	-		GND	-	
AD23	GND	-		GND	-	
AD3	GND	-		GND	-	
AD31	GND	-		GND	-	
AE12	GND	-		GND	-	
AE15	GND	-		GND	-	
AE29	GND	-		GND	-	
AE7	GND	-		GND	-	
AE9	GND	-		GND	-	
AF20	GND	-		GND	-	
AF26	GND	-		GND	-	
AG32	GND	-		GND	-	
AG4	GND	-		GND	-	
AH13	GND	-		GND	-	
AH19	GND	-		GND	-	
AH25	GND	-		GND	-	
AH7	GND	-		GND	-	
AJ10	GND	-		GND	-	
AJ16	GND	-		GND	-	
AJ22	GND	-		GND	-	
AJ28	GND	-		GND	-	
AK3	GND	-		GND	-	
AK31	GND	-		GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
L5	PR38B	2	
K5	PR38A	2	
G2	PR34B	2	
F2	PR34A	2	
F1	PR30B	2	
E1	PR30A	2	
A2	GND	-	
A33	GND	-	
AA15	GND	-	
AA20	GND	-	
AA32	GND	-	
AA4	GND	-	
AB28	GND	-	
AB6	GND	-	
AC11	GND	-	
AC18	GND	-	
AC25	GND	-	
AD23	GND	-	
AD3	GND	-	
AD31	GND	-	
AE12	GND	-	
AE15	GND	-	
AE29	GND	-	
AE7	GND	-	
AE9	GND	-	
AF20	GND	-	
AF26	GND	-	
AG32	GND	-	
AG4	GND	-	
AH13	GND	-	
AH19	GND	-	
AH25	GND	-	
AH7	GND	-	
AJ10	GND	-	
AJ16	GND	-	
AJ22	GND	-	
AJ28	GND	-	
AK3	GND	-	
AK31	GND	-	
AL11	GND	-	
AL17	GND	-	
AL21	GND	-	
AL27	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP41	PL91B	6		PL112B	6	
AK35	PL91C	6		PL112C	6	
AL35	PL91D	6		PL112D	6	
AN38	PL93A	6		PL115A	6	
AP38	PL93B	6		PL115B	6	
AL37	PL93C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL115C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AM37	PL93D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL115D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AR41	PL94A	6		PL116A	6	
AT41	PL94B	6		PL116B	6	
AN37	PL94C	6		PL116C	6	
AP37	PL94D	6		PL116D	6	
AR39	PL95A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL117A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AR40	PL95B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL117B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AN36	PL95C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL117C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AP36	PL95D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL117D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AT40	XRES	-		XRES	-	
AU41	TEMP	6		TEMP	6	
AU42	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AV42	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AL33	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AL34	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AU38	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AV38	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AM34	PB4C	5		PB4C	5	
AM33	PB4D	5		PB4D	5	
AV41	PB5A	5		PB5A	5	
AW41	PB5B	5		PB5B	5	
AK30	PB5C	5		PB5C	5	
AK29	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AW42	PB7A	5		PB7A	5	
AY42	PB7B	5		PB7B	5	
AR37	PB7C	5		PB7C	5	
AR38	PB7D	5		PB7D	5	
AV40	PB8A	5		PB9A	5	
AV39	PB8B	5		PB9B	5	
AN35	PB8C	5		PB9C	5	
AN34	PB8D	5		PB9D	5	
AW40	PB9A	5		PB11A	5	
AY40	PB9B	5		PB11B	5	
AP34	PB9C	5		PB11C	5	
AP35	PB9D	5		PB11D	5	
AW39	PB11A	5		PB12A	5	
AW38	PB11B	5		PB12B	5	
AL32	PB11C	5		PB12C	5	
AL31	PB11D	5		PB12D	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL23	PB56D	5		PB58D	5	
AW24	PB57A	5		PB61A	5	
AW23	PB57B	5		PB61B	5	
AN23	PB57C	5		PB61C	5	
AP23	PB57D	5		PB61D	5	
AY23	PB59A	5		PB63A	5	
AY24	PB59B	5		PB63B	5	
AU23	PB59C	5		PB63C	5	
AU22	PB59D	5		PB63D	5	
AV23	PB60A	5		PB66A	5	
AV22	PB60B	5		PB66B	5	
AM22	PB60C	5		PB66C	5	
AL22	PB60D	5		PB66D	5	
BA23	PB61A	5		PB69A	5	
BA22	PB61B	5		PB69B	5	
AN22	PB61C	5		PB69C	5	
AP22	PB61D	5		PB69D	5	
BB23	PB63A	5		PB71A	5	
BB22	PB63B	5		PB71B	5	
AT22	PB63C	5		PB71C	5	
AR22	PB63D	5		PB71D	5	
BB21	PB65A	4		PB73A	4	
BB20	PB65B	4		PB73B	4	
AR21	PB65C	4		PB73C	4	
AT21	PB65D	4		PB73D	4	
BA21	PB66A	4		PB75A	4	
BA20	PB66B	4		PB75B	4	
AP21	PB66C	4		PB75C	4	
AN21	PB66D	4		PB75D	4	
AV21	PB67A	4		PB78A	4	
AV20	PB67B	4		PB78B	4	
AM21	PB67C	4		PB78C	4	
AL21	PB67D	4		PB78D	4	
AY20	PB69A	4		PB81A	4	
AY19	PB69B	4		PB81B	4	
AU21	PB69C	4		PB81C	4	
AU20	PB69D	4		PB81D	4	
AW20	PB70A	4		PB83A	4	
AW19	PB70B	4		PB83B	4	
AP20	PB70C	4		PB83C	4	
AN20	PB70D	4		PB83D	4	
BB19	PB71A	4		PB86A	4	
BB18	PB71B	4		PB86B	4	
AM20	PB71C	4		PB86C	4	
AL20	PB71D	4		PB86D	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D32	C_HDINP1_L	-	PCS 362 CH 1 IN P	C_HDINP1_L	-	PCS 362 CH 1 IN P
E32	C_HDINN1_L	-	PCS 362 CH 1 IN N	C_HDINN1_L	-	PCS 362 CH 1 IN N
B31	C_HDOUTP1_L	-	PCS 362 CH 1 OUT P	C_HDOUTP1_L	-	PCS 362 CH 1 OUT P
K32	VCC12	-		VCC12	-	
A31	C_HDOUTN1_L	-	PCS 362 CH 1 OUT N	C_HDOUTN1_L	-	PCS 362 CH 1 OUT N
L32	C_VDDOB1_L	-		C_VDDOB1_L	-	
A32	C_HDOUTN0_L	-	PCS 362 CH 0 OUT N	C_HDOUTN0_L	-	PCS 362 CH 0 OUT N
M31	C_VDDOB0_L	-		C_VDDOB0_L	-	
B32	C_HDOUTP0_L	-	PCS 362 CH 0 OUT P	C_HDOUTP0_L	-	PCS 362 CH 0 OUT P
H37	VCC12	-		VCC12	-	
E33	C_HDINN0_L	-	PCS 362 CH 0 IN N	C_HDINN0_L	-	PCS 362 CH 0 IN N
D33	C_HDINP0_L	-	PCS 362 CH 0 IN P	C_HDINP0_L	-	PCS 362 CH 0 IN P
G31	C_VDDIB0_L	-		C_VDDIB0_L	-	
J29	VCC12	-		VCC12	-	
L29	B_REFCLKP_L	-		B_REFCLKP_L	-	
M29	B_REFCLKN_L	-		B_REFCLKN_L	-	
J31	VCC12	-		VCC12	-	
H31	B_VDDIB3_L	-		B_VDDIB3_L	-	
J30	VCC12	-		VCC12	-	
D34	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
E34	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
B33	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
H38	VCC12	-		VCC12	-	
A33	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
C38	B_VDDOB3_L	-		B_VDDOB3_L	-	
A34	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
L31	B_VDDOB2_L	-		B_VDDOB2_L	-	
B34	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G38	VCC12	-		VCC12	-	
E35	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
D35	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H32	B_VDDIB2_L	-		B_VDDIB2_L	-	
K29	VCC12	-		VCC12	-	
K30	B_VDDIB1_L	-		B_VDDIB1_L	-	
F33	VCC12	-		VCC12	-	
D36	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
E36	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
B35	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L34	VCC12	-		VCC12	-	
A35	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
K35	B_VDDOB1_L	-		B_VDDOB1_L	-	
A36	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
G39	B_VDDOB0_L	-		B_VDDOB0_L	-	
B36	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
J35	VCC12	-		VCC12	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM27	GND	-		GND	-	
AM36	GND	-		GND	-	
AM7	GND	-		GND	-	
AP4	GND	-		GND	-	
AP40	GND	-		GND	-	
AR14	GND	-		GND	-	
AR20	GND	-		GND	-	
AR23	GND	-		GND	-	
AR29	GND	-		GND	-	
AR35	GND	-		GND	-	
AR8	GND	-		GND	-	
AT11	GND	-		GND	-	
AT17	GND	-		GND	-	
AT26	GND	-		GND	-	
AT32	GND	-		GND	-	
AU3	GND	-		GND	-	
AU39	GND	-		GND	-	
AW12	GND	-		GND	-	
AW18	GND	-		GND	-	
AW22	GND	-		GND	-	
AW28	GND	-		GND	-	
AW34	GND	-		GND	-	
AW6	GND	-		GND	-	
AY15	GND	-		GND	-	
AY21	GND	-		GND	-	
AY25	GND	-		GND	-	
AY31	GND	-		GND	-	
AY37	GND	-		GND	-	
AY9	GND	-		GND	-	
B1	GND	-		GND	-	
B42	GND	-		GND	-	
BA1	GND	-		GND	-	
BA42	GND	-		GND	-	
BB2	GND	-		GND	-	
BB41	GND	-		GND	-	
C10	GND	-		GND	-	
C12	GND	-		GND	-	
C13	GND	-		GND	-	
C16	GND	-		GND	-	
C18	GND	-		GND	-	
C19	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C27	GND	-		GND	-	
C28	GND	-		GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
T16	GND	-		GND	-	
T19	GND	-		GND	-	
T24	GND	-		GND	-	
T27	GND	-		GND	-	
T32	GND	-		GND	-	
U18	GND	-		GND	-	
U20	GND	-		GND	-	
U23	GND	-		GND	-	
U25	GND	-		GND	-	
U36	GND	-		GND	-	
U7	GND	-		GND	-	
G36	GND	-		GND	-	
G7	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V24	GND	-		GND	-	
V26	GND	-		GND	-	
V4	GND	-		GND	-	
V40	GND	-		GND	-	
W12	GND	-		GND	-	
W16	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W25	GND	-		GND	-	
W27	GND	-		GND	-	
W31	GND	-		GND	-	
Y17	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y22	GND	-		GND	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AA22	VCC	-		VCC	-	
AA24	VCC	-		VCC	-	
AA25	VCC	-		VCC	-	
AA26	VCC	-		VCC	-	
AB17	VCC	-		VCC	-	
AB18	VCC	-		VCC	-	
AB19	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
AB22	VCC	-		VCC	-	
AB24	VCC	-		VCC	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L8	VCCIO2	-		VCCIO2	-	
M3	VCCIO2	-		VCCIO2	-	
P7	VCCIO2	-		VCCIO2	-	
R4	VCCIO2	-		VCCIO2	-	
T12	VCCIO2	-		VCCIO2	-	
U8	VCCIO2	-		VCCIO2	-	
V3	VCCIO2	-		VCCIO2	-	
W11	VCCIO2	-		VCCIO2	-	
Y7	VCCIO2	-		VCCIO2	-	
AB3	VCCIO3	-		VCCIO3	-	
AC7	VCCIO3	-		VCCIO3	-	
AD11	VCCIO3	-		VCCIO3	-	
AE4	VCCIO3	-		VCCIO3	-	
AF8	VCCIO3	-		VCCIO3	-	
AG12	VCCIO3	-		VCCIO3	-	
AH3	VCCIO3	-		VCCIO3	-	
AJ7	VCCIO3	-		VCCIO3	-	
AK11	VCCIO3	-		VCCIO3	-	
AL4	VCCIO3	-		VCCIO3	-	
AM8	VCCIO3	-		VCCIO3	-	
AP3	VCCIO3	-		VCCIO3	-	
AR7	VCCIO3	-		VCCIO3	-	
AU4	VCCIO3	-		VCCIO3	-	
AL16	VCCIO4	-		VCCIO4	-	
AM13	VCCIO4	-		VCCIO4	-	
AM19	VCCIO4	-		VCCIO4	-	
AR11	VCCIO4	-		VCCIO4	-	
AR17	VCCIO4	-		VCCIO4	-	
AT14	VCCIO4	-		VCCIO4	-	
AT20	VCCIO4	-		VCCIO4	-	
AT8	VCCIO4	-		VCCIO4	-	
AW15	VCCIO4	-		VCCIO4	-	
AW21	VCCIO4	-		VCCIO4	-	
AW9	VCCIO4	-		VCCIO4	-	
AY12	VCCIO4	-		VCCIO4	-	
AY18	VCCIO4	-		VCCIO4	-	
AY6	VCCIO4	-		VCCIO4	-	
AL27	VCCIO5	-		VCCIO5	-	
AM24	VCCIO5	-		VCCIO5	-	
AM30	VCCIO5	-		VCCIO5	-	
AR26	VCCIO5	-		VCCIO5	-	
AR32	VCCIO5	-		VCCIO5	-	
AT23	VCCIO5	-		VCCIO5	-	
AT29	VCCIO5	-		VCCIO5	-	
AT35	VCCIO5	-		VCCIO5	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).