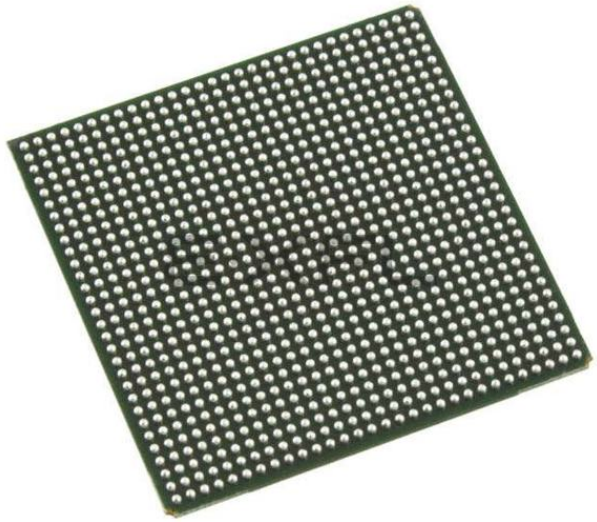
Lattice Semiconductor Corporation - LFSC3GA15E-5FN900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3750
Number of Logic Elements/Cells	15000
Total RAM Bits	1054720
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga15e-5fn900c

toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-9 illustrates the DCS Block diagram.

Figure 2-9. DCS Block Diagram

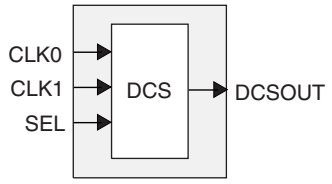
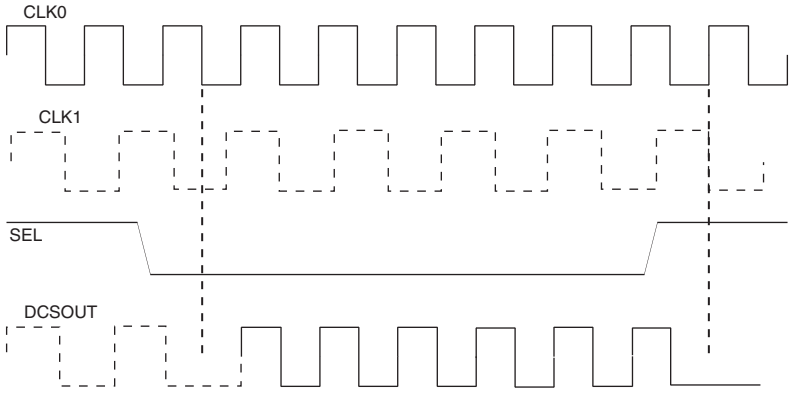


Figure 2-10 shows timing waveforms for one of the DCS operating modes. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-10. DCS Waveforms



Clock Boosting

There are programmable delays available in the clock signal paths in the PFU, PIC and EBR blocks. These allow setup and clock-to-output times to be traded to meet critical timing without slowing the system clock. If this feature is enabled then the design tool automatically uses these delays to improve timing performance.

Global Set/Reset

There is a global set/reset (GSR) network on the device that is distributed to all FFs, PLLs, DLLs and other blocks on the device. This GSR network can operate in two modes:

a) asynchronous - no clock is required to get into or out of the reset state.

b) synchronous - The global GSR net is synchronized to a user selected clock. In this mode it continues to be asynchronous to get into the reset state, but is synchronous to get out of the reset state. This allows all registers on the device to become operational in the same clock period. The synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met (not from the GSR being released).

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider and two clock output dividers. The input divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal.

LatticeSC/M sysCONFIG Port Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
General Configuration Timing				
t_{SMODE}	M[3:0] Setup Time to INITN High	0	—	ns
t_{HMODE}	M[3:0] Hold Time from INITN High	600	—	ns
t_{RW}	RESETN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
t_{PGW}	PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
$f_{ESB_CLK_FRQ}$	System Bus ESB_CLK Frequency (No Wait States)	—	133	MHz
sysCONFIG Master Parallel Configuration Mode				
t_{SMB}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMB}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMB}	RCLK Low Time (Non-compressed Bitstreams)	0.5	0.5	CCLK periods
	RCLK Low Time (Compressed Bitstreams)	0.5	7.5	CCLK periods
t_{CHMB}	RCLK High Time	0.5	0.5	CCLK periods
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CSCK Low	—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low	0	2	µs
t_{SCK}	CSCK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CSCK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN Low to CSCK high Setup Time	—	15	ns
f_{MAXSPI}	Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0)	—	50	MHz
t_{SUSPI}	SOSPI/D0 Data Setup Time Before CSCK	7	—	ns
t_{HSPI}	SOSPI/D0 Data Hold Time After CSCK	2	—	ns
	Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
	Duty Cycle	40	60	%
sysCONFIG Master Serial Configuration Mode				
t_{SMS}	DIN Setup Time	4.4	—	ns
t_{HMS}	DIN Hold Time	0	—	ns
f_{CMS}	CCLK Frequency (No Divider)	90	190	MHz
f_{C_DIV}	CCLK Frequency (Div 128)	0.70	1.48	MHz
t_{D}	CCLK to DOUT Delay	—	7.5	ns
sysCONFIG Master Parallel Configuration Mode				
t_{AVMP}	RCLK to Address Valid	—	10	ns
t_{SMP}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMP}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMP}	RCLK Low Time (Non-compressed Bitstream)	7.5	7.5	CCLK periods
	RCLK Low Time (Compressed Bitstream)	0.5	63.5	
t_{CHMP}	RCLK High Time	0.5	0.5	CCLK periods
t_{DMP}	CCLK to DOUT	—	7.5	ns

Signal Descriptions (Cont.)

Signal Name	I/O	Description
MPI_STRBN	I	Driven active low indicates the start of a transaction on the PowerPC bus. MPI will strobe the address bus at next rising edge of clock.
MPI_ADDR[31:14]	I	Address bus driven by a PowerPC bus master. Only 18-bit width is needed. It has to be the least significant bit of the PowerPC 32-bit address A[31:14].
MPI_DAT[n:0]	I/O	Selectable data bus width from 8, and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
MPI_PAR[m:0]	I/O	Selectable parity bus width from 1, 2, and 3-bit. MPI_DP[0] for MPI_D[7:0], MPI_DP[1] for MPI_D[15:8] and MPI_DP[2] for MPI_D[23:16].
MPI_TA	O	Transfer acknowledge. Driven active low indicates that MPI received the data on the write cycle or returned data on the read cycle.
MPI_TEA	O	Transfer Error Acknowledge. Driven active low indicates that MPI detects a bus error on the internal system bus for current transaction.
MPI_RETRY	O	Active low MPI Retry requests the MPC860 to relinquish the bus and retry the cycle.
Multi-chip Alignment (User I/O if not used.)		
MCA_DONE_OUT	O	Multi-chip alignment done output (to second MCA chip)
MCA_DONE_IN	I	Multi-chip alignment done input (from second MCA chip)
MCA_CLK_P[1:2]_OUT	O	Multi-chip alignment clock [1:2] output (sourced by MCA master chip)
MCA_CLK_P[1:2]_IN	I	Multi-chip alignment clock [1:2] input (from MCA master chip
TEMP	—	Temperature sensing diode pin. Dedicated pin. Accuracy is typically +/- 10°C.
Miscellaneous Dedicated Pins		
XRES	—	External reference resistor between this pin and ground. The reference resistor is used to calibrate the programmable terminating resistors used in the I/Os. Dedicated pin. Value: 1K ± 1% ohm.
DIFFRx	—	Only used if a differential driver is used in a bank. This DIFFRx must be connected to ground via an external 1K ±1% ohm resistor for all banks that have a differential driver.
SERDES Block (Dedicated Pins)		
[A:D]_HDINPx_[L/R]	I	High-speed input (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDINNx_[L/R]	I	High-speed input (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTPx_[L/R]	O	High-speed output (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTNx_[L/R]	O	High-speed output (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_REFCLKP_[L/R]	I	Ref clock input (positive), aux channel on left [L] or right [R] side of device.
[A:D]_REFCLKN_[L/R]	I	Ref clock input (negative), aux channel on left [L] or right [R] side of device.

Pin Information Summary (Cont.)

Pin Type		1152 fcBGA			1704 fcBGA	
		LFSC/M40	LFSC/M80	LFSC/M115	LFSC/M80	LFSC/M115
Single Ended User I/O		604	660	660	904	942
Differential Pair User I/O		302	330	330	452	470
LVDS Output Pairs		78	102	102	114	132
Configuration	Dedicated	11	11	11	11	11
	Muxes/MPI sysBus	72	72	72	72	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		4	4	4	4	4
VCC		44	44	44	76	76
VCC12		52	52	52	88	88
VCCAUX		38	38	38	52	52
VCCIO	Bank 1	10	10	10	10	10
	Bank 2	9	9	9	12	12
	Bank 3	12	12	12	14	14
	Bank 4	12	12	12	14	14
	Bank 5	12	12	12	14	14
	Bank 6	12	12	12	14	14
	Bank 7	9	9	9	12	12
VTT	Bank 2	3	3	3	4	4
	Bank 3	3	3	3	4	4
	Bank 4	3	3	3	5	5
	Bank 5	3	3	3	5	5
	Bank 6	3	3	3	4	4
	Bank 7	3	3	3	4	4
GND		130	130	130	184	184
NC		62	6	6	52	14
Single Ended User / Differential I/O per Bank	Bank 1	80/40	80/40	80/40	80/40	80/40
	Bank 2	60/30	76/38	76/38	96/48	103/51
	Bank 3	96/48	108/54	108/54	132/66	144/72
	Bank 4	106/53	106/53	106/53	184/92	184/92
	Bank 5	106/53	106/53	106/53	184/92	184/92
	Bank 6	96/48	108/54	108/54	132/66	144/72
	Bank 7	60/30	76/38	76/38	96/48	103/51
LVDS Output Pairs Per Bank	Bank 2	15	21	21	24	27
	Bank 3	24	30	30	33	39
	Bank 6	24	30	30	33	39
	Bank 7	15	21	21	24	27
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		108	108	108	212	212
Total		1152	1152	1152	1704	1704

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2]

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F7	A_VDDAX25_L	-		A_VDDAX25_L	-	
B1	A_REFCLKP_L	-		A_REFCLKP_L	-	
C1	A_REFCLKN_L	-		A_REFCLKN_L	-	
D5	VCC12	-		VCC12	-	
A2	RESP_ULC	-		RESP_ULC	-	
E5	VCC12	-		VCC12	-	
D4	VCC12	-		VCC12	-	
H5	RESETN	1		RESETN	1	
H6	TSALLN	1		TSALLN	1	
G6	DONE	1		DONE	1	
G5	INITN	1		INITN	1	
F5	M0	1		M0	1	
F6	M1	1		M1	1	
F4	M2	1		M2	1	
E4	M3	1		M3	1	
D3	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
D2	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
J6	PL15C	7		PL16C	7	
J5	PL15D	7		PL16D	7	
E3	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
E2	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
K4	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
J4	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
F3	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
G3	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
K5	PL18C	7		PL18C	7	
K6	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F2	PL19A	7		PL22A	7	
F1	PL19B	7		PL22B	7	
E1	PL19C	7		PL22C	7	
D1	PL19D	7		PL22D	7	
K3	PL22A	7		PL25A	7	
L3	PL22B	7		PL25B	7	
L6	PL22C	7	VREF1_7	PL25C	7	VREF1_7
M6	PL22D	7	DIFFR_7	PL25D	7	DIFFR_7
J1	PL23A	7	PCLKT7_1	PL26A	7	PCLKT7_1
K1	PL23B	7	PCLKC7_1	PL26B	7	PCLKC7_1
L1	PL24A	7	PCLKT7_0	PL27A	7	PCLKT7_0
M1	PL24B	7	PCLKC7_0	PL27B	7	PCLKC7_0
P8	PL24C	7	PCLKT7_2	PL27C	7	PCLKT7_2
R8	PL24D	7	PCLKC7_2	PL27D	7	PCLKC7_2
N2	PL26A	6	PCLKT6_0	PL29A	6	PCLKT6_0
N1	PL26B	6	PCLKC6_0	PL29B	6	PCLKC6_0
R7	PL26C	6	PCLKT6_1	PL29C	6	PCLKT6_1
R6	PL26D	6	PCLKC6_1	PL29D	6	PCLKC6_1

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
N3	PL27A	6		PL30A	6	
P3	PL27B	6		PL30B	6	
P4	PL27C	6	PCLKT6_3	PL30C	6	PCLKT6_3
P2	PL28A	6		PL31A	6	
R2	PL28B	6		PL31B	6	
T3	PL28C	6	PCLKT6_2	PL31C	6	PCLKT6_2
R3	PL28D	6	PCLKC6_2	PL31D	6	PCLKC6_2
P1	PL31A	6		PL34A	6	
R1	PL31B	6		PL34B	6	
R5	PL31C	6	VREF1_6	PL34C	6	VREF1_6
R4	PL31D	6		PL34D	6	
T2	PL32A	6		PL35A	6	
U2	PL32B	6		PL35B	6	
T1	PL33A	6		PL38A	6	
U1	PL33B	6		PL38B	6	
V1	PL35A	6		PL42A	6	
W1	PL35B	6		PL42B	6	
V6	PL35D	6	DIFFR_6	PL42D	6	DIFFR_6
V2	PL36A	6		PL43A	6	
W2	PL36B	6		PL43B	6	
Y1	PL37A	6		PL44A	6	
AA1	PL37B	6		PL44B	6	
AB1	PL39A	6		PL48A	6	
AC1	PL39B	6		PL48B	6	
Y5	PL40A	6		PL49A	6	
Y6	PL40B	6		PL49B	6	
AD2	PL41A	6		PL51A	6	
AE2	PL41B	6		PL51B	6	
AB5	PL41D	6	VREF2_6	PL51D	6	VREF2_6
AC3	PL43A	6		PL52A	6	
AD3	PL43B	6		PL52B	6	
AF1	PL44A	6		PL55A	6	
AG1	PL44B	6		PL55B	6	
AB6	PL44C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AC5	PL44D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF2	PL45A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG2	PL45B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC6	PL45C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AC7	PL45D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AE4	XRES	-		XRES	-	
AG4	VCC12	-		VCC12	-	
AD5	TEMP	6		TEMP	6	
AF5	VCC12	-		VCC12	-	
AH1	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AJ1	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E16	PT45C	1	D3/MPI_DATA3	PT54C	1	D3/MPI_DATA3
C13	PT45B	1	D2/MPI_DATA2	PT53B	1	D2/MPI_DATA2
C14	PT45A	1	D1/MPI_DATA1	PT53A	1	D1/MPI_DATA1
B14	PT43B	1	D0/MPI_DATA0	PT51B	1	D0/MPI_DATA0
B13	PT43A	1	QOUT/CEON	PT51A	1	QOUT/CEON
L13	PT42D	1	VREF2_1	PT50D	1	VREF2_1
C15	PT42B	1	DOUT	PT50B	1	DOUT
D15	PT42A	1	MCA_DONE_IN	PT50A	1	MCA_DONE_IN
J16	PT41B	1	MCA_CLK_P1_OUT	PT49B	1	MCA_CLK_P1_OUT
K16	PT41A	1	MCA_CLK_P1_IN	PT49A	1	MCA_CLK_P1_IN
H15	PT39D	1	D21/PCLKC1_1/MPI_DATA21	PT47D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT39C	1	D22/PCLKT1_1/MPI_DATA22	PT47C	1	D22/PCLKT1_1/MPI_DATA22
A14	PT39B	1	MCA_CLK_P2_OUT	PT47B	1	MCA_CLK_P2_OUT
A13	PT39A	1	MCA_CLK_P2_IN	PT47A	1	MCA_CLK_P2_IN
G16	PT38D	1	MCA_DONE_OUT	PT46D	1	MCA_DONE_OUT
F16	PT38C	1	BUSYN/RCLK/SCK	PT46C	1	BUSYN/RCLK/SCK
B16	PT38B	1	DP0/MPI_PAR0	PT46B	1	DP0/MPI_PAR0
B15	PT38A	1	MPI_TA	PT46A	1	MPI_TA
L16	PT37C	1	DP2/MPI_PAR2	PT45C	1	DP2/MPI_PAR2
A16	PT37B	1	PCLKC1_0	PT45B	1	PCLKC1_0
A15	PT37A	1	PCLKT1_0/MPI_CLK	PT45A	1	PCLKT1_0/MPI_CLK
L17	PT35C	1	D24/PCLKT1_4/MPI_DATA24	PT43C	1	D24/PCLKT1_4/MPI_DATA24
A17	PT35B	1	MPI_RETRY	PT43B	1	MPI_RETRY
A18	PT35A	1	A0/MPI_ADDR14	PT43A	1	A0/MPI_ADDR14
F17	PT33D	1	A1/MPI_ADDR15	PT42D	1	A1/MPI_ADDR15
G17	PT33C	1	A2/MPI_ADDR16	PT42C	1	A2/MPI_ADDR16
B17	PT33B	1	A3/MPI_ADDR17	PT42B	1	A3/MPI_ADDR17
B18	PT33A	1	A4/MPI_ADDR18	PT42A	1	A4/MPI_ADDR18
H17	PT32D	1	D25/PCLKC1_5/MPI_DATA25	PT41D	1	D25/PCLKC1_5/MPI_DATA25
H18	PT32C	1	D26/PCLKT1_5/MPI_DATA26	PT41C	1	D26/PCLKT1_5/MPI_DATA26
A19	PT32B	1	A5/MPI_ADDR19	PT41B	1	A5/MPI_ADDR19
A20	PT32A	1	A6/MPI_ADDR20	PT41A	1	A6/MPI_ADDR20
L20	PT31C	1	VREF1_1	PT39C	1	VREF1_1
J17	PT31B	1	A7/MPI_ADDR21	PT39B	1	A7/MPI_ADDR21
K17	PT31A	1	A8/MPI_ADDR22	PT39A	1	A8/MPI_ADDR22
C18	PT29B	1	A9/MPI_ADDR23	PT38B	1	A9/MPI_ADDR23
D18	PT29A	1	A10/MPI_ADDR24	PT38A	1	A10/MPI_ADDR24
B19	PT28B	1	A11/MPI_ADDR25	PT37B	1	A11/MPI_ADDR25
B20	PT28A	1	A12/MPI_ADDR26	PT37A	1	A12/MPI_ADDR26
E17	PT27D	1	D11/MPI_DATA11	PT35D	1	D11/MPI_DATA11
E18	PT27C	1	D12/MPI_DATA12	PT35C	1	D12/MPI_DATA12
C20	PT27B	1	A13/MPI_ADDR27	PT35B	1	A13/MPI_ADDR27
C19	PT27A	1	A14/MPI_ADDR28	PT35A	1	A14/MPI_ADDR28
H19	PT25D	1	A16/MPI_ADDR30	PT33D	1	A16/MPI_ADDR30
G19	PT25C	1	D13/MPI_DATA13	PT33C	1	D13/MPI_DATA13
D20	PT25B	1	A15/MPI_ADDR29	PT33B	1	A15/MPI_ADDR29
D19	PT25A	1	A17/MPI_ADDR31	PT33A	1	A17/MPI_ADDR31
H20	PT24D	1	A19/MPI_TSIZ1	PT30D	1	A19/MPI_TSIZ1
G20	PT24C	1	A20/MPI_BDIP	PT30C	1	A20/MPI_BDIP
E19	PT24B	1	A18/MPI_TSIZ0	PT30B	1	A18/MPI_TSIZ0

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B1	GND	-		GND	-	
B32	GND	-		GND	-	
C11	GND	-		GND	-	
C12	GND	-		GND	-	
C16	GND	-		GND	-	
C21	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C25	GND	-		GND	-	
C26	GND	-		GND	-	
C27	GND	-		GND	-	
C29	GND	-		GND	-	
C3	GND	-		GND	-	
C30	GND	-		GND	-	
C4	GND	-		GND	-	
C6	GND	-		GND	-	
C7	GND	-		GND	-	
C8	GND	-		GND	-	
C9	GND	-		GND	-	
D17	GND	-		GND	-	
F18	GND	-		GND	-	
F3	GND	-		GND	-	
F30	GND	-		GND	-	
F9	GND	-		GND	-	
G15	GND	-		GND	-	
G24	GND	-		GND	-	
G29	GND	-		GND	-	
G3	GND	-		GND	-	
J14	GND	-		GND	-	
J22	GND	-		GND	-	
J26	GND	-		GND	-	
J6	GND	-		GND	-	
K11	GND	-		GND	-	
K19	GND	-		GND	-	
K30	GND	-		GND	-	
K4	GND	-		GND	-	
L23	GND	-		GND	-	
L9	GND	-		GND	-	
M13	GND	-		GND	-	
M15	GND	-		GND	-	
M18	GND	-		GND	-	
M20	GND	-		GND	-	
M27	GND	-		GND	-	
M7	GND	-		GND	-	
N12	GND	-		GND	-	
N14	GND	-		GND	-	
N19	GND	-		GND	-	
N21	GND	-		GND	-	
N29	GND	-		GND	-	
N3	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
U12	VCC12	-		VCC12	-	
U21	VCC12	-		VCC12	-	
AA16	VCC12	-		VCC12	-	
AA17	VCC12	-		VCC12	-	
M14	VCC12	-		VCC12	-	
P12	VCC12	-		VCC12	-	
W12	VCC12	-		VCC12	-	
AA14	VCC12	-		VCC12	-	
AA19	VCC12	-		VCC12	-	
W21	VCC12	-		VCC12	-	
P21	VCC12	-		VCC12	-	
M19	VCC12	-		VCC12	-	
A2	GND	-		GND	-	
A10	GND	-		GND	-	
E28	NC	-		NC	-	
E5	NC	-		NC	-	
F10	NC	-		NC	-	
E10	NC	-		NC	-	
E23	NC	-		NC	-	
F23	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M25 and LatticeSC/M40 in a 1020-pin package support a 16-bit MPI interface.

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG18	PB42C	5		PB61C	5	
AF18	PB42D	5		PB61D	5	
AP19	PB43A	5		PB63A	5	
AP18	PB43B	5		PB63B	5	
AJ18	PB43C	5		PB63C	5	
AH18	PB43D	5		PB63D	5	
AP17	PB45A	4		PB65A	4	
AP16	PB45B	4		PB65B	4	
AJ17	PB45C	4		PB65C	4	
AH17	PB45D	4		PB65D	4	
AN17	PB46A	4		PB66A	4	
AN16	PB46B	4		PB66B	4	
AE17	PB46C	4		PB66C	4	
AD17	PB46D	4		PB66D	4	
AK17	PB47A	4		PB67A	4	
AK16	PB47B	4		PB67B	4	
AG17	PB47C	4		PB67C	4	
AF17	PB47D	4		PB67D	4	
AM16	PB49A	4		PB69A	4	
AM15	PB49B	4		PB69B	4	
AJ15	PB49C	4		PB69C	4	
AJ14	PB49D	4		PB69D	4	
AL16	PB50A	4		PB70A	4	
AL15	PB50B	4		PB70B	4	
AG16	PB50C	4		PB70C	4	
AF16	PB50D	4		PB70D	4	
AP15	PB51A	4		PB71A	4	
AP14	PB51B	4		PB71B	4	
AH15	PB51C	4		PB71C	4	
AH14	PB51D	4		PB71D	4	
AN15	PB53A	4	PCLKT4_2	PB74A	4	PCLKT4_2
AN14	PB53B	4	PCLKC4_2	PB74B	4	PCLKC4_2
AE16	PB53C	4	PCLKT4_7	PB74C	4	PCLKT4_7
AD16	PB53D	4	PCLKC4_7	PB74D	4	PCLKC4_7
AK15	PB54A	4	PCLKT4_1	PB75A	4	PCLKT4_1
AK14	PB54B	4	PCLKC4_1	PB75B	4	PCLKC4_1
AG15	PB54C	4	PCLKT4_6	PB75C	4	PCLKT4_6
AG14	PB54D	4	PCLKC4_6	PB75D	4	PCLKC4_6
AM13	PB55A	4	PCLKT4_0	PB77A	4	PCLKT4_0
AM12	PB55B	4	PCLKC4_0	PB77B	4	PCLKC4_0
AJ12	PB55C	4	VREF2_4	PB77C	4	VREF2_4
AJ11	PB55D	4		PB77D	4	
AL13	PB57A	4	PCLKT4_5	PB79A	4	PCLKT4_5
AL12	PB57B	4	PCLKC4_5	PB79B	4	PCLKC4_5
AH12	PB57C	4		PB79C	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP27	PB26A	5	
AP26	PB26B	5	
AK25	PB26C	5	
AK24	PB26D	5	
AN25	PB29A	5	
AN24	PB29B	5	
AE22	PB29C	5	
AE21	PB29D	5	
AM26	PB31A	5	
AM25	PB31B	5	
AF22	PB31C	5	
AF21	PB31D	5	
AN23	PB47A	5	
AN22	PB47B	5	
AP23	PB57A	5	
AP22	PB57B	5	
AG21	PB57C	5	
AG20	PB57D	5	
AP25	PB50A	5	PCLKT5_3
AP24	PB50B	5	PCLKC5_3
AD21	PB50C	5	PCLKT5_4
AD20	PB50D	5	PCLKC5_4
AL23	PB51A	5	PCLKT5_5
AL22	PB51B	5	PCLKC5_5
AH24	PB51C	5	
AH23	PB51D	5	
AM23	PB53A	5	PCLKT5_0
AM22	PB53B	5	PCLKC5_0
AJ24	PB53C	5	
AJ23	PB53D	5	VREF2_5
AN21	PB54A	5	PCLKT5_1
AN20	PB54B	5	PCLKC5_1
AE19	PB54C	5	PCLKT5_6
AD19	PB54D	5	PCLKC5_6
AK21	PB55A	5	PCLKT5_2
AK20	PB55B	5	PCLKC5_2
AK23	PB55C	5	PCLKT5_7
AK22	PB55D	5	PCLKC5_7
AL20	PB58A	5	
AL19	PB58B	5	
AG19	PB58C	5	
AF19	PB58D	5	
AP21	PB61A	5	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J17	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT81B	1	MCA_CLK_P1_OUT
E16	PT81A	1	MCA_CLK_P1_IN
H15	PT78D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT78C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT78B	1	MCA_CLK_P2_OUT
C16	PT78A	1	MCA_CLK_P2_IN
L17	PT75D	1	MCA_DONE_OUT
K17	PT75C	1	BUSYN/RCLK/SCK
E17	PT75B	1	DP0/MPI_PAR0
F17	PT75A	1	MPI_TA
G17	PT73D	1	D23/MPI_DATA23
H17	PT73C	1	DP2/MPI_PAR2
A17	PT73B	1	PCLKC1_0
B17	PT73A	1	PCLKT1_0/MPI_CLK
G18	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT71C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT71B	1	MPI_RETRY
F18	PT71A	1	A0/MPI_ADDR14
J18	PT69D	1	A1/MPI_ADDR15
J19	PT69C	1	A2/MPI_ADDR16
C20	PT69B	1	A3/MPI_ADDR17
C19	PT69A	1	A4/MPI_ADDR18
K18	PT66D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT66C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT66B	1	A5/MPI_ADDR19
E19	PT66A	1	A6/MPI_ADDR20
H19	PT63D	1	D27/MPI_DATA27
H20	PT63C	1	VREF1_1
A18	PT63B	1	A7/MPI_ADDR21
B18	PT63A	1	A8/MPI_ADDR22
H21	PT61D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT61C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT61B	1	A9/MPI_ADDR23
B19	PT61A	1	A10/MPI_ADDR24
H22	PT58D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT58C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT58B	1	A11/MPI_ADDR25
G20	PT58A	1	A12/MPI_ADDR26
K21	PT57D	1	D11/MPI_DATA11
K22	PT57C	1	D12/MPI_DATA12
A20	PT57B	1	A13/MPI_ADDR27
B20	PT57A	1	A14/MPI_ADDR28

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2]

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G34	A_REFCLKP_L	-		A_REFCLKP_L	-	
H34	A_REFCLKN_L	-		A_REFCLKN_L	-	
N30	VCC12	-		VCC12	-	
H33	RESP_ULC	-		RESP_ULC	-	
P25	RESETN	1		RESETN	1	
P26	TSALLN	1		TSALLN	1	
P31	DONE	1		DONE	1	
P23	INITN	1		INITN	1	
P30	M0	1		M0	1	
P22	M1	1		M1	1	
P24	M2	1		M2	1	
R22	M3	1		M3	1	
J37	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J38	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
P32	PL16C	7		PL15C	7	
R32	PL16D	7		PL15D	7	
G40	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
H40	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N33	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P33	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
G41	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
H41	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
T29	PL18C	7		PL18C	7	
U29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
G42	PL20A	7		PL19A	7	
H42	PL20B	7		PL19B	7	
M34	PL20C	7		PL19C	7	
M35	PL20D	7		PL19D	7	
K37	PL21A	7		PL26A	7	
L37	PL21B	7		PL26B	7	
N34	PL21C	7		PL26C	7	
P34	PL21D	7		PL26D	7	
K38	PL22A	7		PL30A	7	
L38	PL22B	7		PL30B	7	
T33	PL22C	7		PL30C	7	
R33	PL22D	7		PL30D	7	
J41	PL24A	7		PL34A	7	
K41	PL24B	7		PL34B	7	
U31	PL24C	7		PL34C	7	
V31	PL24D	7		PL34D	7	
K42	PL25A	7		PL38A	7	
J42	PL25B	7		PL38B	7	
J36	PL25C	7		PL38C	7	
K36	PL25D	7		PL38D	7	
N38	PL26A	7		PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P38	PL26B	7		PL40B	7	
N35	PL26C	7		PL40C	7	
N36	PL26D	7		PL40D	7	
N39	PL29A	7		PL43A	7	
P39	PL29B	7		PL43B	7	
R34	PL29C	7	VREF1_7	PL43C	7	VREF1_7
T34	PL29D	7	DIFFR_7	PL43D	7	DIFFR_7
L41	PL30A	7		PL44A	7	
M41	PL30B	7		PL44B	7	
W29	PL30C	7		PL44C	7	
Y29	PL30D	7		PL44D	7	
L42	PL31A	7		PL45A	7	
M42	PL31B	7		PL45B	7	
U32	PL31C	7		PL45C	7	
V32	PL31D	7		PL45D	7	
R37	PL33A	7		PL47A	7	
T37	PL33B	7		PL47B	7	
M36	PL33C	7		PL47C	7	
M37	PL33D	7		PL47D	7	
P40	PL34A	7		PL48A	7	
N40	PL34B	7		PL48B	7	
R35	PL34C	7		PL48C	7	
T35	PL34D	7		PL48D	7	
N41	PL35A	7		PL49A	7	
P41	PL35B	7		PL49B	7	
V33	PL35C	7		PL49C	7	
U33	PL35D	7		PL49D	7	
R38	PL37A	7		PL51A	7	
T38	PL37B	7		PL51B	7	
R36	PL37C	7		PL51C	7	
T36	PL37D	7		PL51D	7	
N42	PL38A	7		PL52A	7	
P42	PL38B	7		PL52B	7	
Y31	PL38C	7		PL52C	7	
AA31	PL38D	7		PL52D	7	
U37	PL39A	7		PL53A	7	
V37	PL39B	7		PL53B	7	
U34	PL39C	7		PL53C	7	
V34	PL39D	7		PL53D	7	
U39	PL41A	7		PL55A	7	
T39	PL41B	7		PL55B	7	
V35	PL41C	7		PL55C	7	
W35	PL41D	7		PL55D	7	
R41	PL42A	7		PL56A	7	
T41	PL42B	7		PL56B	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P

Date	Version	Section	Change Summary
March 2007 (cont.)	01.5 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Internal Timing Parameters with ispLEVER 6.1 SP1 results.
			Updated t_{FDEL} and t_{CDEL} specifications.
			Updated LatticeSC Family Timing Adders with ispLEVER 6.1 SP1 results.
			Updated PLL specifications to expand frequency range down to 2 MHz and break out jitter for the different ranges.
			Added footnote to sysCLOCK PLL Timing table specifying the conditions for the jitter measurements.
			Added t_{DLL} specification to sysCLOCK DLL Timing table.
			Added footnote to sysCLOCK DLL Timing table specifying the conditions for the jitter measurements.
			Added sysCONFIG Master Parallel Configuration Mode and sysCONFIG SPI Port to LatticeSC sysCONFIG Port Timing table.
		Pin Information	Updated Pin Information Summary with SC40 information.
			Updated LFSC25 Logic Signal Connections: FF1020 with SC40 information.
			Updated LFSC80 Logic Signal Connections: FC1152 with SC40 information.
August 2007	01.6	General	Changed references of "HDC" to "HDC/SI".
			Changed references of "LDCN" to "LDCN/SCS".
			Changed references of "BUSYN/RCLK" to "BUSYN/RCLK/SCK".
			Changed references of "RDCFGN" to "TSALLN".
			Changed references of "TDO/RDDATA" to "TDO".
		Architecture	Updated text in Ripple Mode section.
			Added information to Global Set/Reset.
			Added information for Spread Spectrum Clocking
			Modified information for PLL/DLL Cascading. DLL to PLL is now supported.
			Modified AIL Block text and figure.
			Modified Figure 2-20 DDR/Shift Register Block.
			Added Information to Hot Socketing.
			Added new information for I/O Architecture Rules.
			Added information to SERDES Power Supply Sequencing Requirements.
		DC and Switching Characteristics	Added footnote to Hot Socketing Specifications table.
			Modified Initialization and Standby Supply Current table.
			Modified GSR Timing table.
			Modified sysCLOCK DLL Timing table to include $I_{DUTY.}$
			Deleted Readback Timing information from sysCONFIG Port Timing table.
			Modified data in External Switching Characteristics table.
		Pin Information	Added information to the Signal Descriptions table for HDC/SI, LDCN/SCS.
			Added footnote to Signal Descriptions table.
			Modified Description for signal BUSYN/RCLK/SCK.
			Modified data in Pin Information Summary and device-specific Pinout Information tables.