# Lattice Semiconductor Corporation - LFSC3GA15E-6F256C Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 3750 |
| Number of Logic Elements/Cells | 15000 |
| Total RAM Bits | 1054720 |
| Number of I/O | 139 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga15e-6f256c |

DLLs and dynamic glitch free clock MUXs which are required in today's high end system designs. High-speed, high-bandwidth I/O make this family ideal for high-throughput systems.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeSC family of FPGA devices. Synthesis library support for LatticeSC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeSC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeSC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Innovative high-performance FPGA architecture, high-speed SERDES with PCS support, sysMEM embedded memory and high performance I/O are combined in the LatticeSC to provide excellent performance for today's leading edge systems designs. Table 1-3 details the performance of several common functions implemented within the LatticeSC.

***Table1-3. Speed Performance for Typical Functions[1]***

| Functions | Performance (MHz)[2] |
|---|---|
| 32-bit Address Decoder | 539 |
| 64-bit Address Decoder | 517 |
| 32:1 Multiplexer | 779 |
| 64-bit Adder (ripple) | 353 |
| 32x8 Distributed Single Port (SP) RAM | 768 |
| 64-bit Counter (up or down counter, non-loadable) | 369 |
| True Dual-Port 1024x18 bits | 372 |
| FIFO Port A: x36 bits, B: x9 bits | 375 |

1. For additional information, see Typical Building BLock Function Performance table in this data sheet.
2. Advance information (-7 speed grade).

## Initialization and Standby Supply Current

The table below indicates initialization and standby supply current while operating at 85°C junction temperature ($T_J$), which is the high end of the commercial temperature range, and 105°C, which is the high end of the industrial temperature range. This data assumes all outputs are tri-stated and all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND. The remaining SERDES supply current for $V_{DDIB}$ and $V_{DDOB}$ is detailed in the SERDES section of this data sheet. For power at your design temperature, it is recommended to use the Power Calculator tool which is accessible in ispLEVER or can be used as a standalone tool. For more information on supply current, see the reference to additional technical documentation available at the end of this data sheet.

**Over Recommended Operating Conditions**

| Symbol | Condition | Parameter | Device | 25°C Typ.[1] | 85°C Max.[2] | | 105°C Max.[2] | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | All | -5, -6 | -7 | -5, -6 | |
| $I_{CC}$ | (VCC = 1.2V +/- 5%) | Core Operating Power Supply Current | LFSC/M15 | 65 | 449 | 678 | 755 | mA |
| | | | LFSC/M25 | 113 | 798 | 1255 | 1343 | mA |
| | | | LFSC/M40 | 159 | 1178 | 2006 | 1981 | mA |
| | | | LFSC/M80 | 276 | 2122 | 3827 | 3569 | mA |
| | | | LFSC/M115 | 454 | 3376 | — | 5679 | mA |
| | (VCC = 1.0V +/- 5%) | Core Operating Power Supply Current | LFSC/M15 | 45 | 312 | 471 | 524 | mA |
| | | | LFSC/M25 | 79 | 554 | 872 | 933 | mA |
| | | | LFSC/M40 | 110 | 818 | 1393 | 1375 | mA |
| | | | LFSC/M80 | 191 | 1473 | 2658 | 2478 | mA |
| | | | LFSC/M115 | 315 | 2344 | — | 3943 | mA |
| $I_{CC12}$ | | 1.2V Power Supply Current for Configuration Logic, FPGA PLL, SERDES PLL and SERDES Analog Supplies | LFSC/M15 | 23 | 39 | 59 | 35 | mA |
| | | | LFSC/M25 | 25 | 50 | 78 | 56 | mA |
| | | | LFSC/M40 | 31 | 78 | 133 | 89 | mA |
| | | | LFSC/M80 | 50 | 108 | 195 | 123 | mA |
| | | | LFSC/M115 | 65 | 131 | — | 154 | mA |
| $I_{CCAUX}$ | | Auxiliary Operating Power Supply Current | LFSC/M15 | 7 | 12 | 19 | 14 | mA |
| | | | LFSC/M25 | 9 | 16 | 25 | 18 | mA |
| | | | LFSC/M40 | 12 | 23 | 39 | 25 | mA |
| | | | LFSC/M80 | 13 | 25 | 45 | 23 | mA |
| | | | LFSC/M115 | 16 | 27 | — | 26 | mA |
| $I_{CCIO}$ and $I_{CCJ}$ | | Bank Power Supply Current (per bank) | LFSC/M15 | 0.1 | 0.2 | 0.3 | 0.2 | mA |
| | | | LFSC/M25 | 0.3 | 0.6 | 1.0 | 0.7 | mA |
| | | | LFSC/M40 | 0.4 | 0.9 | 1.5 | 1.0 | mA |
| | | | LFSC/M80 | 0.5 | 1.1 | 2.1 | 1.3 | mA |
| | | | LFSC/M115 | 0.7 | 1.5 | — | 1.8 | mA |

1. $I_{CC}$ is specified at $T_J$ = 25°C and typical $V_{CC}$.
2. $I_{CC}$ is specified at the respective commercial and industrial maximum $T_J$ and $V_{CC}$ limits.

## PURESPEED I/O Recommended Operating Conditions

| Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVCMOS 33 | 3.135 | 3.3 | 3.465 | — | — | — |
| LVCMOS 25 | 2.375 | 2.5 | 2.625 | — | — | — |
| LVCMOS 18 | 1.71 | 1.8 | 1.89 | — | — | — |
| LVCMOS 15 | 1.425 | 1.5 | 1.575 | — | — | — |
| LVCMOS 12 | 1.14 | 1.2 | 1.26 | — | — | — |
| LVTTL | 3.135 | 3.3 | 3.465 | — | — | — |
| PCI33 | 3.135 | 3.3 | 3.465 | — | — | — |
| PCIX33 | 3.135 | 3.3 | 3.465 | — | — | — |
| PCIX15 | 1.425 | 1.5 | 1.575 | $0.49V_{CCIO}$ | $0.5V_{CCIO}$ | $0.51V_{CCIO}$ |
| AGP1X33 | 3.135 | 3.3 | 3.465 | — | — | — |
| AGP2X33 | 3.135 | 3.3 | 3.465 | $0.39V_{CCIO}$ | $0.4V_{CCIO}$ | $0.41V_{CCIO}$ |
| SSTL18_I, II[3] | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL25_I, II[3] | 2.375 | 2.5 | 2.625 | 1.15 | 1.25 | 1.35 |
| SSTL33_I, II[3] | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| HSTL15_I, II[3] | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| HSTL15_III[1, 3] and IV[1, 3] | 1.425 | 1.5 | 1.575 | 0.68 | 0.9 | 0.9 |
| HSTL 18_I[3], II[3] | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| HSTL 18_ III[1, 3], IV[1, 3] | 1.71 | 1.8 | 1.89 | 0.816 | 1.08 | 1.08 |
| GTL12[1, 3], GTLPLUS15[1, 3] | — | — | — | 0.882 | 1.0 | 1.122 |
| LVDS | — | — | — | — | — | — |
| Mini-LVDS | — | — | — | — | — | — |
| RSDS | — | — | — | — | — | — |
| LVPECL33 (outputs)[2] | 3.135 | 3.3 | 3.465 | — | — | — |
| LVPECL33 (inputs)[2, 4] | — | ≤ 2.5 | — | — | — | — |
| BLVDS25[2, 3] | 2.375 | 2.5 | 2.625 | — | — | — |
| MLVDS25[2, 3] | 2.375 | 2.5 | 2.625 | — | — | — |
| SSTL18D_I[3], II[3] | 1.71 | 1.8 | 1.89 | — | — | — |
| SSTL25D_I[3], II[3] | 2.375 | 2.5 | 2.625 | — | — | — |
| SSTL33D_I[3], II[3] | 3.135 | 3.3 | 3.465 | — | — | — |
| HSTL15D_I[3], II[3] | 1.425 | 1.5 | 1.575 | — | — | — |
| HSTL18D_I[3], II[3] | 1.71 | 1.8 | 1.89 | — | — | — |

1. Input only.
2. Inputs on chip. Outputs are implemented with the addition of external resisters.
3. Input for this standard does not depend on the value of $V_{CCIO}$.
4. Inputs for this standard cannot be in 3.3V VCCIO banks (≤ 2.5V only).

## LVPECL

The LatticeSC devices support differential LVPECL standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

***Figure 3-3. Differential LVPECL***

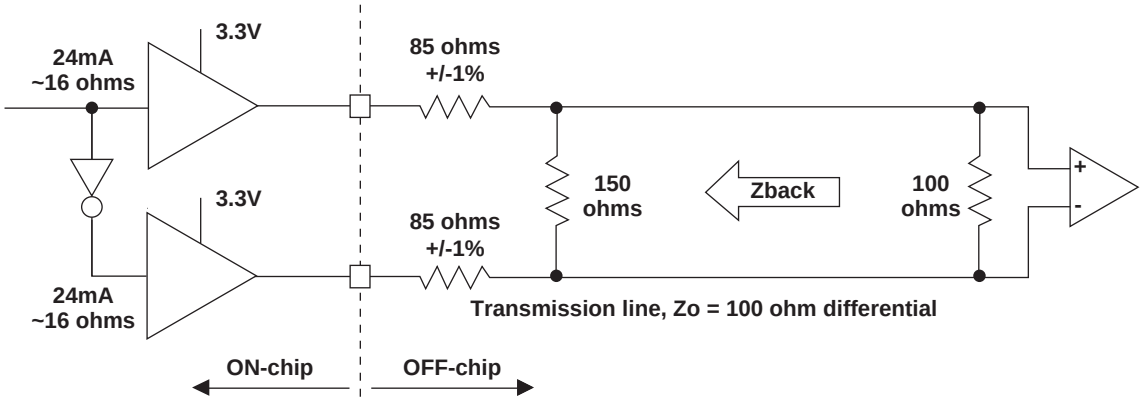


***Table 3-3. LVPECL DC Conditions[1]***

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 16 | ohm |
| $R_S$ | Driver series resistor | 85 | ohm |
| $R_P$ | Driver parallel resistor | 150 | ohm |
| $R_T$ | Receiver termination | 100 | ohm |
| $V_{OH}$ | Output high voltage | 2.03 | V |
| $V_{OL}$ | Output low voltage | 1.27 | V |
| $V_{OD}$ | Output differential voltage | 0.76 | V |
| $V_{CM}$ | Output common mode voltage | 1.65 | V |
| $Z_{BACK}$ | Back impedance | 86 | ohm |
| $I_{DC}$ | DC output current | 12.6 | mA |

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS, MLVDS and other differential interfaces please see details of additional technical documentation at the end of this data sheet.

# On-die Differential Common Mode Termination

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $C_{CMT}$ | Capacitance $V_{CMT}$ to GND | — | 40 | — | pF |

# LatticeSC/M sysCONFIG Port Timing

**Over Recommended Operating Conditions**

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| **General Configuration Timing** | | | | |
| $t_{SMODE}$ | M[3:0] Setup Time to INITN High | 0 | — | ns |
| $t_{HMODE}$ | M[3:0] Hold Time from INITN High | 600 | — | ns |
| $t_{RW}$ | RESETN Pulse Width Low to Start Reconfiguration (1.2 V) | 50 (or 100 at 0.95V) | — | ns |
| $t_{PGW}$ | PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V) | 50 (or 100 at 0.95V) | — | ns |
| $f_{ESB\_CLK\_FRQ}$ | System Bus ESB_CLK Frequency (No Wait States) | — | 133 | MHz |
| **sysCONFIG Master Parallel Configuration Mode** | | | | |
| $t_{SMB}$ | D[7:0] Setup Time to RCLK High | 6 | — | ns |
| $t_{HMB}$ | D[7:0] Hold Time to RCLK High | 0 | — | ns |
| $t_{CLMB}$ | RCLK Low Time (Non-compressed Bitstreams) | 0.5 | 0.5 | CCLK periods |
| | RCLK Low Time (Compressed Bitstreams) | 0.5 | 7.5 | CCLK periods |
| $t_{CHMB}$ | RCLK High Time | 0.5 | 0.5 | CCLK periods |
| **sysCONFIG SPI Port** | | | | |
| $t_{CFGX}$ | INITN High to CSCK Low | — | 80 | ns |
| $t_{CSSPI}$ | INITN High to CSSPIN Low | 0 | 2 | µs |
| $t_{SCK}$ | CSCK Low before CSSPIN Low | 0 | — | ns |
| $t_{SOCDO}$ | CSCK Low to Output Valid | — | 15 | ns |
| $t_{CSPID}$ | CSSPIN Low to CSCK high Setup Time | — | 15 | ns |
| $f_{MAXSPI}$ | Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0) | — | 50 | MHz |
| $t_{SUSPI}$ | SOSPI/D0 Data Setup Time Before CSCK | 7 | — | ns |
| $t_{HSPI}$ | SOSPI/D0 Data Hold Time After CSCK | 2 | — | ns |
| | Master Clock Frequency | Selected value - 30% | Selected value + 30% | MHz |
| | Duty Cycle | 40 | 60 | % |
| **sysCONFIG Master Serial Configuration Mode** | | | | |
| $t_{SMS}$ | DIN Setup Time | 4.4 | — | ns |
| $t_{HMS}$ | DIN Hold Time | 0 | — | ns |
| $f_{CMS}$ | CCLK Frequency (No Divider) | 90 | 190 | MHz |
| $f_{C\_DIV}$ | CCLK Frequency (Div 128) | 0.70 | 1.48 | MHz |
| $t_{D}$ | CCLK to DOUT Delay | — | 7.5 | ns |
| **sysCONFIG Master Parallel Configuration Mode** | | | | |
| $t_{AVMP}$ | RCLK to Address Valid | — | 10 | ns |
| $t_{SMP}$ | D[7:0] Setup Time to RCLK High | 6 | — | ns |
| $t_{HMP}$ | D[7:0] Hold Time to RCLK High | 0 | — | ns |
| $t_{CLMP}$ | RCLK Low Time (Non-compressed Bitstream) | 7.5 | 7.5 | CCLK periods |
| | RCLK Low Time (Compressed Bitstream) | 0.5 | 63.5 | |
| $t_{CHMP}$ | RCLK High Time | 0.5 | 0.5 | CCLK periods |
| $t_{DMP}$ | CCLK to DOUT | — | 7.5 | ns |

## LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

| Ball Number | LFSC/M15 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| M4 | PL43B | 6 | |
| P1 | PL45A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E |
| R1 | PL45B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E |
| R2 | XRES | - | |
| P3 | TEMP | 6 | |
| R3 | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B |
| N4 | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B |
| T3 | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| T2 | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| N5 | PB5D | 5 | VREF1_5 |
| P5 | PB8A | 5 | |
| R5 | PB8B | 5 | |
| T4 | PB9A | 5 | |
| T5 | PB9B | 5 | |
| R6 | PB12A | 5 | PCLKT5_3 |
| T6 | PB12B | 5 | PCLKC5_3 |
| L5 | PB13C | 5 | |
| P6 | PB15A | 5 | PCLKT5_0 |
| T7 | PB15B | 5 | PCLKC5_0 |
| M7 | PB15D | 5 | VREF2_5 |
| R8 | PB16A | 5 | PCLKT5_1 |
| T8 | PB16B | 5 | PCLKC5_1 |
| N7 | PB17A | 5 | PCLKT5_2 |
| N8 | PB17B | 5 | PCLKC5_2 |
| R9 | PB20A | 5 | |
| T9 | PB20B | 5 | |
| M8 | PB21A | 5 | |
| M9 | PB21B | 5 | |
| P8 | PB24A | 5 | |
| P9 | PB24B | 5 | |
| T10 | PB28A | 4 | |
| R11 | PB28B | 4 | |
| N9 | PB31A | 4 | |
| N10 | PB31B | 4 | |
| T11 | PB32A | 4 | |
| R12 | PB32B | 4 | |
| P11 | PB35A | 4 | PCLKT4_2 |
| M10 | PB35B | 4 | PCLKC4_2 |
| T12 | PB36A | 4 | PCLKT4_1 |
| P12 | PB36B | 4 | PCLKC4_1 |
| T13 | PB37A | 4 | PCLKT4_0 |
| T14 | PB37B | 4 | PCLKC4_0 |
| R15 | PB37C | 4 | VREF2_4 |

## LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2]

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| F7 | A_VDDAX25_L | - | | A_VDDAX25_L | - | |
| B1 | A_REFCLKP_L | - | | A_REFCLKP_L | - | |
| C1 | A_REFCLKN_L | - | | A_REFCLKN_L | - | |
| D5 | VCC12 | - | | VCC12 | - | |
| A2 | RESP_ULC | - | | RESP_ULC | - | |
| E5 | VCC12 | - | | VCC12 | - | |
| D4 | VCC12 | - | | VCC12 | - | |
| H5 | RESETN | 1 | | RESETN | 1 | |
| H6 | TSALLN | 1 | | TSALLN | 1 | |
| G6 | DONE | 1 | | DONE | 1 | |
| G5 | INITN | 1 | | INITN | 1 | |
| F5 | M0 | 1 | | M0 | 1 | |
| F6 | M1 | 1 | | M1 | 1 | |
| F4 | M2 | 1 | | M2 | 1 | |
| E4 | M3 | 1 | | M3 | 1 | |
| D3 | PL15A | 7 | ULC_PLLT_IN_A/ULC_PLLT_FB_B | PL16A | 7 | ULC_PLLT_IN_A/ULC_PLLT_FB_B |
| D2 | PL15B | 7 | ULC_PLLC_IN_A/ULC_PLLC_FB_B | PL16B | 7 | ULC_PLLC_IN_A/ULC_PLLC_FB_B |
| J6 | PL15C | 7 | | PL16C | 7 | |
| J5 | PL15D | 7 | | PL16D | 7 | |
| E3 | PL17A | 7 | ULC_DLLT_IN_C/ULC_DLLT_FB_D | PL17A | 7 | ULC_DLLT_IN_C/ULC_DLLT_FB_D |
| E2 | PL17B | 7 | ULC_DLLC_IN_C/ULC_DLLC_FB_D | PL17B | 7 | ULC_DLLC_IN_C/ULC_DLLC_FB_D |
| K4 | PL17C | 7 | ULC_PLLT_IN_B/ULC_PLLT_FB_A | PL17C | 7 | ULC_PLLT_IN_B/ULC_PLLT_FB_A |
| J4 | PL17D | 7 | ULC_PLLC_IN_B/ULC_PLLC_FB_A | PL17D | 7 | ULC_PLLC_IN_B/ULC_PLLC_FB_A |
| F3 | PL18A | 7 | ULC_DLLT_IN_D/ULC_DLLT_FB_C | PL18A | 7 | ULC_DLLT_IN_D/ULC_DLLT_FB_C |
| G3 | PL18B | 7 | ULC_DLLC_IN_D/ULC_DLLC_FB_C | PL18B | 7 | ULC_DLLC_IN_D/ULC_DLLC_FB_C |
| K5 | PL18C | 7 | | PL18C | 7 | |
| K6 | PL18D | 7 | VREF2_7 | PL18D | 7 | VREF2_7 |
| F2 | PL19A | 7 | | PL22A | 7 | |
| F1 | PL19B | 7 | | PL22B | 7 | |
| E1 | PL19C | 7 | | PL22C | 7 | |
| D1 | PL19D | 7 | | PL22D | 7 | |
| K3 | PL22A | 7 | | PL25A | 7 | |
| L3 | PL22B | 7 | | PL25B | 7 | |
| L6 | PL22C | 7 | VREF1_7 | PL25C | 7 | VREF1_7 |
| M6 | PL22D | 7 | DIFFR_7 | PL25D | 7 | DIFFR_7 |
| J1 | PL23A | 7 | PCLKT7_1 | PL26A | 7 | PCLKT7_1 |
| K1 | PL23B | 7 | PCLKC7_1 | PL26B | 7 | PCLKC7_1 |
| L1 | PL24A | 7 | PCLKT7_0 | PL27A | 7 | PCLKT7_0 |
| M1 | PL24B | 7 | PCLKC7_0 | PL27B | 7 | PCLKC7_0 |
| P8 | PL24C | 7 | PCLKT7_2 | PL27C | 7 | PCLKT7_2 |
| R8 | PL24D | 7 | PCLKC7_2 | PL27D | 7 | PCLKC7_2 |
| N2 | PL26A | 6 | PCLKT6_0 | PL29A | 6 | PCLKT6_0 |
| N1 | PL26B | 6 | PCLKC6_0 | PL29B | 6 | PCLKC6_0 |
| R7 | PL26C | 6 | PCLKT6_1 | PL29C | 6 | PCLKT6_1 |
| R6 | PL26D | 6 | PCLKC6_1 | PL29D | 6 | PCLKC6_1 |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| A29 | RESP_URC | - | | RESP_URC | - | |
| D26 | VCC12 | - | | VCC12 | - | |
| C30 | A_REFCLKN_R | - | | A_REFCLKN_R | - | |
| B30 | A_REFCLKP_R | - | | A_REFCLKP_R | - | |
| F24 | A_VDDAX25_R | - | | A_VDDAX25_R | - | |
| D25 | VCC12 | - | | VCC12 | - | |
| C28 | A_VDDIB0_R | - | | A_VDDIB0_R | - | |
| B28 | A_HDINP0_R | - | PCS 3E0 CH 0 IN P | A_HDINP0_R | - | PCS 3E0 CH 0 IN P |
| B27 | A_HDINN0_R | - | PCS 3E0 CH 0 IN N | A_HDINN0_R | - | PCS 3E0 CH 0 IN N |
| E25 | VCC12 | - | | VCC12 | - | |
| A28 | A_HDOUTP0_R | - | PCS 3E0 CH 0 OUT P | A_HDOUTP0_R | - | PCS 3E0 CH 0 OUT P |
| C27 | A_VDDOB0_R | - | | A_VDDOB0_R | - | |
| A27 | A_HDOUTN0_R | - | PCS 3E0 CH 0 OUT N | A_HDOUTN0_R | - | PCS 3E0 CH 0 OUT N |
| C26 | A_VDDOB1_R | - | | A_VDDOB1_R | - | |
| A26 | A_HDOUTN1_R | - | PCS 3E0 CH 1 OUT N | A_HDOUTN1_R | - | PCS 3E0 CH 1 OUT N |
| D24 | VCC12 | - | | VCC12 | - | |
| A25 | A_HDOUTP1_R | - | PCS 3E0 CH 1 OUT P | A_HDOUTP1_R | - | PCS 3E0 CH 1 OUT P |
| B26 | A_HDINN1_R | - | PCS 3E0 CH 1 IN N | A_HDINN1_R | - | PCS 3E0 CH 1 IN N |
| B25 | A_HDINP1_R | - | PCS 3E0 CH 1 IN P | A_HDINP1_R | - | PCS 3E0 CH 1 IN P |
| E24 | VCC12 | - | | VCC12 | - | |
| C25 | A_VDDIB1_R | - | | A_VDDIB1_R | - | |
| D23 | VCC12 | - | | VCC12 | - | |
| C24 | A_VDDIB2_R | - | | A_VDDIB2_R | - | |
| B24 | A_HDINP2_R | - | PCS 3E0 CH 2 IN P | A_HDINP2_R | - | PCS 3E0 CH 2 IN P |
| B23 | A_HDINN2_R | - | PCS 3E0 CH 2 IN N | A_HDINN2_R | - | PCS 3E0 CH 2 IN N |
| E23 | VCC12 | - | | VCC12 | - | |
| A24 | A_HDOUTP2_R | - | PCS 3E0 CH 2 OUT P | A_HDOUTP2_R | - | PCS 3E0 CH 2 OUT P |
| C23 | A_VDDOB2_R | - | | A_VDDOB2_R | - | |
| A23 | A_HDOUTN2_R | - | PCS 3E0 CH 2 OUT N | A_HDOUTN2_R | - | PCS 3E0 CH 2 OUT N |
| C22 | A_VDDOB3_R | - | | A_VDDOB3_R | - | |
| A22 | A_HDOUTN3_R | - | PCS 3E0 CH 3 OUT N | A_HDOUTN3_R | - | PCS 3E0 CH 3 OUT N |
| D22 | VCC12 | - | | VCC12 | - | |
| A21 | A_HDOUTP3_R | - | PCS 3E0 CH 3 OUT P | A_HDOUTP3_R | - | PCS 3E0 CH 3 OUT P |
| B22 | A_HDINN3_R | - | PCS 3E0 CH 3 IN N | A_HDINN3_R | - | PCS 3E0 CH 3 IN N |
| B21 | A_HDINP3_R | - | PCS 3E0 CH 3 IN P | A_HDINP3_R | - | PCS 3E0 CH 3 IN P |
| E22 | VCC12 | - | | VCC12 | - | |
| C21 | A_VDDIB3_R | - | | A_VDDIB3_R | - | |
| G22 | PT43D | 1 | HDC/SI | PT49D | 1 | HDC/SI |
| F22 | PT43C | 1 | LDCN/SCS | PT49C | 1 | LDCN/SCS |
| B20 | PT41B | 1 | D8/MPI_DATA8 | PT49B | 1 | D8/MPI_DATA8 |
| B19 | PT41A | 1 | CS1/MPI_CS1 | PT49A | 1 | CS1/MPI_CS1 |
| A20 | PT40D | 1 | D9/MPI_DATA9 | PT47D | 1 | D9/MPI_DATA9 |
| A19 | PT40C | 1 | D10/MPI_DATA10 | PT47C | 1 | D10/MPI_DATA10 |
| D19 | PT39B | 1 | CS0N/MPI_CS0N | PT47B | 1 | CS0N/MPI_CS0N |
| D18 | PT39A | 1 | RDN/MPI_STRB_N | PT47A | 1 | RDN/MPI_STRB_N |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AH11 | PB47C | 4 | PCLKT4_6 | PB54C | 4 | PCLKT4_6 |
| AH10 | PB47D | 4 | PCLKC4_6 | PB54D | 4 | PCLKC4_6 |
| AK12 | PB49A | 4 | PCLKT4_0 | PB55A | 4 | PCLKT4_0 |
| AJ12 | PB49B | 4 | PCLKC4_0 | PB55B | 4 | PCLKC4_0 |
| AF14 | PB49C | 4 | VREF2_4 | PB55C | 4 | VREF2_4 |
| AE14 | PB49D | 4 | | PB55D | 4 | |
| AL11 | PB51A | 4 | PCLKT4_5 | PB57A | 4 | PCLKT4_5 |
| AL10 | PB51B | 4 | PCLKC4_5 | PB57B | 4 | PCLKC4_5 |
| AH9 | PB51C | 4 | | PB57C | 4 | |
| AH8 | PB51D | 4 | | PB57D | 4 | |
| AK11 | PB52A | 4 | PCLKT4_3 | PB58A | 4 | PCLKT4_3 |
| AJ11 | PB52B | 4 | PCLKC4_3 | PB58B | 4 | PCLKC4_3 |
| AH7 | PB52C | 4 | PCLKT4_4 | PB58C | 4 | PCLKT4_4 |
| AH6 | PB52D | 4 | PCLKC4_4 | PB58D | 4 | PCLKC4_4 |
| AK8 | PB53A | 4 | | PB67A | 4 | |
| AJ8 | PB53B | 4 | | PB67B | 4 | |
| AF11 | PB53C | 4 | | PB67C | 4 | |
| AD12 | PB55A | 4 | | PB69A | 4 | |
| AE12 | PB55B | 4 | | PB69B | 4 | |
| AM6 | PB56A | 4 | | PB70A | 4 | |
| AM5 | PB56B | 4 | | PB70B | 4 | |
| AC12 | PB56C | 4 | | PB70C | 4 | |
| AL6 | PB57A | 4 | | PB73A | 4 | |
| AL5 | PB57B | 4 | | PB73B | 4 | |
| AG7 | PB59A | 4 | | PB74A | 4 | |
| AG8 | PB59B | 4 | | PB74B | 4 | |
| AK6 | PB60A | 4 | | PB75A | 4 | |
| AJ6 | PB60B | 4 | | PB75B | 4 | |
| AF10 | PB60C | 4 | | PB75C | 4 | |
| AE11 | PB60D | 4 | | PB75D | 4 | |
| AM4 | PB61A | 4 | | PB77A | 4 | |
| AM3 | PB61B | 4 | | PB77B | 4 | |
| AH5 | PB63A | 4 | | PB78A | 4 | |
| AH4 | PB63B | 4 | | PB78B | 4 | |
| AK5 | PB64A | 4 | | PB79A | 4 | |
| AJ5 | PB64B | 4 | | PB79B | 4 | |
| AF8 | PB64C | 4 | | PB79C | 4 | |
| AF7 | PB64D | 4 | | PB79D | 4 | |
| AL4 | PB65A | 4 | | PB81A | 4 | |
| AL3 | PB65B | 4 | | PB81B | 4 | |
| AG5 | PB65C | 4 | | PB81C | 4 | |
| AF6 | PB65D | 4 | | PB81D | 4 | |
| AK3 | PB67A | 4 | | PB82A | 4 | |
| AJ3 | PB67B | 4 | | PB82B | 4 | |
| AE10 | PB67C | 4 | VREF1_4 | PB82C | 4 | VREF1_4 |
| AD10 | PB67D | 4 | | PB82D | 4 | |
| AL2 | PB68A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D | PB83A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D |
| AK2 | PB68B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D | PB83B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D |
| AE9 | PB68C | 4 | | PB83C | 4 | |
| AE8 | PB68D | 4 | | PB83D | 4 | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| Y6 | PR42D | 3 | DIFFR_3 | PR51D | 3 | DIFFR_3 |
| W6 | PR42C | 3 | | PR51C | 3 | |
| Y2 | PR42B | 3 | | PR51B | 3 | |
| W2 | PR42A | 3 | | PR51A | 3 | |
| W7 | PR40D | 3 | | PR49D | 3 | |
| V8 | PR40C | 3 | | PR49C | 3 | |
| W4 | PR40B | 3 | | PR49B | 3 | |
| W3 | PR40A | 3 | | PR49A | 3 | |
| V5 | PR39D | 3 | | PR48D | 3 | |
| U6 | PR39C | 3 | | PR48C | 3 | |
| V3 | PR39B | 3 | | PR48B | 3 | |
| V4 | PR39A | 3 | | PR48A | 3 | |
| V10 | PR38D | 3 | | PR47D | 3 | |
| V9 | PR38C | 3 | | PR47C | 3 | |
| V2 | PR38B | 3 | | PR47B | 3 | |
| V1 | PR38A | 3 | | PR47A | 3 | |
| U8 | PR36D | 3 | | PR45D | 3 | |
| U7 | PR36C | 3 | | PR45C | 3 | |
| U2 | PR36B | 3 | | PR45B | 3 | |
| U1 | PR36A | 3 | | PR45A | 3 | |
| U5 | PR35D | 3 | | PR44D | 3 | |
| T6 | PR35C | 3 | | PR44C | 3 | |
| T1 | PR35B | 3 | | PR44B | 3 | |
| T2 | PR35A | 3 | | PR44A | 3 | |
| U9 | PR34D | 3 | | PR43D | 3 | |
| U10 | PR34C | 3 | VREF1_3 | PR43C | 3 | VREF1_3 |
| R1 | PR34B | 3 | | PR43B | 3 | |
| R2 | PR34A | 3 | | PR43A | 3 | |
| T7 | PR31D | 3 | PCLKC3_2 | PR40D | 3 | PCLKC3_2 |
| T8 | PR31C | 3 | PCLKT3_2 | PR40C | 3 | PCLKT3_2 |
| R4 | PR31B | 3 | | PR40B | 3 | |
| R3 | PR31A | 3 | | PR40A | 3 | |
| T5 | PR30D | 3 | PCLKC3_3 | PR39D | 3 | PCLKC3_3 |
| R5 | PR30C | 3 | PCLKT3_3 | PR39C | 3 | PCLKT3_3 |
| P2 | PR30B | 3 | | PR39B | 3 | |
| P1 | PR30A | 3 | | PR39A | 3 | |
| T9 | PR29D | 3 | PCLKC3_1 | PR38D | 3 | PCLKC3_1 |
| T10 | PR29C | 3 | PCLKT3_1 | PR38C | 3 | PCLKT3_1 |
| P4 | PR29B | 3 | PCLKC3_0 | PR38B | 3 | PCLKC3_0 |
| P3 | PR29A | 3 | PCLKT3_0 | PR38A | 3 | PCLKT3_0 |
| P5 | PR27D | 2 | PCLKC2_2 | PR36D | 2 | PCLKC2_2 |
| P6 | PR27C | 2 | PCLKT2_2 | PR36C | 2 | PCLKT2_2 |
| N1 | PR27B | 2 | PCLKC2_0 | PR36B | 2 | PCLKC2_0 |
| N2 | PR27A | 2 | PCLKT2_0 | PR36A | 2 | PCLKT2_0 |
| R9 | PR26D | 2 | PCLKC2_3 | PR35D | 2 | PCLKC2_3 |
| R8 | PR26C | 2 | PCLKT2_3 | PR35C | 2 | PCLKT2_3 |
| M1 | PR26B | 2 | PCLKC2_1 | PR35B | 2 | PCLKC2_1 |
| L1 | PR26A | 2 | PCLKT2_1 | PR35A | 2 | PCLKT2_1 |
| N9 | PR25D | 2 | DIFFR_2 | PR23D | 2 | DIFFR_2 |
| M9 | PR25C | 2 | VREF1_2 | PR23C | 2 | VREF1_2 |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| B30 | A_HDOUTN0_L | - | PCS 360 CH 0 OUT N | A_HDOUTN0_L | - | PCS 360 CH 0 OUT N |
| D30 | A_VDDOB0_L | - | | A_VDDOB0_L | - | |
| A30 | A_HDOUTP0_L | - | PCS 360 CH 0 OUT P | A_HDOUTP0_L | - | PCS 360 CH 0 OUT P |
| C31 | A_HDINN0_L | - | PCS 360 CH 0 IN N | A_HDINN0_L | - | PCS 360 CH 0 IN N |
| C32 | A_HDINP0_L | - | PCS 360 CH 0 IN P | A_HDINP0_L | - | PCS 360 CH 0 IN P |
| B31 | A_VDDIB0_L | - | | A_VDDIB0_L | - | |
| AL25 | NC | - | | PB26A | 5 | |
| AL24 | NC | - | | PB26B | 5 | |
| AG27 | NC | - | | PB26C | 5 | |
| AH27 | NC | - | | PB26D | 5 | |
| AM25 | NC | - | | PB27A | 5 | |
| AM24 | NC | - | | PB27B | 5 | |
| AL9 | NC | - | | PB62A | 4 | |
| AL8 | NC | - | | PB62B | 4 | |
| AK9 | NC | - | | PB63A | 4 | |
| AJ9 | NC | - | | PB63B | 4 | |
| AG10 | NC | - | | PB63C | 4 | |
| AG11 | NC | - | | PB63D | 4 | |
| J30 | NC | - | | PL26A | 7 | |
| H30 | NC | - | | PL26B | 7 | |
| M28 | NC | - | | PL26C | 7 | |
| N28 | NC | - | | PL26D | 7 | |
| J32 | NC | - | | PL27A | 7 | |
| J31 | NC | - | | PL27B | 7 | |
| N26 | NC | - | | PL27C | 7 | |
| N27 | NC | - | | PL27D | 7 | |
| K31 | NC | - | | PL29A | 7 | |
| K32 | NC | - | | PL29B | 7 | |
| P25 | NC | - | | PL29C | 7 | |
| P26 | NC | - | | PL29D | 7 | |
| L27 | NC | - | | PL22C | 7 | |
| L28 | NC | - | | PL22D | 7 | |
| M29 | NC | - | | PL30A | 7 | |
| L29 | NC | - | | PL30B | 7 | |
| M30 | NC | - | | PL31A | 7 | |
| L30 | NC | - | | PL31B | 7 | |
| L31 | NC | - | | PL34A | 7 | |
| M31 | NC | - | | PL34B | 7 | |
| AA29 | NC | - | | PL56A | 6 | |
| AA30 | NC | - | | PL56B | 6 | |
| AB31 | NC | - | | PL57A | 6 | |
| AA31 | NC | - | | PL57B | 6 | |
| AG30 | NC | - | | PL57C | 6 | |
| AG29 | NC | - | | PL57D | 6 | |
| AB29 | NC | - | | PL58A | 6 | |
| AB30 | NC | - | | PL58B | 6 | |
| Y25 | NC | - | | PL58C | 6 | |
| AA25 | NC | - | | PL58D | 6 | |
| AA8 | NC | - | | PR58D | 3 | |
| Y8 | NC | - | | PR58C | 3 | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| C2 | VCCJ | - | | VCCJ | - | |
| M9 | TDO | - | TDO | TDO | - | TDO |
| L9 | TMS | - | | TMS | - | |
| D1 | TCK | - | | TCK | - | |
| C1 | TDI | - | | TDI | - | |
| J8 | PROGRAMN | 1 | | PROGRAMN | 1 | |
| K8 | MPIIRQN | 1 | CFGIRQN/MPI_IRQ_N | MPIIRQN | 1 | CFGIRQN/MPI_IRQ_N |
| B2 | CCLK | 1 | | CCLK | 1 | |
| H9 | RESP_URC | - | | RESP_URC | - | |
| H10 | VCC12 | - | | VCC12 | - | |
| H8 | A_REFCLKN_R | - | | A_REFCLKN_R | - | |
| G8 | A_REFCLKP_R | - | | A_REFCLKP_R | - | |
| C3 | VCC12 | - | | VCC12 | - | |
| D3 | A_VDDIB0_R | - | | A_VDDIB0_R | - | |
| A3 | A_HDINP0_R | - | PCS 3E0 CH 0 IN P | A_HDINP0_R | - | PCS 3E0 CH 0 IN P |
| B3 | A_HDINN0_R | - | PCS 3E0 CH 0 IN N | A_HDINN0_R | - | PCS 3E0 CH 0 IN N |
| E5 | VCC12 | - | | VCC12 | - | |
| A4 | A_HDOUTP0_R | - | PCS 3E0 CH 0 OUT P | A_HDOUTP0_R | - | PCS 3E0 CH 0 OUT P |
| F6 | A_VDDOB0_R | - | | A_VDDOB0_R | - | |
| B4 | A_HDOUTN0_R | - | PCS 3E0 CH 0 OUT N | A_HDOUTN0_R | - | PCS 3E0 CH 0 OUT N |
| F7 | A_VDDOB1_R | - | | A_VDDOB1_R | - | |
| B5 | A_HDOUTN1_R | - | PCS 3E0 CH 1 OUT N | A_HDOUTN1_R | - | PCS 3E0 CH 1 OUT N |
| E6 | VCC12 | - | | VCC12 | - | |
| A5 | A_HDOUTP1_R | - | PCS 3E0 CH 1 OUT P | A_HDOUTP1_R | - | PCS 3E0 CH 1 OUT P |
| B6 | A_HDINN1_R | - | PCS 3E0 CH 1 IN N | A_HDINN1_R | - | PCS 3E0 CH 1 IN N |
| A6 | A_HDINP1_R | - | PCS 3E0 CH 1 IN P | A_HDINP1_R | - | PCS 3E0 CH 1 IN P |
| C6 | VCC12 | - | | VCC12 | - | |
| D4 | A_VDDIB1_R | - | | A_VDDIB1_R | - | |
| C7 | VCC12 | - | | VCC12 | - | |
| D5 | A_VDDIB2_R | - | | A_VDDIB2_R | - | |
| A7 | A_HDINP2_R | - | PCS 3E0 CH 2 IN P | A_HDINP2_R | - | PCS 3E0 CH 2 IN P |
| B7 | A_HDINN2_R | - | PCS 3E0 CH 2 IN N | A_HDINN2_R | - | PCS 3E0 CH 2 IN N |
| E7 | VCC12 | - | | VCC12 | - | |
| A8 | A_HDOUTP2_R | - | PCS 3E0 CH 2 OUT P | A_HDOUTP2_R | - | PCS 3E0 CH 2 OUT P |
| F8 | A_VDDOB2_R | - | | A_VDDOB2_R | - | |
| B8 | A_HDOUTN2_R | - | PCS 3E0 CH 2 OUT N | A_HDOUTN2_R | - | PCS 3E0 CH 2 OUT N |
| F9 | A_VDDOB3_R | - | | A_VDDOB3_R | - | |
| B9 | A_HDOUTN3_R | - | PCS 3E0 CH 3 OUT N | A_HDOUTN3_R | - | PCS 3E0 CH 3 OUT N |
| E8 | VCC12 | - | | VCC12 | - | |
| A9 | A_HDOUTP3_R | - | PCS 3E0 CH 3 OUT P | A_HDOUTP3_R | - | PCS 3E0 CH 3 OUT P |
| B10 | A_HDINN3_R | - | PCS 3E0 CH 3 IN N | A_HDINN3_R | - | PCS 3E0 CH 3 IN N |
| A10 | A_HDINP3_R | - | PCS 3E0 CH 3 IN P | A_HDINP3_R | - | PCS 3E0 CH 3 IN P |
| C10 | VCC12 | - | | VCC12 | - | |
| D6 | A_VDDIB3_R | - | | A_VDDIB3_R | - | |
| G10 | VCC12 | - | | VCC12 | - | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| W30 | PL69B | 6 | |
| W27 | PL69C | 6 | VREF1_6 |
| Y27 | PL69D | 6 | |
| T33 | PL70A | 6 | |
| U33 | PL70B | 6 | |
| V25 | PL70C | 6 | |
| W25 | PL70D | 6 | |
| U34 | PL71A | 6 | |
| V34 | PL71B | 6 | |
| V26 | PL71C | 6 | |
| W26 | PL71D | 6 | |
| V33 | PL74A | 6 | |
| W33 | PL74B | 6 | |
| V24 | PL74C | 6 | |
| W24 | PL74D | 6 | |
| W31 | PL77A | 6 | |
| Y31 | PL77B | 6 | |
| Y29 | PL77C | 6 | |
| AA29 | PL77D | 6 | |
| Y33 | PL79A | 6 | |
| AA33 | PL79B | 6 | |
| Y28 | PL79C | 6 | |
| AA28 | PL79D | 6 | |
| AB32 | PL90A | 6 | |
| AC32 | PL90B | 6 | |
| AA26 | PL90C | 6 | |
| AA27 | PL90D | 6 | DIFFR_6 |
| AB31 | PL91A | 6 | |
| AC31 | PL91B | 6 | |
| Y24 | PL91C | 6 | |
| AA24 | PL91D | 6 | |
| AE34 | PL92A | 6 | |
| AF34 | PL92B | 6 | |
| AB30 | PL92C | 6 | |
| AC30 | PL92D | 6 | |
| AD33 | PL94A | 6 | |
| AE33 | PL94B | 6 | |
| AD30 | PL94C | 6 | |
| AE30 | PL94D | 6 | |
| AE32 | PL96A | 6 | |
| AF32 | PL96B | 6 | |
| AA25 | PL96C | 6 | |
| AB25 | PL96D | 6 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AP41 | PL91B | 6 | | PL112B | 6 | |
| AK35 | PL91C | 6 | | PL112C | 6 | |
| AL35 | PL91D | 6 | | PL112D | 6 | |
| AN38 | PL93A | 6 | | PL115A | 6 | |
| AP38 | PL93B | 6 | | PL115B | 6 | |
| AL37 | PL93C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F | PL115C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F |
| AM37 | PL93D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F | PL115D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F |
| AR41 | PL94A | 6 | | PL116A | 6 | |
| AT41 | PL94B | 6 | | PL116B | 6 | |
| AN37 | PL94C | 6 | | PL116C | 6 | |
| AP37 | PL94D | 6 | | PL116D | 6 | |
| AR39 | PL95A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E | PL117A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E |
| AR40 | PL95B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E | PL117B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E |
| AN36 | PL95C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A | PL117C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A |
| AP36 | PL95D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A | PL117D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A |
| AT40 | XRES | - | | XRES | - | |
| AU41 | TEMP | 6 | | TEMP | 6 | |
| AU42 | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B |
| AV42 | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B |
| AL33 | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| AL34 | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| AU38 | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C |
| AV38 | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C |
| AM34 | PB4C | 5 | | PB4C | 5 | |
| AM33 | PB4D | 5 | | PB4D | 5 | |
| AV41 | PB5A | 5 | | PB5A | 5 | |
| AW41 | PB5B | 5 | | PB5B | 5 | |
| AK30 | PB5C | 5 | | PB5C | 5 | |
| AK29 | PB5D | 5 | VREF1_5 | PB5D | 5 | VREF1_5 |
| AW42 | PB7A | 5 | | PB7A | 5 | |
| AY42 | PB7B | 5 | | PB7B | 5 | |
| AR37 | PB7C | 5 | | PB7C | 5 | |
| AR38 | PB7D | 5 | | PB7D | 5 | |
| AV40 | PB8A | 5 | | PB9A | 5 | |
| AV39 | PB8B | 5 | | PB9B | 5 | |
| AN35 | PB8C | 5 | | PB9C | 5 | |
| AN34 | PB8D | 5 | | PB9D | 5 | |
| AW40 | PB9A | 5 | | PB11A | 5 | |
| AY40 | PB9B | 5 | | PB11B | 5 | |
| AP34 | PB9C | 5 | | PB11C | 5 | |
| AP35 | PB9D | 5 | | PB11D | 5 | |
| AW39 | PB11A | 5 | | PB12A | 5 | |
| AW38 | PB11B | 5 | | PB12B | 5 | |
| AL32 | PB11C | 5 | | PB12C | 5 | |
| AL31 | PB11D | 5 | | PB12D | 5 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AY41 | PB12A | 5 | | PB13A | 5 | |
| BA41 | PB12B | 5 | | PB13B | 5 | |
| AT39 | PB12C | 5 | | PB13C | 5 | |
| AT38 | PB12D | 5 | | PB13D | 5 | |
| AV37 | PB13A | 5 | | PB15A | 5 | |
| AV36 | PB13B | 5 | | PB15B | 5 | |
| AM31 | PB13C | 5 | | PB15C | 5 | |
| AM32 | PB13D | 5 | | PB15D | 5 | |
| BA40 | PB15A | 5 | | PB16A | 5 | |
| BB40 | PB15B | 5 | | PB16B | 5 | |
| AM29 | PB15C | 5 | | PB16C | 5 | |
| AL29 | PB15D | 5 | | PB16D | 5 | |
| AY39 | PB16A | 5 | | PB17A | 5 | |
| AY38 | PB16B | 5 | | PB17B | 5 | |
| AN33 | PB16C | 5 | | PB17C | 5 | |
| AN32 | PB16D | 5 | | PB17D | 5 | |
| BA39 | PB17A | 5 | | PB19A | 5 | |
| BA38 | PB17B | 5 | | PB19B | 5 | |
| AT37 | PB17C | 5 | | PB19C | 5 | |
| AT36 | PB17D | 5 | | PB19D | 5 | |
| AW36 | PB19A | 5 | | PB20A | 5 | |
| AW35 | PB19B | 5 | | PB20B | 5 | |
| AM28 | PB19C | 5 | | PB20C | 5 | |
| AL28 | PB19D | 5 | | PB20D | 5 | |
| BB38 | PB20A | 5 | | PB21A | 5 | |
| BB39 | PB20B | 5 | | PB21B | 5 | |
| AR34 | PB20C | 5 | | PB21C | 5 | |
| AR33 | PB20D | 5 | | PB21D | 5 | |
| AV35 | PB21A | 5 | | PB23A | 5 | |
| AV34 | PB21B | 5 | | PB23B | 5 | |
| AT33 | PB21C | 5 | | PB23C | 5 | |
| AT34 | PB21D | 5 | | PB23D | 5 | |
| BA37 | PB23A | 5 | | PB25A | 5 | |
| BA36 | PB23B | 5 | | PB25B | 5 | |
| AP33 | PB23C | 5 | | PB25C | 5 | |
| AP32 | PB23D | 5 | | PB25D | 5 | |
| AY36 | PB24A | 5 | | PB26A | 5 | |
| AY35 | PB24B | 5 | | PB26B | 5 | |
| AN31 | PB24C | 5 | | PB26C | 5 | |
| AN30 | PB24D | 5 | | PB26D | 5 | |
| BB37 | PB25A | 5 | | PB27A | 5 | |
| BB36 | PB25B | 5 | | PB27B | 5 | |
| AP31 | PB25C | 5 | | PB27C | 5 | |
| AP30 | PB25D | 5 | | PB27D | 5 | |
| AV33 | PB27A | 5 | | PB29A | 5 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AP8 | PB117D | 4 | | PB131D | 4 | |
| AY3 | PB119A | 4 | | PB133A | 4 | |
| AW3 | PB119B | 4 | | PB133B | 4 | |
| AR6 | PB119C | 4 | | PB133C | 4 | |
| AR5 | PB119D | 4 | | PB133D | 4 | |
| AU5 | PB120A | 4 | | PB134A | 4 | |
| AV5 | PB120B | 4 | | PB134B | 4 | |
| AL12 | PB120C | 4 | | PB134C | 4 | |
| AL11 | PB120D | 4 | | PB134D | 4 | |
| AV3 | PB121A | 4 | | PB135A | 4 | |
| AV4 | PB121B | 4 | | PB135B | 4 | |
| AN9 | PB121C | 4 | | PB135C | 4 | |
| AN8 | PB121D | 4 | | PB135D | 4 | |
| AW1 | PB123A | 4 | | PB138A | 4 | |
| AY1 | PB123B | 4 | | PB138B | 4 | |
| AK14 | PB123C | 4 | VREF1_4 | PB138C | 4 | VREF1_4 |
| AK13 | PB123D | 4 | | PB138D | 4 | |
| AV2 | PB124A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D | PB139A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D |
| AW2 | PB124B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D | PB139B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D |
| AM10 | PB124C | 4 | | PB139C | 4 | |
| AM9 | PB124D | 4 | | PB139D | 4 | |
| AV1 | PB125A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B | PB141A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B |
| AU1 | PB125B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B | PB141B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B |
| AL10 | PB125C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C | PB141C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C |
| AL9 | PB125D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C | PB141D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C |
| AT3 | PROBE_VCC | - | | PROBE_VCC | - | |
| AU2 | PROBE_GND | - | | PROBE_GND | - | |
| AP7 | PR95D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A | PR117D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A |
| AN7 | PR95C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A | PR117C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A |
| AR3 | PR95B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E | PR117B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E |
| AR4 | PR95A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E | PR117A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E |
| AP6 | PR94D | 3 | | PR116D | 3 | |
| AN6 | PR94C | 3 | | PR116C | 3 | |
| AT2 | PR94B | 3 | | PR116B | 3 | |
| AR2 | PR94A | 3 | | PR116A | 3 | |
| AM6 | PR93D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F | PR115D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F |
| AL6 | PR93C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F | PR115C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F |
| AP5 | PR93B | 3 | | PR115B | 3 | |
| AN5 | PR93A | 3 | | PR115A | 3 | |
| AL8 | PR91D | 3 | | PR112D | 3 | |
| AK8 | PR91C | 3 | | PR112C | 3 | |
| AP2 | PR91B | 3 | | PR112B | 3 | |
| AN2 | PR91A | 3 | | PR112A | 3 | |
| AJ12 | PR90D | 3 | | PR109D | 3 | |
| AH12 | PR90C | 3 | | PR109C | 3 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| D1 | A_HDINN0_R | - | PCS 3E0 CH 0 IN N | A_HDINN0_R | - | PCS 3E0 CH 0 IN N |
| F1 | VCC12 | - | | VCC12 | - | |
| A3 | A_HDOUTP0_R | - | PCS 3E0 CH 0 OUT P | A_HDOUTP0_R | - | PCS 3E0 CH 0 OUT P |
| E1 | A_VDDOB0_R | - | | A_VDDOB0_R | - | |
| B3 | A_HDOUTN0_R | - | PCS 3E0 CH 0 OUT N | A_HDOUTN0_R | - | PCS 3E0 CH 0 OUT N |
| C2 | A_VDDOB1_R | - | | A_VDDOB1_R | - | |
| A4 | A_HDOUTN1_R | - | PCS 3E0 CH 1 OUT N | A_HDOUTN1_R | - | PCS 3E0 CH 1 OUT N |
| B2 | VCC12 | - | | VCC12 | - | |
| B4 | A_HDOUTP1_R | - | PCS 3E0 CH 1 OUT P | A_HDOUTP1_R | - | PCS 3E0 CH 1 OUT P |
| E3 | A_HDINN1_R | - | PCS 3E0 CH 1 IN N | A_HDINN1_R | - | PCS 3E0 CH 1 IN N |
| D3 | A_HDINP1_R | - | PCS 3E0 CH 1 IN P | A_HDINP1_R | - | PCS 3E0 CH 1 IN P |
| M10 | VCC12 | - | | VCC12 | - | |
| E2 | A_VDDIB1_R | - | | A_VDDIB1_R | - | |
| J11 | VCC12 | - | | VCC12 | - | |
| M11 | A_VDDIB2_R | - | | A_VDDIB2_R | - | |
| D4 | A_HDINP2_R | - | PCS 3E0 CH 2 IN P | A_HDINP2_R | - | PCS 3E0 CH 2 IN P |
| E4 | A_HDINN2_R | - | PCS 3E0 CH 2 IN N | A_HDINN2_R | - | PCS 3E0 CH 2 IN N |
| K9 | VCC12 | - | | VCC12 | - | |
| A5 | A_HDOUTP2_R | - | PCS 3E0 CH 2 OUT P | A_HDOUTP2_R | - | PCS 3E0 CH 2 OUT P |
| D2 | A_VDDOB2_R | - | | A_VDDOB2_R | - | |
| B5 | A_HDOUTN2_R | - | PCS 3E0 CH 2 OUT N | A_HDOUTN2_R | - | PCS 3E0 CH 2 OUT N |
| L10 | A_VDDOB3_R | - | | A_VDDOB3_R | - | |
| B6 | A_HDOUTN3_R | - | PCS 3E0 CH 3 OUT N | A_HDOUTN3_R | - | PCS 3E0 CH 3 OUT N |
| G6 | VCC12 | - | | VCC12 | - | |
| A6 | A_HDOUTP3_R | - | PCS 3E0 CH 3 OUT P | A_HDOUTP3_R | - | PCS 3E0 CH 3 OUT P |
| E5 | A_HDINN3_R | - | PCS 3E0 CH 3 IN N | A_HDINN3_R | - | PCS 3E0 CH 3 IN N |
| D5 | A_HDINP3_R | - | PCS 3E0 CH 3 IN P | A_HDINP3_R | - | PCS 3E0 CH 3 IN P |
| K12 | VCC12 | - | | VCC12 | - | |
| L13 | A_VDDIB3_R | - | | A_VDDIB3_R | - | |
| N14 | VCC12 | - | | VCC12 | - | |
| F9 | B_VDDIB0_R | - | | B_VDDIB0_R | - | |
| D6 | B_HDINP0_R | - | PCS 3E1 CH 0 IN P | B_HDINP0_R | - | PCS 3E1 CH 0 IN P |
| E6 | B_HDINN0_R | - | PCS 3E1 CH 0 IN N | B_HDINN0_R | - | PCS 3E1 CH 0 IN N |
| J8 | VCC12 | - | | VCC12 | - | |
| B7 | B_HDOUTP0_R | - | PCS 3E1 CH 0 OUT P | B_HDOUTP0_R | - | PCS 3E1 CH 0 OUT P |
| G4 | B_VDDOB0_R | - | | B_VDDOB0_R | - | |
| A7 | B_HDOUTN0_R | - | PCS 3E1 CH 0 OUT N | B_HDOUTN0_R | - | PCS 3E1 CH 0 OUT N |
| K8 | B_VDDOB1_R | - | | B_VDDOB1_R | - | |
| A8 | B_HDOUTN1_R | - | PCS 3E1 CH 1 OUT N | B_HDOUTN1_R | - | PCS 3E1 CH 1 OUT N |
| L9 | VCC12 | - | | VCC12 | - | |
| B8 | B_HDOUTP1_R | - | PCS 3E1 CH 1 OUT P | B_HDOUTP1_R | - | PCS 3E1 CH 1 OUT P |
| E7 | B_HDINN1_R | - | PCS 3E1 CH 1 IN N | B_HDINN1_R | - | PCS 3E1 CH 1 IN N |
| D7 | B_HDINP1_R | - | PCS 3E1 CH 1 IN P | B_HDINP1_R | - | PCS 3E1 CH 1 IN P |
| F10 | VCC12 | - | | VCC12 | - | |
| K13 | B_VDDIB1_R | - | | B_VDDIB1_R | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| L8 | VCCIO2 | - | | VCCIO2 | - | |
| M3 | VCCIO2 | - | | VCCIO2 | - | |
| P7 | VCCIO2 | - | | VCCIO2 | - | |
| R4 | VCCIO2 | - | | VCCIO2 | - | |
| T12 | VCCIO2 | - | | VCCIO2 | - | |
| U8 | VCCIO2 | - | | VCCIO2 | - | |
| V3 | VCCIO2 | - | | VCCIO2 | - | |
| W11 | VCCIO2 | - | | VCCIO2 | - | |
| Y7 | VCCIO2 | - | | VCCIO2 | - | |
| AB3 | VCCIO3 | - | | VCCIO3 | - | |
| AC7 | VCCIO3 | - | | VCCIO3 | - | |
| AD11 | VCCIO3 | - | | VCCIO3 | - | |
| AE4 | VCCIO3 | - | | VCCIO3 | - | |
| AF8 | VCCIO3 | - | | VCCIO3 | - | |
| AG12 | VCCIO3 | - | | VCCIO3 | - | |
| AH3 | VCCIO3 | - | | VCCIO3 | - | |
| AJ7 | VCCIO3 | - | | VCCIO3 | - | |
| AK11 | VCCIO3 | - | | VCCIO3 | - | |
| AL4 | VCCIO3 | - | | VCCIO3 | - | |
| AM8 | VCCIO3 | - | | VCCIO3 | - | |
| AP3 | VCCIO3 | - | | VCCIO3 | - | |
| AR7 | VCCIO3 | - | | VCCIO3 | - | |
| AU4 | VCCIO3 | - | | VCCIO3 | - | |
| AL16 | VCCIO4 | - | | VCCIO4 | - | |
| AM13 | VCCIO4 | - | | VCCIO4 | - | |
| AM19 | VCCIO4 | - | | VCCIO4 | - | |
| AR11 | VCCIO4 | - | | VCCIO4 | - | |
| AR17 | VCCIO4 | - | | VCCIO4 | - | |
| AT14 | VCCIO4 | - | | VCCIO4 | - | |
| AT20 | VCCIO4 | - | | VCCIO4 | - | |
| AT8 | VCCIO4 | - | | VCCIO4 | - | |
| AW15 | VCCIO4 | - | | VCCIO4 | - | |
| AW21 | VCCIO4 | - | | VCCIO4 | - | |
| AW9 | VCCIO4 | - | | VCCIO4 | - | |
| AY12 | VCCIO4 | - | | VCCIO4 | - | |
| AY18 | VCCIO4 | - | | VCCIO4 | - | |
| AY6 | VCCIO4 | - | | VCCIO4 | - | |
| AL27 | VCCIO5 | - | | VCCIO5 | - | |
| AM24 | VCCIO5 | - | | VCCIO5 | - | |
| AM30 | VCCIO5 | - | | VCCIO5 | - | |
| AR26 | VCCIO5 | - | | VCCIO5 | - | |
| AR32 | VCCIO5 | - | | VCCIO5 | - | |
| AT23 | VCCIO5 | - | | VCCIO5 | - | |
| AT29 | VCCIO5 | - | | VCCIO5 | - | |
| AT35 | VCCIO5 | - | | VCCIO5 | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AH22 | VTT_5 | 5 | | VTT_5 | 5 | |
| AJ22 | VTT_5 | 5 | | VTT_5 | 5 | |
| AJ23 | VTT_5 | 5 | | VTT_5 | 5 | |
| AJ24 | VTT_5 | 5 | | VTT_5 | 5 | |
| AJ25 | VTT_5 | 5 | | VTT_5 | 5 | |
| AB28 | VTT_6 | 6 | | VTT_6 | 6 | |
| AB29 | VTT_6 | 6 | | VTT_6 | 6 | |
| AE29 | VTT_6 | 6 | | VTT_6 | 6 | |
| AJ30 | VTT_6 | 6 | | VTT_6 | 6 | |
| AA28 | VTT_7 | 7 | | VTT_7 | 7 | |
| AA29 | VTT_7 | 7 | | VTT_7 | 7 | |
| R31 | VTT_7 | 7 | | VTT_7 | 7 | |
| V29 | VTT_7 | 7 | | VTT_7 | 7 | |
| Y24 | GND | - | | GND | - | |
| Y26 | GND | - | | GND | - | |
| Y8 | GND | - | | GND | - | |
| Y35 | GND | - | | GND | - | |
| AA16 | VCC12 | - | | VCC12 | - | |
| AA27 | VCC12 | - | | VCC12 | - | |
| AB16 | VCC12 | - | | VCC12 | - | |
| AB27 | VCC12 | - | | VCC12 | - | |
| AF16 | VCC12 | - | | VCC12 | - | |
| AF27 | VCC12 | - | | VCC12 | - | |
| AG17 | VCC12 | - | | VCC12 | - | |
| AG21 | VCC12 | - | | VCC12 | - | |
| G33 | NC | - | | NC | - | |
| G10 | NC | - | | NC | - | |
| M15 | NC | - | | NC | - | |
| L15 | NC | - | | NC | - | |
| K16 | NC | - | | NC | - | |
| J16 | NC | - | | NC | - | |
| M18 | NC | - | | NC | - | |
| L18 | NC | - | | NC | - | |
| M25 | NC | - | | NC | - | |
| L25 | NC | - | | NC | - | |
| J27 | NC | - | | NC | - | |
| K27 | NC | - | | NC | - | |
| L28 | NC | - | | NC | - | |
| M28 | NC | - | | NC | - | |

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M80 and LatticeSC/M115 in a 1704-pin package supports a 32-bit MPI interface.

**Industrial, Cont.**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA115E-6FCN1152I[1] | -6 | Lead-Free Ceramic fcBGA | 1152 | IND | 115.2 |
| LFSC3GA115E-5FCN1152I[1] | -5 | Lead-Free Ceramic fcBGA | 1152 | IND | 115.2 |
| LFSC3GA115E-6FFN1152I | -6 | Lead-Free Organic fcBGA | 1152 | IND | 115.2 |
| LFSC3GA115E-5FFN1152I | -5 | Lead-Free Organic fcBGA | 1152 | IND | 115.2 |
| LFSC3GA115E-6FCN1704I[1] | -6 | Lead-Free Ceramic fcBGA | 1704 | IND | 115.2 |
| LFSC3GA115E-5FCN1704I[1] | -5 | Lead-Free Ceramic fcBGA | 1704 | IND | 115.2 |
| LFSC3GA115E-6FFN1704I | -6 | Lead-Free Organic fcBGA | 1704 | IND | 115.2 |
| LFSC3GA115E-5FFN1704I | -5 | Lead-Free Organic fcBGA | 1704 | IND | 115.2 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA115EP1-6FCN1152I[1] | -6 | Lead-Free Ceramic fcBGA | 1152 | IND | 115.2 |
| LFSCM3GA115EP1-5FCN1152I[1] | -5 | Lead-Free Ceramic fcBGA | 1152 | IND | 115.2 |
| LFSCM3GA115EP1-6FFN1152I | -6 | Lead-Free Organic fcBGA | 1152 | IND | 115.2 |
| LFSCM3GA115EP1-5FFN1152I | -5 | Lead-Free Organic fcBGA | 1152 | IND | 115.2 |
| LFSCM3GA115EP1-6FCN1704I[1] | -6 | Lead-Free Ceramic fcBGA | 1704 | IND | 115.2 |
| LFSCM3GA115EP1-5FCN1704I[1] | -5 | Lead-Free Ceramic fcBGA | 1704 | IND | 115.2 |
| LFSCM3GA115EP1-6FFN1704I | -6 | Lead-Free Organic fcBGA | 1704 | IND | 115.2 |
| LFSCM3GA115EP1-5FFN1704I | -5 | Lead-Free Organic fcBGA | 1704 | IND | 115.2 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.