Lattice Semiconductor Corporation - LFSC3GA15E-7F256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3750
Number of Logic Elements/Cells	15000
Total RAM Bits	1054720
Number of I/O	139
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga15e-7f256c

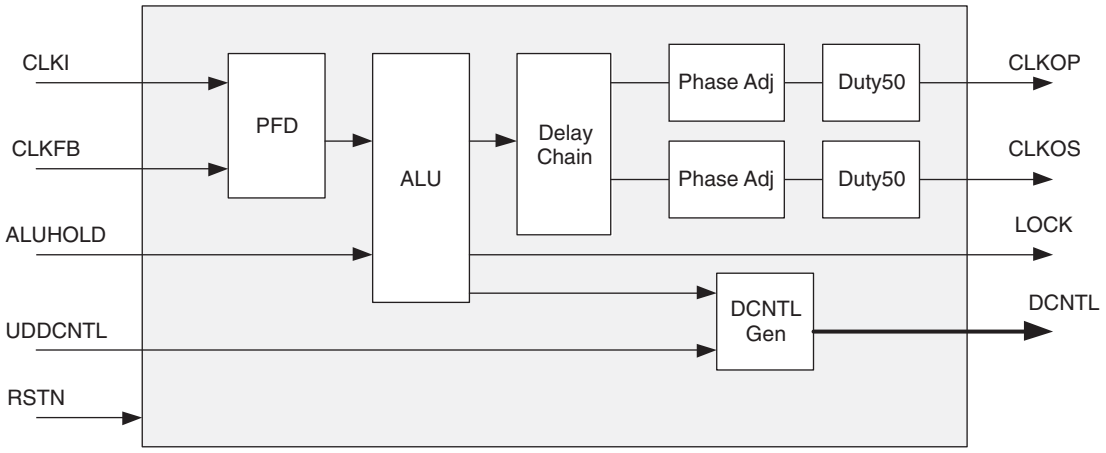
There is a Digital Control (DCNTL) bus available from the DLL block. This Digital Control bus is available to the delay lines in the PIC blocks in the adjacent banks. The UDDCNTL signal allows the user to latch the current value on the digital control bus.

Figure 2-12 shows the DLL block diagram of the DLL inputs and outputs. The output of the phase frequency detector controls an arithmetic logic unit (ALU) to add or subtract one delay tap. The digital output of this ALU is used to control the delay value of the delay chain and this digital code is transmitted via the DCNTL bus.

The sysCLOCK DLL can be configured at power-up, then, if desired, reconfigured dynamically through the Serial Memory Interface bus which interfaces with the on-chip Microprocessor Interface (MPI) bus. In addition, users can drive the SMI interface from routing if desired.

The user can configure the DLL for many common functions such as clock injection match and single delay cell. Lattice provides primitives in its design for time reference delay (DDR memory) and clock injection delay removal.

Figure 2-12. DLL Diagram



PLL/DLL Cascading

The LatticeSC devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are as follows:

- PLL to PLL
- PLL to DLL
- DLL to DLL
- DLL to PLL

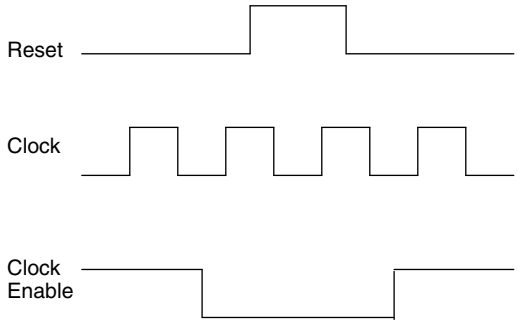
DLLs are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLL and PLLs.

When cascading the DLL to the PLL, the DLL can be used to drive the PLL to create fine phase shifts of an input clock signal. Figure 2-13 shows a shift of all outputs for CLKOP and CLKOS out in time.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset, as shown in Figure 2-16.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM, FIFO and shift register implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-16. The reset timing rules apply to the RPReset input vs. the RE input and the RST input vs. the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For the EBR shift register mode, the GSR signal is always enabled and the local RESET pin is always asynchronous.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled. For more information about on-chip memory, see TN1094, On-Chip Memory Usage Guide for LatticeSC Devices.

Programmable I/O Cells (PIC)

Each PIC contains four PIOs connected to their respective PURESPEED I/O Buffer which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to PURESPEED I/O buffer, and receives input (DI) from the buffer. The PIO contains advanced capabilities to allow the support of speeds up to 2Gbps. These include dedicated shift and DDR logic and adaptive input logic. The dedicated resources simplify the design of robust interfaces.

PURESPEED I/O Buffer Banks

LatticeSC devices have seven PURESPEED I/O buffer banks; each is capable of supporting multiple I/O standards. Each PURESPEED I/O bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-26 shows the seven banks and their associated supplies. Table 2-7 lists the maximum number of I/Os per bank for the whole LatticeSC family.

In the LatticeSC devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI33 and PCIX33) are powered using V_{CCIO}. In addition to the bank V_{CCIO} supplies, the LatticeSC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers. VCCAUX also powers a predriver of single-ended output buffers to enhance buffer performance.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeSC devices any I/O pin in a bank can be configured to be a dedicated reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Differential drivers have user selectable internal or external bias. External bias is brought in by the VREF1 pin in the bank. External bias for differential buffers is needed for applications that requires tighter than standard output common mode range.

Since a bank can have only one external bias circuit for differential drivers, LVDS and RSDS differential outputs can be mixed in a bank.

If a differential driver is configured in a bank, one pin in that bank becomes a DIFFR pin. This DIFFR pin must be connected to ground via an external 1K +/-1% ohm resistor. Note that differential drivers are not supported in banks 1, 4 and 5.

In addition, there are dedicated Terminating Supply (V_{TT}) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These V_{TT} pins are available in banks 2-7, these pins are not available in some packages. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.

There are further restrictions on the use of V_{TT} pins, for additional details refer to technical information at the end of this data sheet.

3. **Bottom Side (Banks 4 and 5)**
   These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but true HLVDS and RSDS differential drivers are not available. Adaptive input logic is available on PIOs A or C.

Table 2-8 lists the standards supported by each side.

Table 2-8. I/O Standards Supported by Different Banks

Description	Top Side Banks 1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
I/O Buffer Type	Single-ended, Differential Receiver	Single-ended, Differential Receiver and Driver	Single-ended, Differential Receiver	Single-ended, Differential Receiver and Driver
Output Standards Supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II SSTL33_ I, II HSTL15_I, II, III[1], IV[1] HSTL18_I, II,III[1], IV[1] SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL[2], GTL+[2]	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II HSTL15_I,III HSTL18_I,II,III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL[2], GTL+[2]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II SSTL33_ I, II HSTL15_I, II, III[1], IV[1] HSTL18_I, II,III[1], IV[1] SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL[2], GTL+[2]	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II HSTL15_I,III HSTL18_I,II,III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL[2], GTL+[2]
Input Standards Supported	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Clock Inputs	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Differential Output Support via Emulation	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL
AIL Support	No	Yes	Yes	Yes

1. Input only.
2. Input only. Outputs supported by bussing multiple outputs together.

Supported Standards

The LatticeSC PURESPEED I/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 12, 15, 18, 25 and 33 standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, termination resistance, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL, HSTL, GTL (input only), GTL+ (input only), PCI33, PCIX33, PCIX15, AGP-1X33 and AGP-2X33. Differential standards supported include LVDS, RSDS, BLVDS, MLVDS, LVPECL, differential SSTL and differential HSTL. Tables 12 and 13 show the I/O standards (together with their supply and reference voltages) supported by the LatticeSC devices. The tables also provide the available internal termination schemes. For further information on utilizing the PURESPEED I/O buffer to support a variety of standards please see details of additional technical documentation at the end of this data sheet.

PCI Specification, Revision 2.2 requires the use of clamping diodes for 3.3V operation. For more information on the PCI interface, please refer to the PCI Specification, Revision 2.2.

Programmable Slew Rate Control

All output and bidirectional buffers have an optional programmable output slew rate control that can be configured for either low noise or high-speed performance. Each I/O pin has an individual slew rate control. This allows designers to specify slew rate control on a pin-by-pin basis. This slew rate control affects both the rising and falling edges.

Programmable Termination

Many of the I/O standards supported by the LatticeSC devices require termination at the transmitter, receiver or both. The SC devices provide the capability to implement many kinds of termination on-chip, minimizing stub lengths and hence improving performance. Utilizing this feature also has the benefit of reducing the number of discrete components required on the circuit board. The termination schemes can be split into two categories single-ended and differential.

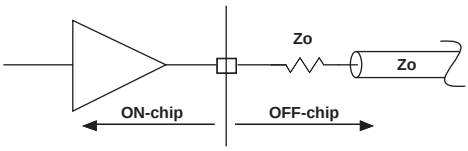
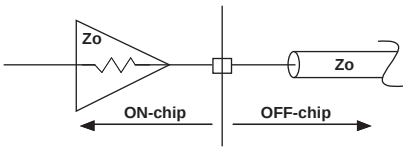
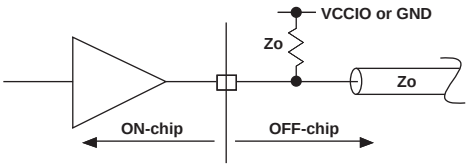
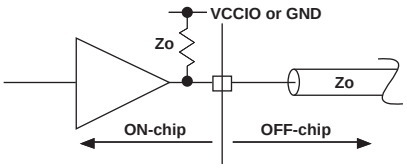
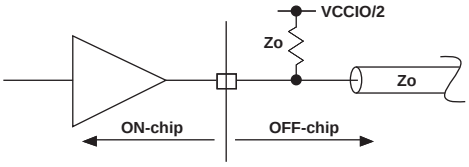
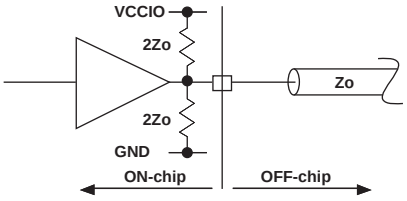
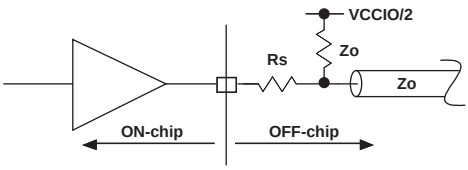
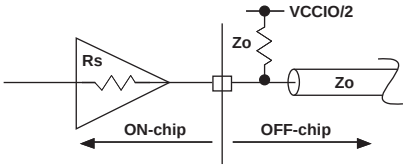
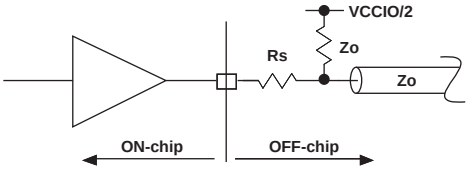
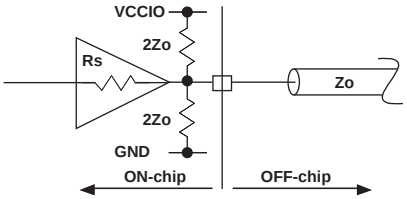
Single Ended Termination

Single Ended Outputs: The SC devices support a number of different terminations for single ended outputs:

- Series
- Parallel to V_{CCIO} or GND
- Parallel to $V_{CCIO}/2$
- Parallel to $V_{CCIO}/2$ combined with series

Figure 2-27 shows the single ended output schemes that are supported. The nominal values of the termination resistors are shown in Table 2-10.

Figure 2-27. Output Termination Schemes

Termination Type	Discrete Off-Chip Solution	Lattice On-Chip Solution
Series termination (controlled output impedance)		
Parallel termination to V_{CCIO}, or parallel driving end		
Parallel termination to $V_{CCIO}/2$ driving end		
Combined series + parallel termination to $V_{CCIO}/2$ at driving end (only series termination moved on-chip)		
Combined series + parallel to $V_{CCIO}/2$ driving end		

Initialization and Standby Supply Current

The table below indicates initialization and standby supply current while operating at 85°C junction temperature (T_J), which is the high end of the commercial temperature range, and 105°C, which is the high end of the industrial temperature range. This data assumes all outputs are tri-stated and all inputs are configured as LVCMOS and held at V_{CCIO} or GND. The remaining SERDES supply current for V_{DDIB} and V_{DDOB} is detailed in the SERDES section of this data sheet. For power at your design temperature, it is recommended to use the Power Calculator tool which is accessible in ispLEVER or can be used as a standalone tool. For more information on supply current, see the reference to additional technical documentation available at the end of this data sheet.

Over Recommended Operating Conditions

Symbol	Condition	Parameter	Device	25°C Typ.[1]	85°C Max.[2]		105°C Max.[2]	Units
				All	-5, -6	-7	-5, -6	
I_{CC}	(VCC = 1.2V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	65	449	678	755	mA
			LFSC/M25	113	798	1255	1343	mA
			LFSC/M40	159	1178	2006	1981	mA
			LFSC/M80	276	2122	3827	3569	mA
			LFSC/M115	454	3376	—	5679	mA
	(VCC = 1.0V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	45	312	471	524	mA
			LFSC/M25	79	554	872	933	mA
			LFSC/M40	110	818	1393	1375	mA
			LFSC/M80	191	1473	2658	2478	mA
			LFSC/M115	315	2344	—	3943	mA
I_{CC12}		1.2V Power Supply Current for Configuration Logic, FPGA PLL, SERDES PLL and SERDES Analog Supplies	LFSC/M15	23	39	59	35	mA
			LFSC/M25	25	50	78	56	mA
			LFSC/M40	31	78	133	89	mA
			LFSC/M80	50	108	195	123	mA
			LFSC/M115	65	131	—	154	mA
I_{CCAUX}		Auxiliary Operating Power Supply Current	LFSC/M15	7	12	19	14	mA
			LFSC/M25	9	16	25	18	mA
			LFSC/M40	12	23	39	25	mA
			LFSC/M80	13	25	45	23	mA
			LFSC/M115	16	27	—	26	mA
I_{CCIO} and I_{CCJ}		Bank Power Supply Current (per bank)	LFSC/M15	0.1	0.2	0.3	0.2	mA
			LFSC/M25	0.3	0.6	1.0	0.7	mA
			LFSC/M40	0.4	0.9	1.5	1.0	mA
			LFSC/M80	0.5	1.1	2.1	1.3	mA
			LFSC/M115	0.7	1.5	—	1.8	mA

1. I_{CC} is specified at T_J = 25°C and typical V_{CC}.
2. I_{CC} is specified at the respective commercial and industrial maximum T_J and V_{CC} limits.

PURESPEED I/O Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 33	3.135	3.3	3.465	—	—	—
LVCMOS 25	2.375	2.5	2.625	—	—	—
LVCMOS 18	1.71	1.8	1.89	—	—	—
LVCMOS 15	1.425	1.5	1.575	—	—	—
LVCMOS 12	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
PCIX33	3.135	3.3	3.465	—	—	—
PCIX15	1.425	1.5	1.575	$0.49V_{CCIO}$	$0.5V_{CCIO}$	$0.51V_{CCIO}$
AGP1X33	3.135	3.3	3.465	—	—	—
AGP2X33	3.135	3.3	3.465	$0.39V_{CCIO}$	$0.4V_{CCIO}$	$0.41V_{CCIO}$
SSTL18_I, II[3]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II[3]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II[3]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I, II[3]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15_III[1, 3] and IV[1, 3]	1.425	1.5	1.575	0.68	0.9	0.9
HSTL 18_I[3], II[3]	1.71	1.8	1.89	0.816	0.9	1.08
HSTL 18_ III[1, 3], IV[1, 3]	1.71	1.8	1.89	0.816	1.08	1.08
GTL12[1, 3], GTLPLUS15[1, 3]	—	—	—	0.882	1.0	1.122
LVDS	—	—	—	—	—	—
Mini-LVDS	—	—	—	—	—	—
RSDS	—	—	—	—	—	—
LVPECL33 (outputs)[2]	3.135	3.3	3.465	—	—	—
LVPECL33 (inputs)[2, 4]	—	≤ 2.5	—	—	—	—
BLVDS25[2, 3]	2.375	2.5	2.625	—	—	—
MLVDS25[2, 3]	2.375	2.5	2.625	—	—	—
SSTL18D_I[3], II[3]	1.71	1.8	1.89	—	—	—
SSTL25D_I[3], II[3]	2.375	2.5	2.625	—	—	—
SSTL33D_I[3], II[3]	3.135	3.3	3.465	—	—	—
HSTL15D_I[3], II[3]	1.425	1.5	1.575	—	—	—
HSTL18D_I[3], II[3]	1.71	1.8	1.89	—	—	—

1. Input only.
2. Inputs on chip. Outputs are implemented with the addition of external resisters.
3. Input for this standard does not depend on the value of V_{CCIO}.
4. Inputs for this standard cannot be in 3.3V VCCIO banks (≤ 2.5V only).

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AK14	PB25A	5		PB35A	5	
AK15	PB25B	5		PB35B	5	
AK16	PB27A	4		PB37A	4	
AK17	PB27B	4		PB37B	4	
AJ16	PB28A	4		PB38A	4	
AJ17	PB28B	4		PB38B	4	
AE16	PB28C	4		PB38C	4	
AH16	PB29A	4		PB39A	4	
AG16	PB29B	4		PB39B	4	
AK18	PB31A	4		PB41A	4	
AK19	PB31B	4		PB41B	4	
AH17	PB32A	4		PB42A	4	
AH18	PB32B	4		PB42B	4	
AG17	PB32D	4		PB42D	4	
AJ18	PB33A	4		PB43A	4	
AJ19	PB33B	4		PB43B	4	
AK20	PB35A	4	PCLKT4_2	PB46A	4	PCLKT4_2
AK21	PB35B	4	PCLKC4_2	PB46B	4	PCLKC4_2
AF18	PB36A	4	PCLKT4_1	PB47A	4	PCLKT4_1
AG18	PB36B	4	PCLKC4_1	PB47B	4	PCLKC4_1
AJ20	PB37A	4	PCLKT4_0	PB49A	4	PCLKT4_0
AJ21	PB37B	4	PCLKC4_0	PB49B	4	PCLKC4_0
AG19	PB37C	4	VREF2_4	PB49C	4	VREF2_4
AK22	PB39A	4	PCLKT4_5	PB51A	4	PCLKT4_5
AK23	PB39B	4	PCLKC4_5	PB51B	4	PCLKC4_5
AH19	PB39C	4		PB51C	4	
AK24	PB40A	4	PCLKT4_3	PB52A	4	PCLKT4_3
AK25	PB40B	4	PCLKC4_3	PB52B	4	PCLKC4_3
AE19	PB40C	4	PCLKT4_4	PB52C	4	PCLKT4_4
AE20	PB40D	4	PCLKC4_4	PB52D	4	PCLKC4_4
AE21	PB41A	4		PB53A	4	
AF21	PB41B	4		PB53B	4	
AG21	PB43A	4		PB55A	4	
AG22	PB43B	4		PB55B	4	
AH22	PB44A	4		PB56A	4	
AH23	PB44B	4		PB56B	4	
AH21	PB44C	4		PB56C	4	
AK28	PB45A	4		PB60A	4	
AK29	PB45B	4		PB60B	4	
AE22	PB45C	4		PB60C	4	
AJ28	PB47A	4		PB67A	4	
AH28	PB47B	4		PB67B	4	
AE24	PB47C	4	VREF1_4	PB67C	4	VREF1_4
AE25	PB47D	4		PB67D	4	
AJ29	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P17	VCC	-		VCC	-	
P19	VCC	-		VCC	-	
R13	VCC	-		VCC	-	
R15	VCC	-		VCC	-	
R18	VCC	-		VCC	-	
R20	VCC	-		VCC	-	
T13	VCC	-		VCC	-	
T14	VCC	-		VCC	-	
T16	VCC	-		VCC	-	
T17	VCC	-		VCC	-	
T19	VCC	-		VCC	-	
T20	VCC	-		VCC	-	
U13	VCC	-		VCC	-	
U14	VCC	-		VCC	-	
U16	VCC	-		VCC	-	
U17	VCC	-		VCC	-	
U19	VCC	-		VCC	-	
U20	VCC	-		VCC	-	
V13	VCC	-		VCC	-	
V15	VCC	-		VCC	-	
V18	VCC	-		VCC	-	
V20	VCC	-		VCC	-	
W14	VCC	-		VCC	-	
W16	VCC	-		VCC	-	
W17	VCC	-		VCC	-	
W19	VCC	-		VCC	-	
Y13	VCC	-		VCC	-	
Y15	VCC	-		VCC	-	
Y16	VCC	-		VCC	-	
Y17	VCC	-		VCC	-	
Y18	VCC	-		VCC	-	
Y20	VCC	-		VCC	-	
C17	VCCIO1	-		VCCIO1	-	
D16	VCCIO1	-		VCCIO1	-	
F15	VCCIO1	-		VCCIO1	-	
F24	VCCIO1	-		VCCIO1	-	
G18	VCCIO1	-		VCCIO1	-	
G9	VCCIO1	-		VCCIO1	-	
J11	VCCIO1	-		VCCIO1	-	
J19	VCCIO1	-		VCCIO1	-	
K14	VCCIO1	-		VCCIO1	-	
K22	VCCIO1	-		VCCIO1	-	
G4	VCCIO2	-		VCCIO2	-	
J7	VCCIO2	-		VCCIO2	-	
K3	VCCIO2	-		VCCIO2	-	
L10	VCCIO2	-		VCCIO2	-	
M6	VCCIO2	-		VCCIO2	-	
N4	VCCIO2	-		VCCIO2	-	
P9	VCCIO2	-		VCCIO2	-	
R7	VCCIO2	-		VCCIO2	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB57D	4		PB79D	4	
AN13	PB58A	4	PCLKT4_3	PB80A	4	PCLKT4_3
AN12	PB58B	4	PCLKC4_3	PB80B	4	PCLKC4_3
AD14	PB58C	4	PCLKT4_4	PB80C	4	PCLKT4_4
AD15	PB58D	4	PCLKC4_4	PB80D	4	PCLKC4_4
AP13	PB61A	4		PB73A	4	
AP12	PB61B	4		PB73B	4	
AK13	PB61C	4		PB73C	4	
AK12	PB61D	4		PB73D	4	
AP11	PB62A	4		PB83A	4	
AP10	PB62B	4		PB83B	4	
AN11	PB63A	4		PB99A	4	
AN10	PB63B	4		PB99B	4	
AF14	PB63C	4		PB99C	4	
AF13	PB63D	4		PB99D	4	
AM10	PB67A	4		PB101A	4	
AM9	PB67B	4		PB101B	4	
AE14	PB67C	4		PB101C	4	
AE13	PB67D	4		PB101D	4	
AP9	PB69A	4		PB104A	4	
AP8	PB69B	4		PB104B	4	
AK11	PB69C	4		PB104C	4	
AK10	PB69D	4		PB104D	4	
AL10	PB70A	4		PB107A	4	
AL9	PB70B	4		PB107B	4	
AF12	PB70C	4		PB107C	4	
AF11	PB70D	4		PB107D	4	
AN9	PB73A	4		PB109A	4	
AN8	PB73B	4		PB109B	4	
AG11	PB73C	4		PB109C	4	
AG10	PB73D	4		PB109D	4	
AP7	PB74A	4		PB111A	4	
AP6	PB74B	4		PB111B	4	
AG13	PB74C	4		PB111C	4	
AG12	PB74D	4		PB111D	4	
AN7	PB75A	4		PB113A	4	
AN6	PB75B	4		PB113B	4	
AK9	PB75C	4		PB113C	4	
AK8	PB75D	4		PB113D	4	
AP5	PB77A	4		PB115A	4	
AP4	PB77B	4		PB115B	4	
AD11	PB77C	4		PB115C	4	
AE11	PB77D	4		PB115D	4	
AM7	PB78A	4		PB117A	4	
AM6	PB78B	4		PB117B	4	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
R7	NC	-		PR39D	2	
P7	NC	-		PR39C	2	
N3	NC	-		PR39B	2	
M3	NC	-		PR39A	2	
H1	NC	-		PR26B	2	
G1	NC	-		PR26A	2	
L5	NC	-		PR25B	2	
K5	NC	-		PR25A	2	
G2	NC	-		PR24B	2	
F2	NC	-		PR24A	2	
F1	NC	-		PR22B	2	
E1	NC	-		PR22A	2	
A2	GND	-		GND	-	
A33	GND	-		GND	-	
AA15	GND	-		GND	-	
AA20	GND	-		GND	-	
AA32	GND	-		GND	-	
AA4	GND	-		GND	-	
AB28	GND	-		GND	-	
AB6	GND	-		GND	-	
AC11	GND	-		GND	-	
AC18	GND	-		GND	-	
AC25	GND	-		GND	-	
AD23	GND	-		GND	-	
AD3	GND	-		GND	-	
AD31	GND	-		GND	-	
AE12	GND	-		GND	-	
AE15	GND	-		GND	-	
AE29	GND	-		GND	-	
AE7	GND	-		GND	-	
AE9	GND	-		GND	-	
AF20	GND	-		GND	-	
AF26	GND	-		GND	-	
AG32	GND	-		GND	-	
AG4	GND	-		GND	-	
AH13	GND	-		GND	-	
AH19	GND	-		GND	-	
AH25	GND	-		GND	-	
AH7	GND	-		GND	-	
AJ10	GND	-		GND	-	
AJ16	GND	-		GND	-	
AJ22	GND	-		GND	-	
AJ28	GND	-		GND	-	
AK3	GND	-		GND	-	
AK31	GND	-		GND	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W7	GND	-		GND	-	
AA14	VCC	-		VCC	-	
AA16	VCC	-		VCC	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AB13	VCC	-		VCC	-	
AB22	VCC	-		VCC	-	
N13	VCC	-		VCC	-	
N22	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	
P17	VCC	-		VCC	-	
P18	VCC	-		VCC	-	
P19	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
R15	VCC	-		VCC	-	
R17	VCC	-		VCC	-	
R18	VCC	-		VCC	-	
R20	VCC	-		VCC	-	
T14	VCC	-		VCC	-	
T16	VCC	-		VCC	-	
T19	VCC	-		VCC	-	
T21	VCC	-		VCC	-	
U14	VCC	-		VCC	-	
U15	VCC	-		VCC	-	
U17	VCC	-		VCC	-	
U18	VCC	-		VCC	-	
U20	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V14	VCC	-		VCC	-	
V15	VCC	-		VCC	-	
V17	VCC	-		VCC	-	
V18	VCC	-		VCC	-	
V20	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W14	VCC	-		VCC	-	
W16	VCC	-		VCC	-	
W19	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y15	VCC	-		VCC	-	
Y17	VCC	-		VCC	-	
Y18	VCC	-		VCC	-	
Y20	VCC	-		VCC	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
L5	PR38B	2	
K5	PR38A	2	
G2	PR34B	2	
F2	PR34A	2	
F1	PR30B	2	
E1	PR30A	2	
A2	GND	-	
A33	GND	-	
AA15	GND	-	
AA20	GND	-	
AA32	GND	-	
AA4	GND	-	
AB28	GND	-	
AB6	GND	-	
AC11	GND	-	
AC18	GND	-	
AC25	GND	-	
AD23	GND	-	
AD3	GND	-	
AD31	GND	-	
AE12	GND	-	
AE15	GND	-	
AE29	GND	-	
AE7	GND	-	
AE9	GND	-	
AF20	GND	-	
AF26	GND	-	
AG32	GND	-	
AG4	GND	-	
AH13	GND	-	
AH19	GND	-	
AH25	GND	-	
AH7	GND	-	
AJ10	GND	-	
AJ16	GND	-	
AJ22	GND	-	
AJ28	GND	-	
AK3	GND	-	
AK31	GND	-	
AL11	GND	-	
AL17	GND	-	
AL21	GND	-	
AL27	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM27	GND	-		GND	-	
AM36	GND	-		GND	-	
AM7	GND	-		GND	-	
AP4	GND	-		GND	-	
AP40	GND	-		GND	-	
AR14	GND	-		GND	-	
AR20	GND	-		GND	-	
AR23	GND	-		GND	-	
AR29	GND	-		GND	-	
AR35	GND	-		GND	-	
AR8	GND	-		GND	-	
AT11	GND	-		GND	-	
AT17	GND	-		GND	-	
AT26	GND	-		GND	-	
AT32	GND	-		GND	-	
AU3	GND	-		GND	-	
AU39	GND	-		GND	-	
AW12	GND	-		GND	-	
AW18	GND	-		GND	-	
AW22	GND	-		GND	-	
AW28	GND	-		GND	-	
AW34	GND	-		GND	-	
AW6	GND	-		GND	-	
AY15	GND	-		GND	-	
AY21	GND	-		GND	-	
AY25	GND	-		GND	-	
AY31	GND	-		GND	-	
AY37	GND	-		GND	-	
AY9	GND	-		GND	-	
B1	GND	-		GND	-	
B42	GND	-		GND	-	
BA1	GND	-		GND	-	
BA42	GND	-		GND	-	
BB2	GND	-		GND	-	
BB41	GND	-		GND	-	
C10	GND	-		GND	-	
C12	GND	-		GND	-	
C13	GND	-		GND	-	
C16	GND	-		GND	-	
C18	GND	-		GND	-	
C19	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C27	GND	-		GND	-	
C28	GND	-		GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L8	VCCIO2	-		VCCIO2	-	
M3	VCCIO2	-		VCCIO2	-	
P7	VCCIO2	-		VCCIO2	-	
R4	VCCIO2	-		VCCIO2	-	
T12	VCCIO2	-		VCCIO2	-	
U8	VCCIO2	-		VCCIO2	-	
V3	VCCIO2	-		VCCIO2	-	
W11	VCCIO2	-		VCCIO2	-	
Y7	VCCIO2	-		VCCIO2	-	
AB3	VCCIO3	-		VCCIO3	-	
AC7	VCCIO3	-		VCCIO3	-	
AD11	VCCIO3	-		VCCIO3	-	
AE4	VCCIO3	-		VCCIO3	-	
AF8	VCCIO3	-		VCCIO3	-	
AG12	VCCIO3	-		VCCIO3	-	
AH3	VCCIO3	-		VCCIO3	-	
AJ7	VCCIO3	-		VCCIO3	-	
AK11	VCCIO3	-		VCCIO3	-	
AL4	VCCIO3	-		VCCIO3	-	
AM8	VCCIO3	-		VCCIO3	-	
AP3	VCCIO3	-		VCCIO3	-	
AR7	VCCIO3	-		VCCIO3	-	
AU4	VCCIO3	-		VCCIO3	-	
AL16	VCCIO4	-		VCCIO4	-	
AM13	VCCIO4	-		VCCIO4	-	
AM19	VCCIO4	-		VCCIO4	-	
AR11	VCCIO4	-		VCCIO4	-	
AR17	VCCIO4	-		VCCIO4	-	
AT14	VCCIO4	-		VCCIO4	-	
AT20	VCCIO4	-		VCCIO4	-	
AT8	VCCIO4	-		VCCIO4	-	
AW15	VCCIO4	-		VCCIO4	-	
AW21	VCCIO4	-		VCCIO4	-	
AW9	VCCIO4	-		VCCIO4	-	
AY12	VCCIO4	-		VCCIO4	-	
AY18	VCCIO4	-		VCCIO4	-	
AY6	VCCIO4	-		VCCIO4	-	
AL27	VCCIO5	-		VCCIO5	-	
AM24	VCCIO5	-		VCCIO5	-	
AM30	VCCIO5	-		VCCIO5	-	
AR26	VCCIO5	-		VCCIO5	-	
AR32	VCCIO5	-		VCCIO5	-	
AT23	VCCIO5	-		VCCIO5	-	
AT29	VCCIO5	-		VCCIO5	-	
AT35	VCCIO5	-		VCCIO5	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C[1]	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C[1]	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C[1]	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C[1]	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Industrial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-6FN256I	-6	Lead-Free fpBGA	256	IND	15.2
LFSC3GA15E-5FN256I	-5	Lead-Free fpBGA	256	IND	15.2
LFSC3GA15E-6FN900I	-6	Lead-Free fpBGA	900	IND	15.2
LFSC3GA15E-5FN900I	-5	Lead-Free fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-6FN256I	-6	Lead-Free fpBGA	256	IND	15.2
LFSCM3GA15EP1-5FN256I	-5	Lead-Free fpBGA	256	IND	15.2
LFSCM3GA15EP1-6FN900I	-6	Lead-Free fpBGA	900	IND	15.2
LFSCM3GA15EP1-5FN900I	-5	Lead-Free fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-6FN900I	-6	Lead-Free fpBGA	900	IND	25.4
LFSC3GA25E-5FN900I	-5	Lead-Free fpBGA	900	IND	25.4
LFSC3GA25E-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	25.4
LFSC3GA25E-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	25.4
LFSC3GA25E-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4
LFSC3GA25E-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-6FN900I	-6	Lead-Free fpBGA	900	IND	25.4
LFSCM3GA25EP1-5FN900I	-5	Lead-Free fpBGA	900	IND	25.4
LFSCM3GA25EP1-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4
LFSCM3GA25EP1-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSC3GA40E-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSC3GA40E-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-6FCN1152I[2]	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-5FCN1152I[2]	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSC3GA40E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Date	Version	Section	Change Summary
June 2006 (cont.)	01.2 (cont.)	DC and Switching Characteristics (cont.)	Updated Typical Building Block Performance with ispLEVER 6.0 values.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.0 values.
			Updated Lattice SC Internal Timing Parameters with ispLEVER 6.0 values.
			Updated Lattice SC Family Timing Adders with ispLEVER 6.0 values
			Changed % spread from 1 to 0.5 min and from 3 to 1.5 max.
			Changed conditions to refer to “with multiplication” and “without multiplication”.
			Changed the formula for t_{OPJIT} with multiplication (same result, different representation).
		Pinout Information	Expanded definition of NC.
			Expanded definition of GND.
			Expanded definition of VTT_x.
			Expanded definition of VCC12.
			Added accuracy of TEMP pin.
			Added RESPN_[ULC/URC].
			Updated Pin Information Summary with additional devices and packages.
			Added additional devices and packages pinouts.
			Removed Power Supply and NC connections table
			Removed VTT table
			Removed LFSC25 Logic Signal Connections: 900-Ball ffBGA1 table
			Changed all VDDP, VDDTX and VDDRX to VCC12.
		Ordering Information	Added dual marking.
			Added lead free packaging information to part number description.
August 2006	01.3	Introduction	Added SC40 1152 information to Table 1-1.
			Updated Table 1-3 with ispLEVER 6.0 SP1 results.
		Architecture	Added SSTL18 II to Table 2-8.
			Changed Table 2-10 VCCIO column to “N/A” for LVDS, mini-LVDS, BLVDS25, MLVDS25, HYPT and RSDS.
			Changed Hypertransport performance to 700 MHz (1400 Mbps) in Table 2-11.
			Changed SPI4.2 performance to 500 MHz (1000 Mbps) in Table 2-11
			Added “On packages that include PROBE_GND, the most accurate measurements will occur between the TEMP pin and the PROBE_GND pin. On packages that do not include PROBE_GND, measurements should be made between the TEMP pin and board ground.”
			Added VCCIO of 2.5 V for LVPECL33 in table 2-9.
		DC and Switching Characteristics	Updated Typical Building Block Performance with ispLEVER 6.0 SP1 results.
			Updated Initialization and Standby Supply Current table to break out ICC and ICC12.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.0 SP1 results.
			Updated LatticeSC Internal Timing Parameters with ispLEVER 6.0 SP1 results.

Date	Version	Section	Change Summary
March 2007 (cont.)	01.5 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Internal Timing Parameters with ispLEVER 6.1 SP1 results.
			Updated t_{FDEL} and t_{CDEL} specifications.
			Updated LatticeSC Family Timing Adders with ispLEVER 6.1 SP1 results.
			Updated PLL specifications to expand frequency range down to 2 MHz and break out jitter for the different ranges.
			Added footnote to sysCLOCK PLL Timing table specifying the conditions for the jitter measurements.
			Added t_{DLL} specification to sysCLOCK DLL Timing table.
			Added footnote to sysCLOCK DLL Timing table specifying the conditions for the jitter measurements.
			Added sysCONFIG Master Parallel Configuration Mode and sysCONFIG SPI Port to LatticeSC sysCONFIG Port Timing table.
		Pin Information	Updated Pin Information Summary with SC40 information.
			Updated LFSC25 Logic Signal Connections: FF1020 with SC40 information.
			Updated LFSC80 Logic Signal Connections: FC1152 with SC40 information.
August 2007	01.6	General	Changed references of "HDC" to "HDC/SI".
			Changed references of "LDCN" to "LDCN/SCS".
			Changed references of "BUSYN/RCLK" to "BUSYN/RCLK/SCK".
			Changed references of "RDCFGN" to "TSALLN".
			Changed references of "TDO/RDDATA" to "TDO".
		Architecture	Updated text in Ripple Mode section.
			Added information to Global Set/Reset.
			Added information for Spread Spectrum Clocking
			Modified information for PLL/DLL Cascading. DLL to PLL is now supported.
			Modified AIL Block text and figure.
			Modified Figure 2-20 DDR/Shift Register Block.
			Added Information to Hot Socketing.
			Added new information for I/O Architecture Rules.
			Added information to SERDES Power Supply Sequencing Requirements.
		DC and Switching Characteristics	Added footnote to Hot Socketing Specifications table.
			Modified Initialization and Standby Supply Current table.
			Modified GSR Timing table.
			Modified sysCLOCK DLL Timing table to include $I_{DUTY.}$
			Deleted Readback Timing information from sysCONFIG Port Timing table.
			Modified data in External Switching Characteristics table.
		Pin Information	Added information to the Signal Descriptions table for HDC/SI, LDCN/SCS.
			Added footnote to Signal Descriptions table.
			Modified Description for signal BUSYN/RCLK/SCK.
			Modified data in Pin Information Summary and device-specific Pinout Information tables.