*Table 1-1. LatticeSC Family Selection Guide[1]*

| Device | SC15 | SC25 | SC40 | SC80 | SC115 |
|---|---|---|---|---|---|
| LUT4s (K) | 15 | 25 | 40 | 80 | 115 |
| sysMEM Blocks (18Kb) | 56 | 104 | 216 | 308 | 424 |
| Embedded Memory (Mbits) | 1.03 | 1.92 | 3.98 | 5.68 | 7.8 |
| Max. Distributed Memory (Mbits) | 0.24 | 0.41 | 0.65 | 1.28 | 1.84 |
| Number of 3.8Gbps SERDES (Max.) | 8 | 16 | 16 | 32 | 32 |
| DLLs | 12 | 12 | 12 | 12 | 12 |
| Analog PLLs | 8 | 8 | 8 | 8 | 8 |
| MACO Blocks | 4 | 6 | 10 | 10 | 12 |
| **Package I/O/SERDES Combinations (1mm ball pitch)** | | | | | |
| 256-ball fpBGA (17 x 17mm) | 139/4 | | | | |
| 900-ball fpBGA (31 x 31mm) | 300/8 | 378/8 | | | |
| 1020-ball fcBGA (33 x 33mm)[2] | | 476/16 | 562/16 | | |
| 1152-ball fcBGA (35 x 35mm)[3] | | | 604/16 | 660/16 | 660/16 |
| 1704-ball fcBGA (42.5 x 42.5mm)[3] | | | | 904/32 | 942/32 |

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per PCN #02A-10.
3. Ceramic fcBGA converted to organic fcBGA per PCN #01A-10.

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

*Table 1-2. LatticeSCM Family*

| Device | SCM15 | SCM25 | SCM40 | SCM80 | SCM115 |
|---|---|---|---|---|---|
| flexiMAC Blocks<br>• 1GbE Mode<br>• 10GbE Mode<br>• PCI Express Mode | 1 | 2 | 2 | 2 | 4 |
| SPI4.2 Blocks | 1 | 2 | 2 | 2 | 2 |
| Memory Controller Blocks<br>• DDR/DDR2 DRAM Mode<br>• QDR II/II+ SRAM Mode<br>• RLDRAM I<br>• RLDRAM II CIO/SIO | 1 | 2 | 2 | 2 | 2 |
| Low-Speed CDR Blocks | 0 | 0 | 2 | 2 | 2 |
| PCI Express LTSSM (PHY) Blocks | 1 | 0 | 2 | 2 | 2 |

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

## Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

### PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

***Table 2-4. PFU Modes of Operation***

| Logic | Ripple | RAM | ROM |
|---|---|---|---|
| LUT 4x8 or<br>MUX 2x1 x 8 | 2-bit Add x 4 | SPR 16x2 x 4<br>DPR 16x2 x 2 | ROM 16x1 x 8 |
| LUT 5x4 or<br>MUX 4x1 x 4 | 2-bit Sub x 4 | SPR 16x4 x 2<br>DPR 16x4 x 1 | ROM 16x2 x 4 |
| LUT 6x2 or<br>MUX 8x1 x 2 | 2-bit Counter x 4 | SPR 16x8 x 1 | ROM 16x4 x 2 |
| LUT 7x1 or<br>MUX 16x1 x 1 | 2-bit Comp x 4 | | ROM 16x8 x1 |

## Routing

There are many resources provided in the LatticeSC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

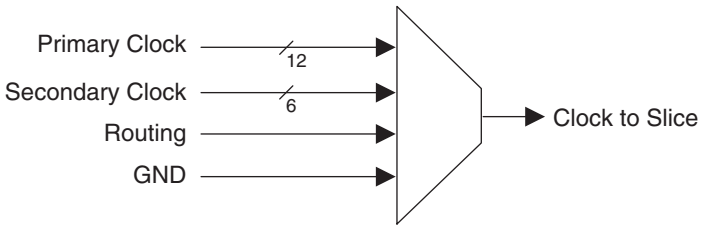
The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU) resources. The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. All connections are buffered to ensure high-speed operation even with long high-fanout connections.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## sysCLOCK Network

The LatticeSC devices have three distinct clock networks for use in distributing high-performance clocks within the device: primary clocks, secondary clocks and edge clocks. In addition to these dedicated clock networks, users are free to route clocks within the device using the general purpose routing. Figure 2-4 shows the clock resources available to each slice.

***Figure 2-4. Slice Clock Selection***




Note: GND is available to switch off the network.

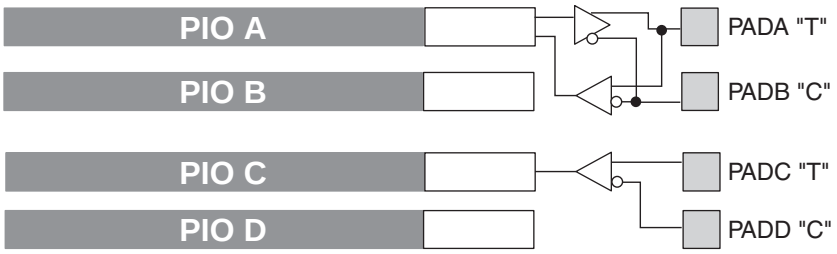
### Primary Clock Sources

LatticeSC devices have a wide variety of primary clock sources available. Primary clocks sources consists of the following:

- Primary clock input pins
- Edge clock input pins
- Two outputs per DLL

high-speed interfaces in the LatticeSC devices. Figure 2-18 shows how differential receivers and drivers are arranged between PIOs.

***Figure 2-18. Differential Drivers and Receivers***




*Differential Driver only available on right and left of the device.

## PIO

The PIO contains five blocks: an input register block, output register block, tristate register block, update block, and a control logic block. These blocks contain registers for both single data rate (SDR), double data rate (DDR), and shift register operation along with the necessary clock and selection logic.

## Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 show the diagram of the input register block. The signal from the PURE-SPEED I/O buffer (DI) enters the input register block and can be used for three purposes, as a source for the combinatorial (INDD) and clock outputs (INCK), the input into the SDR register/latch block and the input to the delay block. The output of the delay block can be used as combinatorial (INDD) and clock (INCK) outputs, an input to the DDR/Shift Register Block or an input into the SDR register block.

### Input SDR Register/Latch Block

The SDR register/latch block has a latch and a register/latch that can be used in a variety of combinations to provide a registered or latched output (INFF). The latch operates off high-speed input clocks and latches data on the positive going edge. The register/latch operates off the low-speed input clock and registers/latches data on the positive going edge. Both the latch and the register/latch have a clock enable input that is driven by the input clock enable. In addition both have a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register and latch LSR inputs are driven from LSRI, which is generated from the PIO control MUX. The GSR inputs are driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

### Input Delay Block

The delay block uses 144 tapped delay lines to obtain coarse and fine delay resolution. These delays can be adjusted during configuration or automatically via DLL or AIL blocks. The Adaptive Input Logic (AIL) uses this delay block to adjust automatically the delay in the data path to ensure that it has sufficient setup and hold time.

The delay line in this block matches the delay line that is used in the 12 on-chip DLLs. The delay line can be set via configuration bits or driven from a calibration bus that allows the setting to be controlled either from one of the on-chip DLLs or user logic. Controlling the delay from one of the on-chip DLLs allow the delay to be calibrated to the DLL clock and hence compensated for the variations in process, voltage and temperature.

## BLVDS

The LatticeSC devices support BLVDS standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

***Figure 3-2. BLVDS Multi-point Output Example***

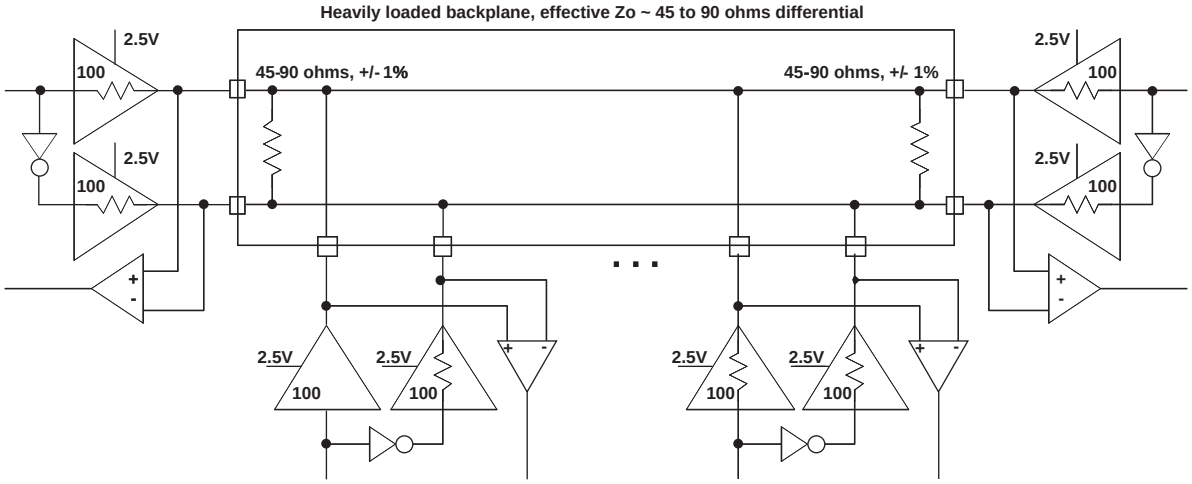



***Table 3-2. BLVDS DC Conditions[1]***

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | | Units |
|---|---|---|---|---|
| | | Zo = 45 | Zo = 90 | |
| $Z_{OUT}$ | Output impedance | 100 | 100 | ohm |
| $R_{TLEFT}$ | Left end termination | 45 | 90 | ohm |
| $R_{TRIGHT}$ | Right end termination | 45 | 90 | ohm |
| $V_{OH}$ | Output high voltage | 1.375 | 1.48 | V |
| $V_{OL}$ | Output low voltage | 1.125 | 1.02 | V |
| $V_{OD}$ | Output differential voltage | 0.25 | 0.46 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC output current | 11.2 | 10.2 | mA |

1. For input buffer, see LVDS table.

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AL23 | PB56D | 5 | | PB58D | 5 | |
| AW24 | PB57A | 5 | | PB61A | 5 | |
| AW23 | PB57B | 5 | | PB61B | 5 | |
| AN23 | PB57C | 5 | | PB61C | 5 | |
| AP23 | PB57D | 5 | | PB61D | 5 | |
| AY23 | PB59A | 5 | | PB63A | 5 | |
| AY24 | PB59B | 5 | | PB63B | 5 | |
| AU23 | PB59C | 5 | | PB63C | 5 | |
| AU22 | PB59D | 5 | | PB63D | 5 | |
| AV23 | PB60A | 5 | | PB66A | 5 | |
| AV22 | PB60B | 5 | | PB66B | 5 | |
| AM22 | PB60C | 5 | | PB66C | 5 | |
| AL22 | PB60D | 5 | | PB66D | 5 | |
| BA23 | PB61A | 5 | | PB69A | 5 | |
| BA22 | PB61B | 5 | | PB69B | 5 | |
| AN22 | PB61C | 5 | | PB69C | 5 | |
| AP22 | PB61D | 5 | | PB69D | 5 | |
| BB23 | PB63A | 5 | | PB71A | 5 | |
| BB22 | PB63B | 5 | | PB71B | 5 | |
| AT22 | PB63C | 5 | | PB71C | 5 | |
| AR22 | PB63D | 5 | | PB71D | 5 | |
| BB21 | PB65A | 4 | | PB73A | 4 | |
| BB20 | PB65B | 4 | | PB73B | 4 | |
| AR21 | PB65C | 4 | | PB73C | 4 | |
| AT21 | PB65D | 4 | | PB73D | 4 | |
| BA21 | PB66A | 4 | | PB75A | 4 | |
| BA20 | PB66B | 4 | | PB75B | 4 | |
| AP21 | PB66C | 4 | | PB75C | 4 | |
| AN21 | PB66D | 4 | | PB75D | 4 | |
| AV21 | PB67A | 4 | | PB78A | 4 | |
| AV20 | PB67B | 4 | | PB78B | 4 | |
| AM21 | PB67C | 4 | | PB78C | 4 | |
| AL21 | PB67D | 4 | | PB78D | 4 | |
| AY20 | PB69A | 4 | | PB81A | 4 | |
| AY19 | PB69B | 4 | | PB81B | 4 | |
| AU21 | PB69C | 4 | | PB81C | 4 | |
| AU20 | PB69D | 4 | | PB81D | 4 | |
| AW20 | PB70A | 4 | | PB83A | 4 | |
| AW19 | PB70B | 4 | | PB83B | 4 | |
| AP20 | PB70C | 4 | | PB83C | 4 | |
| AN20 | PB70D | 4 | | PB83D | 4 | |
| BB19 | PB71A | 4 | | PB86A | 4 | |
| BB18 | PB71B | 4 | | PB86B | 4 | |
| AM20 | PB71C | 4 | | PB86C | 4 | |
| AL20 | PB71D | 4 | | PB86D | 4 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AP1 | PR90B | 3 | | PR109B | 3 | |
| AN1 | PR90A | 3 | | PR109A | 3 | |
| AK10 | PR89D | 3 | VREF2_3 | PR107D | 3 | VREF2_3 |
| AJ10 | PR89C | 3 | | PR107C | 3 | |
| AM5 | PR89B | 3 | | PR107B | 3 | |
| AL5 | PR89A | 3 | | PR107A | 3 | |
| AL7 | PR86D | 3 | | PR104D | 3 | |
| AK7 | PR86C | 3 | | PR104C | 3 | |
| AM1 | PR86B | 3 | | PR104B | 3 | |
| AL1 | PR86A | 3 | | PR104A | 3 | |
| AJ11 | PR85D | 3 | | PR103D | 3 | |
| AH11 | PR85C | 3 | | PR103C | 3 | |
| AK5 | PR85B | 3 | | PR103B | 3 | |
| AJ5 | PR85A | 3 | | PR103A | 3 | |
| AK9 | PR84D | 3 | | PR99D | 3 | |
| AJ9 | PR84C | 3 | | PR99C | 3 | |
| AK3 | PR84B | 3 | | PR99B | 3 | |
| AJ3 | PR84A | 3 | | PR99A | 3 | |
| AK6 | PR82D | 3 | | PR98D | 3 | |
| AJ6 | PR82C | 3 | | PR98C | 3 | |
| AK2 | PR82B | 3 | | PR98B | 3 | |
| AJ2 | PR82A | 3 | | PR98A | 3 | |
| AH10 | PR81D | 3 | | PR96D | 3 | |
| AG10 | PR81C | 3 | | PR96C | 3 | |
| AK1 | PR81B | 3 | | PR96B | 3 | |
| AJ1 | PR81A | 3 | | PR96A | 3 | |
| AH9 | PR80D | 3 | | PR94D | 3 | |
| AG9 | PR80C | 3 | | PR94C | 3 | |
| AH2 | PR80B | 3 | | PR94B | 3 | |
| AG2 | PR80A | 3 | | PR94A | 3 | |
| AH8 | PR78D | 3 | | PR92D | 3 | |
| AG8 | PR78C | 3 | | PR92C | 3 | |
| AG1 | PR78B | 3 | | PR92B | 3 | |
| AH1 | PR78A | 3 | | PR92A | 3 | |
| AG14 | PR77D | 3 | | PR91D | 3 | |
| AF14 | PR77C | 3 | | PR91C | 3 | |
| AG4 | PR77B | 3 | | PR91B | 3 | |
| AF4 | PR77A | 3 | | PR91A | 3 | |
| AH7 | PR76D | 3 | DIFFR_3 | PR90D | 3 | DIFFR_3 |
| AG7 | PR76C | 3 | | PR90C | 3 | |
| AG3 | PR76B | 3 | | PR90B | 3 | |
| AF3 | PR76A | 3 | | PR90A | 3 | |
| AH6 | PR74D | 3 | | PR88D | 3 | |
| AG6 | PR74C | 3 | | PR88C | 3 | |
| AF1 | PR74B | 3 | | PR88B | 3 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| H18 | PT77C | 1 | LDCN/SCS | PT93C | 1 | LDCN/SCS |
| F18 | PT77B | 1 | D8/MPI_DATA8 | PT93B | 1 | D8/MPI_DATA8 |
| E18 | PT77A | 1 | CS1/MPI_CS1 | PT93A | 1 | CS1/MPI_CS1 |
| H19 | PT75D | 1 | D9/MPI_DATA9 | PT90D | 1 | D9/MPI_DATA9 |
| G19 | PT75C | 1 | D10/MPI_DATA10 | PT90C | 1 | D10/MPI_DATA10 |
| D19 | PT75B | 1 | CS0N/MPI_CS0N | PT90B | 1 | CS0N/MPI_CS0N |
| D18 | PT75A | 1 | RDN/MPI_STRB_N | PT90A | 1 | RDN/MPI_STRB_N |
| J20 | PT74D | 1 | WRN/MPI_WR_N | PT89D | 1 | WRN/MPI_WR_N |
| K20 | PT74C | 1 | D7/MPI_DATA7 | PT89C | 1 | D7/MPI_DATA7 |
| E19 | PT74B | 1 | D6/MPI_DATA6 | PT89B | 1 | D6/MPI_DATA6 |
| F19 | PT74A | 1 | D5/MPI_DATA5 | PT89A | 1 | D5/MPI_DATA5 |
| K18 | PT73D | 1 | D4/MPI_DATA4 | PT87D | 1 | D4/MPI_DATA4 |
| J18 | PT73C | 1 | D3/MPI_DATA3 | PT87C | 1 | D3/MPI_DATA3 |
| A19 | PT73B | 1 | D2/MPI_DATA2 | PT87B | 1 | D2/MPI_DATA2 |
| B19 | PT73A | 1 | D1/MPI_DATA1 | PT87A | 1 | D1/MPI_DATA1 |
| H17 | PT71D | 1 | D16/PCLKC1_3/MPI_DATA16 | PT86D | 1 | D16/PCLKC1_3/MPI_DATA16 |
| J17 | PT71C | 1 | D17/PCLKT1_3/MPI_DATA17 | PT86C | 1 | D17/PCLKT1_3/MPI_DATA17 |
| B20 | PT71B | 1 | D0/MPI_DATA0 | PT86B | 1 | D0/MPI_DATA0 |
| C20 | PT71A | 1 | QOUT/CEON | PT86A | 1 | QOUT/CEON |
| M20 | PT70D | 1 | VREF2_1 | PT83D | 1 | VREF2_1 |
| L20 | PT70C | 1 | D18/MPI_DATA18 | PT83C | 1 | D18/MPI_DATA18 |
| F20 | PT70B | 1 | DOUT | PT83B | 1 | DOUT |
| G20 | PT70A | 1 | MCA_DONE_IN | PT83A | 1 | MCA_DONE_IN |
| K19 | PT69D | 1 | D19/PCLKC1_2/MPI_DATA19 | PT81D | 1 | D19/PCLKC1_2/MPI_DATA19 |
| J19 | PT69C | 1 | D20/PCLKT1_2/MPI_DATA20 | PT81C | 1 | D20/PCLKT1_2/MPI_DATA20 |
| D20 | PT69B | 1 | MCA_CLK_P1_OUT | PT81B | 1 | MCA_CLK_P1_OUT |
| E20 | PT69A | 1 | MCA_CLK_P1_IN | PT81A | 1 | MCA_CLK_P1_IN |
| H21 | PT67D | 1 | D21/PCLKC1_1/MPI_DATA21 | PT78D | 1 | D21/PCLKC1_1/MPI_DATA21 |
| G21 | PT67C | 1 | D22/PCLKT1_1/MPI_DATA22 | PT78C | 1 | D22/PCLKT1_1/MPI_DATA22 |
| B21 | PT67B | 1 | MCA_CLK_P2_OUT | PT78B | 1 | MCA_CLK_P2_OUT |
| C21 | PT67A | 1 | MCA_CLK_P2_IN | PT78A | 1 | MCA_CLK_P2_IN |
| M21 | PT66D | 1 | MCA_DONE_OUT | PT75D | 1 | MCA_DONE_OUT |
| L21 | PT66C | 1 | BUSYN/RCLK/SCK | PT75C | 1 | BUSYN/RCLK/SCK |
| A21 | PT66B | 1 | DP0/MPI_PAR0 | PT75B | 1 | DP0/MPI_PAR0 |
| A20 | PT66A | 1 | MPI_TA | PT75A | 1 | MPI_TA |
| J21 | PT65D | 1 | D23/MPI_DATA23 | PT73D | 1 | D23/MPI_DATA23 |
| K21 | PT65C | 1 | DP2/MPI_PAR2 | PT73C | 1 | DP2/MPI_PAR2 |
| E21 | PT65B | 1 | PCLKC1_0 | PT73B | 1 | PCLKC1_0 |
| F21 | PT65A | 1 | PCLKT1_0/MPI_CLK | PT73A | 1 | PCLKT1_0/MPI_CLK |
| G22 | PT63D | 1 | DP3/PCLKC1_4/MPI_PAR3 | PT71D | 1 | DP3/PCLKC1_4/MPI_PAR3 |
| H22 | PT63C | 1 | D24/PCLKT1_4/MPI_DATA24 | PT71C | 1 | D24/PCLKT1_4/MPI_DATA24 |
| A23 | PT63B | 1 | MPI_RETRY | PT71B | 1 | MPI_RETRY |
| A22 | PT63A | 1 | A0/MPI_ADDR14 | PT71A | 1 | A0/MPI_ADDR14 |
| L22 | PT61D | 1 | A1/MPI_ADDR15 | PT69D | 1 | A1/MPI_ADDR15 |
| M22 | PT61C | 1 | A2/MPI_ADDR16 | PT69C | 1 | A2/MPI_ADDR16 |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| L8 | VCCIO2 | - | | VCCIO2 | - | |
| M3 | VCCIO2 | - | | VCCIO2 | - | |
| P7 | VCCIO2 | - | | VCCIO2 | - | |
| R4 | VCCIO2 | - | | VCCIO2 | - | |
| T12 | VCCIO2 | - | | VCCIO2 | - | |
| U8 | VCCIO2 | - | | VCCIO2 | - | |
| V3 | VCCIO2 | - | | VCCIO2 | - | |
| W11 | VCCIO2 | - | | VCCIO2 | - | |
| Y7 | VCCIO2 | - | | VCCIO2 | - | |
| AB3 | VCCIO3 | - | | VCCIO3 | - | |
| AC7 | VCCIO3 | - | | VCCIO3 | - | |
| AD11 | VCCIO3 | - | | VCCIO3 | - | |
| AE4 | VCCIO3 | - | | VCCIO3 | - | |
| AF8 | VCCIO3 | - | | VCCIO3 | - | |
| AG12 | VCCIO3 | - | | VCCIO3 | - | |
| AH3 | VCCIO3 | - | | VCCIO3 | - | |
| AJ7 | VCCIO3 | - | | VCCIO3 | - | |
| AK11 | VCCIO3 | - | | VCCIO3 | - | |
| AL4 | VCCIO3 | - | | VCCIO3 | - | |
| AM8 | VCCIO3 | - | | VCCIO3 | - | |
| AP3 | VCCIO3 | - | | VCCIO3 | - | |
| AR7 | VCCIO3 | - | | VCCIO3 | - | |
| AU4 | VCCIO3 | - | | VCCIO3 | - | |
| AL16 | VCCIO4 | - | | VCCIO4 | - | |
| AM13 | VCCIO4 | - | | VCCIO4 | - | |
| AM19 | VCCIO4 | - | | VCCIO4 | - | |
| AR11 | VCCIO4 | - | | VCCIO4 | - | |
| AR17 | VCCIO4 | - | | VCCIO4 | - | |
| AT14 | VCCIO4 | - | | VCCIO4 | - | |
| AT20 | VCCIO4 | - | | VCCIO4 | - | |
| AT8 | VCCIO4 | - | | VCCIO4 | - | |
| AW15 | VCCIO4 | - | | VCCIO4 | - | |
| AW21 | VCCIO4 | - | | VCCIO4 | - | |
| AW9 | VCCIO4 | - | | VCCIO4 | - | |
| AY12 | VCCIO4 | - | | VCCIO4 | - | |
| AY18 | VCCIO4 | - | | VCCIO4 | - | |
| AY6 | VCCIO4 | - | | VCCIO4 | - | |
| AL27 | VCCIO5 | - | | VCCIO5 | - | |
| AM24 | VCCIO5 | - | | VCCIO5 | - | |
| AM30 | VCCIO5 | - | | VCCIO5 | - | |
| AR26 | VCCIO5 | - | | VCCIO5 | - | |
| AR32 | VCCIO5 | - | | VCCIO5 | - | |
| AT23 | VCCIO5 | - | | VCCIO5 | - | |
| AT29 | VCCIO5 | - | | VCCIO5 | - | |
| AT35 | VCCIO5 | - | | VCCIO5 | - | |

# Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

## For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1101 - Power Estimation and Management for LatticeSC Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

## Part Number Description

LF XXX XXX XX E PX – X XXXXXX X

**LF = Lattice FPGA**

**Device Family**
- LatticeSC FPGA
- LatticeSCM FPGA

**SERDES Speed**
- 3GA = 3.8G

**Logic Capacity**
- 15K LUTs
- 25K LUTs
- 40K LUTs
- 80K LUTs
- 115K LUTs

**Supply Voltage**
- E = 1.2V

**Grade**
- C = Commercial
- I = Industrial

**Package**[1]
- F256 = 256-ball fpBGA
- F900 = 900-ball fpBGA
- FF1020 = 1020-ball Organic fcBGA[2]
- FFA1020 = 1020-ball Organic fcBGA Revision 2
- FC1152 = 1152-ball Ceramic fcBGA[3]
- FF1152 = 1152-ball Organic fcBGA
- FC1704 = 1704-ball Ceramic fcBGA[3]
- FF1704 = 1704-ball Organic fcBGA

- FN256 = 256-ball Lead-Free fpBGA
- FN900 = 900-ball Lead-Free fpBGA
- FFN1020 = 1020-ball Lead-Free Organic fcBGA[2]
- FFAN1020 = 1020-ball Lead-Free Organic fcBGA Revision 2
- FCN1152 = 1152-ball Lead-Free Ceramic fcBGA[3]
- FFN1152 = 1152-ball Lead-Free Organic fcBGA
- FCN1704 = 1704-ball Lead-Free Ceramic fcBGA[3]
- FFN1704 = 1704-ball Lead-Free Organic fcBGA

**Speed Grade**
- -5 (Slowest)
- -6
- -7 (Fastest)[4]

**Predefined Function (LatticeSCM Only)**
- P1 = Initial MACO Option

1. fpBGA = 1.0 mm pitch BGA, fcBGA = 1.0 mm flip-chip BGA (organic and ceramic).
2. Converted to organic fcBGA per PCN #02A-10.
3. Converted to organic fcBGA per PCN #01A-10.
4. Not available in the LatticeSC115 and LatticeSCM115 devices.

## Ordering Information

Depending on the speed and temperature grade, the device can either be dual marked or single marked. The commercial grade is one speed grade faster than the associated dual marked industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

Lattice SC
LFSC3GA25E
6F900C-5I
XXXXXXXX

or

Lattice SC
LFSC3GA25E
7F900C
XXXXXXXX

| Temperature Grade | Speed Grade | Single or Dual Mark? |
|---|---|---|
| Commercial | -7 | Either OK |
| | -6 | Dual Only |
| | -5 | Single Only |
| Industrial | -6 | Either OK |
| | -5 | Dual Only |

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| Date | Version | Section | Change Summary |
|---|---|---|---|
| August 2006 (cont.) | 01.3 (cont.) | DC and Switching Characteristics (cont.) | Updated LatticeSC Family Timing Adders with ispLEVER 6.0 SP1 results |
| | | | Updated PLL Timing Parameters based on PDE testing results |
| | | | Removed RDDATA parameter from sysCONFIG readback timing table |
| | | Multiple | Changed TDO/RDDATA to TDO |
| | | Pinout Information | Removed all MPI signals from SC15 256 pin package Dual Function Column |
| | | | Added note to SC15, SC25 900 pin package that the package supports a 16 bit MPI |
| | | | Added note that pin D3 in an SC15 and SC25 900 pin package should not be used for single-ended outputs |
| | | | Added note that pin D28 in an SC15 and SC25 900 pin package should not be used for single-ended outputs |
| | | | Added note to SC25 1020 pin package that the package supports a 16 bit MPI |
| | | | Added note to SC80 1152 pin package that the package supports a 32 bit MPI |
| | | | Added note to SC80 1704 pin package that the package supports a 32 bit MPI |
| | | Ordering Information | Changed “fcBGA” for the 1020 packages to “ffBGA” |
| November 2006 | 01.4 | Introduction | LatticeSC Family Selection Guide table – I/O count for SC80 device, 1704 fcBGA package changed to 904/32. I/O count for SC115 device, 1704 fcBGA package changed to 942/32. |
| | | DC and Switching Characteristics | DC Electrical Characteristics table – Updated the initialization and standby supply current values. |
| | | | DC Electrical Characteristics table – Updated the sysCONFIG Master Parallel mode RCLK low and RCLK high time specifications. |
| | | | DC Electrical Characteristics table – Updated VCCIO values for LVPECL33 I/Os. |
| | | Pin Information | Pin Information Summary table - Changed number of single ended user I/Os from 906 to 904 for 1704 fcBGA. |
| | | | Removed the single-ended only output restriction on pins D3 and D28 in an SC15 and SC25 900 pin package. |
| | | Ordering Information | Ordering Information tables - Changed number of I/Os from 906 to 904 for 1704 fcBGA. |
| | | | Added ordering part numbers for LatticeSC/SCM 40K and 115K LUT devices. |
| | | | Added lead-free ordering part numbers. |
| | | Multiple | Changed number of available SC80 I/O from 906 to 904. |
| | | | Changed number of available SC115 I/O from 944 to 942. |
| January 2007 | 01.4a | Architecture | Added EBR Asynchronous Reset section. |
| February 2007 | 01.4b | Architecture | Updated EBR Asynchronous Reset section. |
| March 2007 | 01.5 | Architecture | Added EBR asynchronous reset clarification |
| | | | Clarified that differential drivers are not supported in banks 1, 4 and 5 |
| | | DC and Switching Characteristics | Added clarification for the description of the junction temperature specification in the Absolute Maximum Ratings section. |
| | | | Updated Initialization and Standby Current table. |
| | | | Updated LatticeSC External Switching Characteristics with ispLEVER 6.1 SP1 results. |