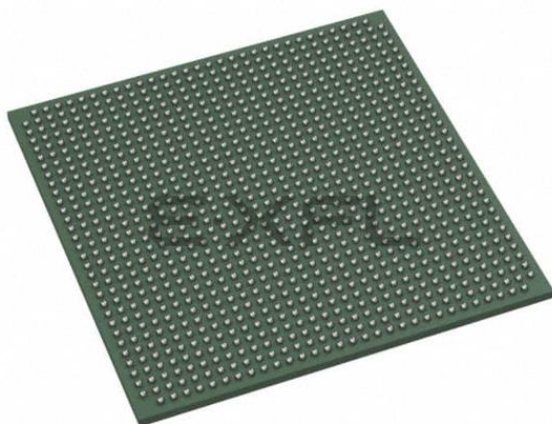




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

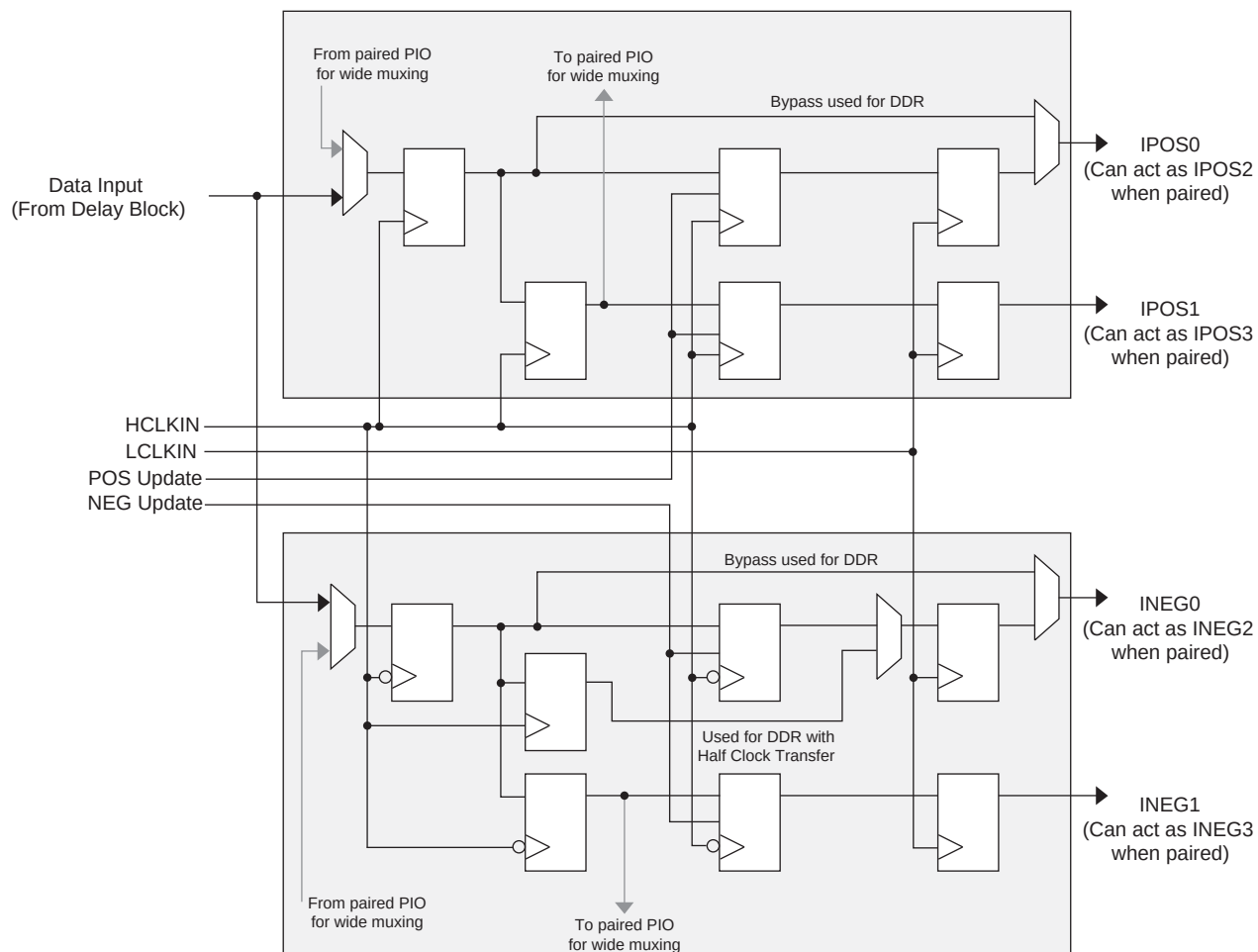
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	476
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga25e-5ff1020c

Figure 2-21. Input DDR/Shift Register Block

Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the PURESPEED I/O buffers. The block contains a register for SDR operation and a group of registers for DDR and shift register operation. The output signal (DO) can be derived directly from one of the inputs (bypass mode), the SDR register or the DDR/shift register block. Figure 2-22 shows the diagram of the Output Register Block.

Output SDR Register/Latch Block

The SDR register operates on the positive edge of the high-speed clock. It has clock enable that is driven by the clock enable output signal generated by the control MUX. In addition it has a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register LSR input is driven from LSRO, which is generated from the PIO control MUX. The GSR inputs is driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Output DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer from the low-speed clock domain. It functions as a gearbox allowing low-speed parallel data from the FPGA fabric be output as a higher speed serial stream. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. Figure 2-22 shows a simplified block diagram of the shift register block.

- 8-bit SERDES Only
- 10-bit SERDES Only
- SONET (STS-12/STS-48)
- Gigabit Ethernet
- Fibre Channel
- XAUI
- Serial RapidIO
- PCI-Express
- Generic 8b10b

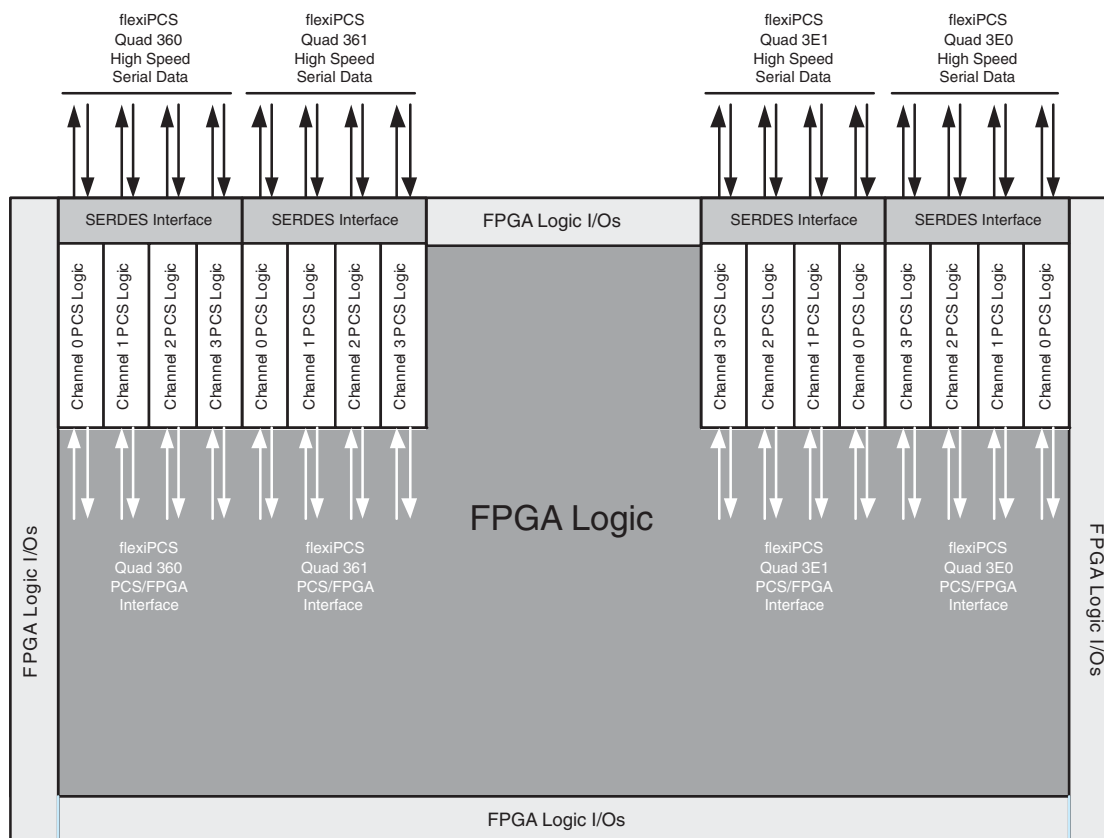
flexiPCS Quad

The flexiPCS logic is arranged in quads containing logic for four independent full-duplex data channels. Each device in the LatticeSC family has up to eight quads of flexiPCS logic. The LatticeSC Family Selection Guide table on the first page of this data sheet contains the number of flexiPCS channels present on the chip. Note that in some packages (particularly lower pin count packages), not all channels from all quads on a given device may be bonded to package pins.

Each quad supports up to four channels of full-duplex data and can be programmed into any one of several protocol based modes. Each quad requires its own reference clock which can be sourced externally or from the FPGA logic. The user can utilize between one and four channels in a quad, depending on the application.

Figure 2-30 shows an example of four flexiPCS quads in a LatticeSC device. Quads are labeled according to the address of their software controlled registers.

Figure 2-30. LatticeSC flexiPCS



Since each quad has its own reference clock, different quads can support different standards on the same chip. This feature makes the LatticeSC family of devices ideal for bridging between different standards.

Power Supply Ramp Rates

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
t_{RAMP}	Power supply ramp rates for all power supplies	Over process, voltage, temperature	3.45	—	—	mV/ μ s
			—	—	75	ms

1. See the Power-up and Power-Down requirements section for more details on power sequencing.
2. From 0.5V to minimum operating voltage.

Hot Socketing Specifications¹

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Programmable and dedicated Input or I/O leakage current ^{2, 3, 4, 5, 6}	$0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	—	—	± 1500	μ A
I_{HDIN}	SERDES average input current when device powered down and inputs driven ⁷		—	—	4	mA

1. See Hot Socket power up/down information in Chapter 2 of this document.
2. Assumes monotonic rise/fall rates for all power supplies.
3. Sensitive to power supply sequencing as described in hot socketing section.
4. Assumes power supplies are between 0 and maximum recommended operations conditions.
5. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .
6. Represents DC conditions. For the first 20ns after hot insertion, current specification is 8 mA.
7. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed VDDOB of 1.575V, 8b/10b data and internal AC coupling.

DC Electrical Characteristics⁵

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min. ³	Typ.	Max.	Units
$I_{\text{IL}}, I_{\text{IH}}^1$	Input or I/O Low leakage	$0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	—	—	10	μ A
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{\text{IN}} \leq 0.7 V_{\text{CCIO}}$	-30	—	-210	μ A
I_{PD}	I/O Active Pull-down Current	$V_{\text{IL}} (\text{MAX}) \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	30	—	210	μ A
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{\text{IN}} = V_{\text{IL}} (\text{MAX})$	30	—	—	μ A
I_{BHHS}	Bus Hold High Sustaining Current	$V_{\text{IN}} = 0.7 V_{\text{CCIO}}$	-30	—	—	μ A
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	—	—	210	μ A
I_{BHLH}	Bus Hold High Overdrive Current	$0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	—	—	-210	μ A
I_{CL}	PCI Low Clamp Current	$-3 < V_{\text{IN}} \leq -1$	$-25 + (V_{\text{IN}} + 1)/0.015$	—	—	mA
I_{CH}	PCI High Clamp Current	$V_{\text{CC}} + 4 > V_{\text{IN}} \geq V_{\text{CC}} + 1$	$25 + (V_{\text{IN}} - V_{\text{CC}} - 1)/0.015$	—	—	mA
V_{BHT}	Bus Hold trip Points	$0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	$V_{\text{IL}} (\text{MAX})$	—	$V_{\text{IH}} (\text{MIN})$	V
C1	I/O Capacitance ²	$V_{\text{CCIO}} = 3.3\text{V}, 2.5\text{V}, 1.8\text{V}, 1.5\text{V}, 1.2\text{V},$ $V_{\text{CC}} = 1.2\text{V}, V_{\text{CCIP2}} = 1.2\text{V},$ $V_{\text{CCAUX}} = 2.5, V_{\text{IO}} = 0 \text{ to } V_{\text{IH}} (\text{MAX})$	—	8	—	pf
C3 ²	Dedicated Input Capacitance ²	$V_{\text{CCIO}} = 3.3\text{V}, 2.5\text{V}, 1.8\text{V}, 1.5\text{V}, 1.2\text{V},$ $V_{\text{CC}} = 1.2\text{V}, V_{\text{CCIP2}} = 1.2\text{V},$ $V_{\text{CCAUX}} = 2.5, V_{\text{IO}} = 0 \text{ to } V_{\text{IH}} (\text{MAX})$	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_{\text{A}} = 25^{\circ}\text{C}$, $f = 1.0\text{MHz}$
3. I_{PU} , I_{PD} , I_{BHLS} and I_{BHHS} have minimum values of 15 or -15 μ A if V_{CCIO} is set to 1.2V nominal.
4. This table does not apply to SERDES pins.
5. For programmable I/Os.

PURESPEED I/O Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

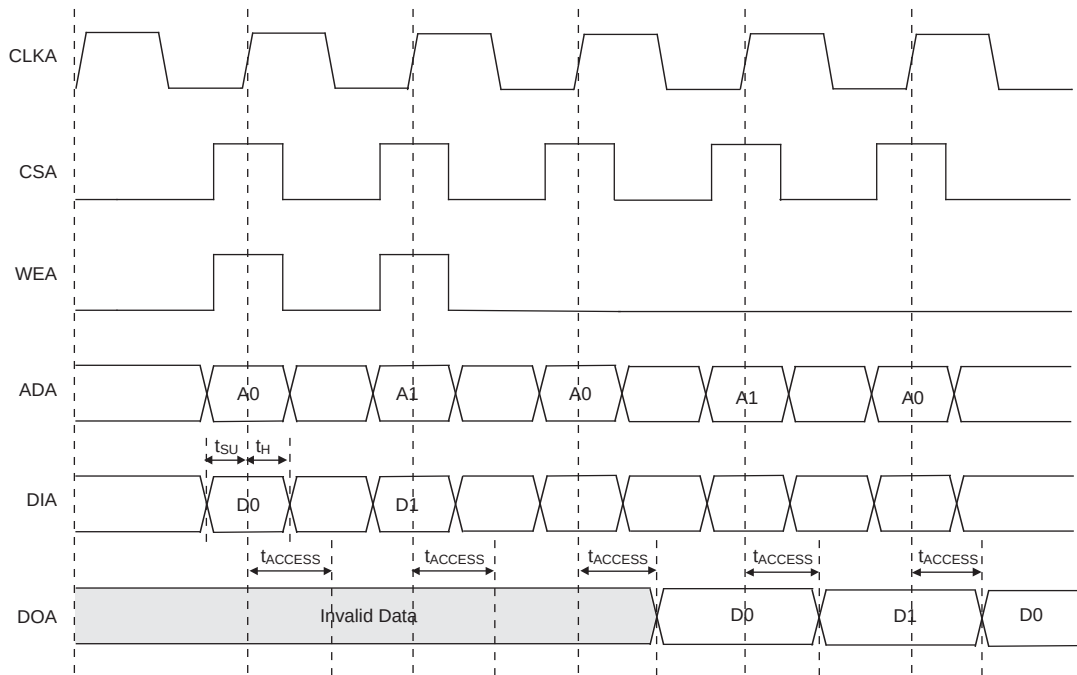
Input/Output Standard	V _{IL}		V _{IH}		V _{OL} Max. (V)	V _{OH} Min. (V)	I _{OL} (mA)	I _{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 33	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 25	-0.3	0.7	1.7	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 18	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 15	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 12	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.3	VCCIO - 0.3	12, 8, 4, 2	-12, -8, -4, -2
					0.2	VCCIO - 0.2	0.1	-0.1
PCIX15	-0.3	0.3VCCIO	0.5VCCIO	1.5	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCI33	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCIX33	-0.3	0.35VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
AGP-1X, AGP-2X	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
SSTL3_I	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.7	VCCIO - 1.1	8	-8
SSTS3_I OST ²	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 1.3	8	-8
SSTL3_II	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.5	VCCIO - 0.9	16	-16
SSTL3_II OST ²	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 0.13	16	-16
SSTL2_I	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.54	VCCIO - 0.62	7.6	-7.6
SSTL2_I OST ²	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	7.6	-7.6
SSTL2_II	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.35	VCCIO - 0.43	15.2	-15.2
SSTL2_II OST ²	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	15.2	-15.2
SSTL18_I	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
SSTL18_II	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
HSTL15_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	8	-8
HSTL15_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	16	-16
HSTL15_III ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL15_IV ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	9.6	-9.6
HSTL18_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	19.2	-19.2
HSTL18_III ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_IV ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
GTL12 ¹ , GTLPLUS15 ¹	-0.3	VREF - 0.2	VREF + 0.2	N/A	N/A	N/A	N/A	N/A

1. Input only.

2. Input with on-chip series termination.

EBR Memory Timing Diagrams

Figure 3-6. Read Mode



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-7. Read Mode with Input Registers Only

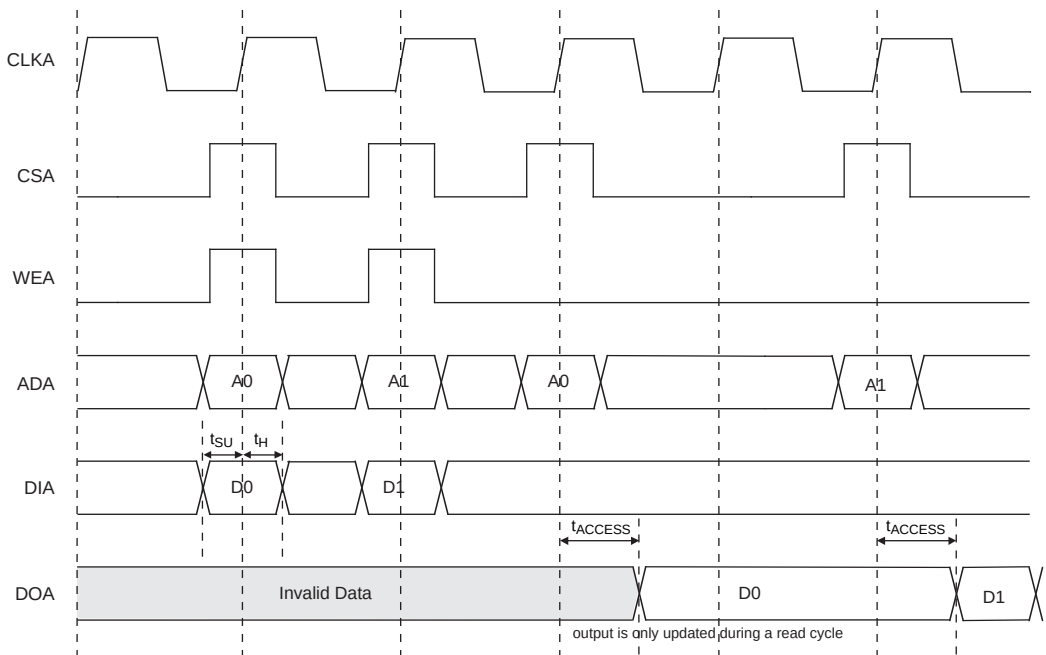


Figure 3-8. Read Mode with Input and Output Registers

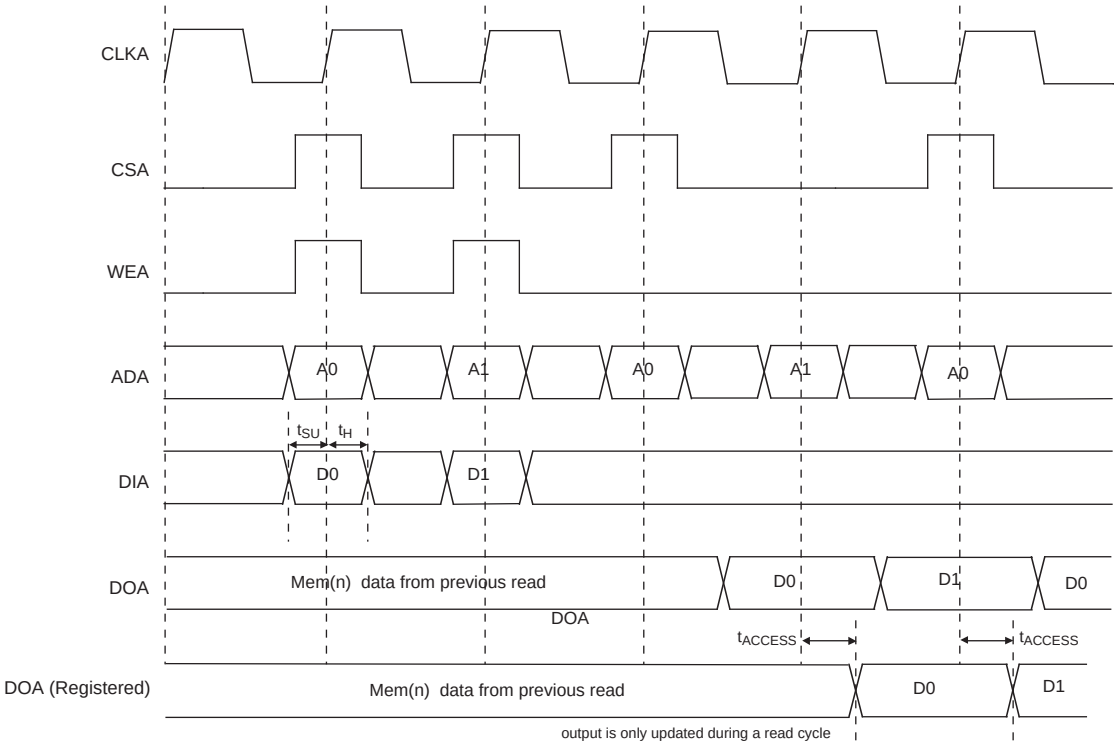
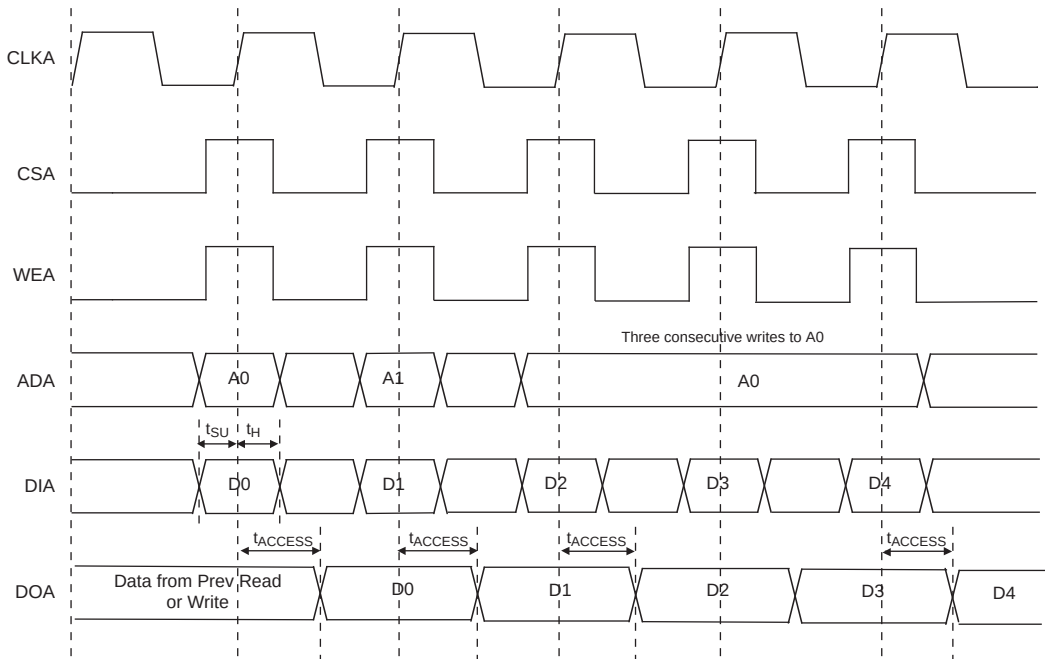


Figure 3-9. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

LatticeSC/M sysCONFIG Port Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
General Configuration Timing				
t_{SMODE}	M[3:0] Setup Time to INITN High	0	—	ns
t_{HMODE}	M[3:0] Hold Time from INITN High	600	—	ns
t_{RW}	RESETN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
t_{PGW}	PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
$f_{ESB_CLK_FRQ}$	System Bus ESB_CLK Frequency (No Wait States)	—	133	MHz
sysCONFIG Master Parallel Configuration Mode				
t_{SMB}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMB}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMB}	RCLK Low Time (Non-compressed Bitstreams)	0.5	0.5	CCLK periods
	RCLK Low Time (Compressed Bitstreams)	0.5	7.5	CCLK periods
t_{CHMB}	RCLK High Time	0.5	0.5	CCLK periods
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CSCK Low	—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low	0	2	μ s
t_{SCK}	CSCK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CSCK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN Low to CSCK high Setup Time	—	15	ns
f_{MAXSPI}	Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0)	—	50	MHz
t_{SUSPI}	SOSPI/D0 Data Setup Time Before CSCK	7	—	ns
t_{HSPI}	SOSPI/D0 Data Hold Time After CSCK	2	—	ns
	Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
	Duty Cycle	40	60	%
sysCONFIG Master Serial Configuration Mode				
t_{SMS}	DIN Setup Time	4.4	—	ns
t_{HMS}	DIN Hold Time	0	—	ns
f_{CMS}	CCLK Frequency (No Divider)	90	190	MHz
f_{C_DIV}	CCLK Frequency (Div 128)	0.70	1.48	MHz
t_D	CCLK to DOUT Delay	—	7.5	ns
sysCONFIG Master Parallel Configuration Mode				
t_{AVMP}	RCLK to Address Valid	—	10	ns
t_{SMP}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMP}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMP}	RCLK Low Time (Non-compressed Bitstream)	7.5	7.5	CCLK periods
	RCLK Low Time (Compressed Bitstream)	0.5	63.5	CCLK periods
t_{CHMP}	RCLK High Time	0.5	0.5	CCLK periods
t_{DMP}	CCLK to DOUT	—	7.5	ns

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB10	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
J10	VCC	-		VCC	-	
J21	VCC	-		VCC	-	
K10	VCC	-		VCC	-	
K11	VCC	-		VCC	-	
K12	VCC	-		VCC	-	
K13	VCC	-		VCC	-	
K14	VCC	-		VCC	-	
K17	VCC	-		VCC	-	
K18	VCC	-		VCC	-	
K19	VCC	-		VCC	-	
K20	VCC	-		VCC	-	
K21	VCC	-		VCC	-	
K22	VCC	-		VCC	-	
K9	VCC	-		VCC	-	
L10	VCC	-		VCC	-	
L21	VCC	-		VCC	-	
M10	VCC	-		VCC	-	
M21	VCC	-		VCC	-	
N10	VCC	-		VCC	-	
N21	VCC	-		VCC	-	
P10	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
U10	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V10	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W10	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y10	VCC	-		VCC	-	
Y21	VCC	-		VCC	-	
H11	VCCAUX	-		VCCAUX	-	
H12	VCCAUX	-		VCCAUX	-	
H19	VCCAUX	-		VCCAUX	-	
H20	VCCAUX	-		VCCAUX	-	
M23	VCCAUX	-		VCCAUX	-	
M24	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
N24	VCCAUX	-		VCCAUX	-	
U23	VCCAUX	-		VCCAUX	-	
U24	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	
V24	VCCAUX	-		VCCAUX	-	
W23	VCCAUX	-		VCCAUX	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG11	VCCIO5	-		VCCIO5	-	
AJ9	VCCIO5	-		VCCIO5	-	
AJ23	VCCIO4	-		VCCIO4	-	
AG20	VCCIO4	-		VCCIO4	-	
AJ26	VCCIO4	-		VCCIO4	-	
AG23	VCCIO4	-		VCCIO4	-	
AC29	VCCIO3	-		VCCIO3	-	
AA26	VCCIO3	-		VCCIO3	-	
Y28	VCCIO3	-		VCCIO3	-	
AA29	VCCIO3	-		VCCIO3	-	
G30	VCCIO2	-		VCCIO2	-	
J29	VCCIO2	-		VCCIO2	-	
K27	VCCIO2	-		VCCIO2	-	
N25	VCCIO2	-		VCCIO2	-	
F20	VCCIO1	-		VCCIO1	-	
C19	VCCIO1	-		VCCIO1	-	
C12	VCCIO1	-		VCCIO1	-	
F11	VCCIO1	-		VCCIO1	-	
H1	GND	-		GND	-	
L4	GND	-		GND	-	
M3	GND	-		GND	-	
N5	GND	-		GND	-	
K2	GND	-		GND	-	
M2	GND	-		GND	-	
P6	GND	-		GND	-	
G4	GND	-		GND	-	
H3	GND	-		GND	-	
AC2	GND	-		GND	-	
AA3	GND	-		GND	-	
AE1	GND	-		GND	-	
Y4	GND	-		GND	-	
AB4	GND	-		GND	-	
AA5	GND	-		GND	-	
AE6	GND	-		GND	-	
AE8	GND	-		GND	-	
AH5	GND	-		GND	-	
AG9	GND	-		GND	-	
AG6	GND	-		GND	-	
AF11	GND	-		GND	-	
AG12	GND	-		GND	-	
AJ10	GND	-		GND	-	
AK26	GND	-		GND	-	
AJ22	GND	-		GND	-	
AF20	GND	-		GND	-	
AJ25	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E22	VCC12	-		VCC12	-	
E21	VCC12	-		VCC12	-	
E3	VCC12	-		VCC12	-	
E4	VCC12	-		VCC12	-	
E6	VCC12	-		VCC12	-	
E7	VCC12	-		VCC12	-	
E8	VCC12	-		VCC12	-	
E9	VCC12	-		VCC12	-	
E11	VCC12	-		VCC12	-	
E12	VCC12	-		VCC12	-	
A23	GND	-		GND	-	
A31	GND	-		GND	-	
AA13	GND	-		GND	-	
AA15	GND	-		GND	-	
AA18	GND	-		GND	-	
AA20	GND	-		GND	-	
AA26	GND	-		GND	-	
AA6	GND	-		GND	-	
AB10	GND	-		GND	-	
AB24	GND	-		GND	-	
AC14	GND	-		GND	-	
AC22	GND	-		GND	-	
AC29	GND	-		GND	-	
AC3	GND	-		GND	-	
AD11	GND	-		GND	-	
AD19	GND	-		GND	-	
AD27	GND	-		GND	-	
AD7	GND	-		GND	-	
AF12	GND	-		GND	-	
AF18	GND	-		GND	-	
AF24	GND	-		GND	-	
AF30	GND	-		GND	-	
AF4	GND	-		GND	-	
AG15	GND	-		GND	-	
AG21	GND	-		GND	-	
AG9	GND	-		GND	-	
AJ10	GND	-		GND	-	
AJ16	GND	-		GND	-	
AJ20	GND	-		GND	-	
AJ26	GND	-		GND	-	
AJ29	GND	-		GND	-	
AJ4	GND	-		GND	-	
AK13	GND	-		GND	-	
AK17	GND	-		GND	-	
AK23	GND	-		GND	-	
AK7	GND	-		GND	-	
AL1	GND	-		GND	-	
AL32	GND	-		GND	-	
AM2	GND	-		GND	-	
AM31	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P10	GND	-		GND	-	
P13	GND	-		GND	-	
P15	GND	-		GND	-	
P18	GND	-		GND	-	
P20	GND	-		GND	-	
P24	GND	-		GND	-	
R12	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R17	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
R6	GND	-		GND	-	
T15	GND	-		GND	-	
T18	GND	-		GND	-	
T30	GND	-		GND	-	
T4	GND	-		GND	-	
U15	GND	-		GND	-	
U18	GND	-		GND	-	
U29	GND	-		GND	-	
U3	GND	-		GND	-	
V12	GND	-		GND	-	
V14	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V21	GND	-		GND	-	
V27	GND	-		GND	-	
V7	GND	-		GND	-	
W13	GND	-		GND	-	
W15	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W9	GND	-		GND	-	
Y12	GND	-		GND	-	
Y14	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y30	GND	-		GND	-	
Y4	GND	-		GND	-	
N13	VCC	-		VCC	-	
N15	VCC	-		VCC	-	
N16	VCC	-		VCC	-	
N17	VCC	-		VCC	-	
N18	VCC	-		VCC	-	
N20	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H21	PT38D	1	D28/PCLKC1_6/MPI_DATA28	PT57D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT38C	1	D29/PCLKT1_6/MPI_DATA29	PT57C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT38B	1	A9/MPI_ADDR23	PT57B	1	A9/MPI_ADDR23
B19	PT38A	1	A10/MPI_ADDR24	PT57A	1	A10/MPI_ADDR24
H22	PT37D	1	D30/PCLKC1_7/MPI_DATA30	PT56D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT37C	1	D31/PCLKT1_7/MPI_DATA31	PT56C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT37B	1	A11/MPI_ADDR25	PT56B	1	A11/MPI_ADDR25
G20	PT37A	1	A12/MPI_ADDR26	PT56A	1	A12/MPI_ADDR26
K21	PT35D	1	D11/MPI_DATA11	PT55D	1	D11/MPI_DATA11
K22	PT35C	1	D12/MPI_DATA12	PT55C	1	D12/MPI_DATA12
A20	PT35B	1	A13/MPI_ADDR27	PT55B	1	A13/MPI_ADDR27
B20	PT35A	1	A14/MPI_ADDR28	PT55A	1	A14/MPI_ADDR28
L21	PT33D	1	A16/MPI_ADDR30	PT53D	1	A16/MPI_ADDR30
L20	PT33C	1	D13/MPI_DATA13	PT53C	1	D13/MPI_DATA13
D20	PT33B	1	A15/MPI_ADDR29	PT53B	1	A15/MPI_ADDR29
E20	PT33A	1	A17/MPI_ADDR31	PT53A	1	A17/MPI_ADDR31
L19	PT30D	1	A19/MPI_TSI21	PT52D	1	A19/MPI_TSI21
K19	PT30C	1	A20/MPI_BDIP	PT52C	1	A20/MPI_BDIP
D21	PT30B	1	A18/MPI_TSI20	PT52B	1	A18/MPI_TSI20
E21	PT30A	1	MPI_TEA	PT52A	1	MPI_TEA
M20	PT28D	1	D14/MPI_DATA14	PT51D	1	D14/MPI_DATA14
M19	PT28C	1	DP1/MPI_PAR1	PT51C	1	DP1/MPI_PAR1
F21	PT27B	1	A21/MPI_BURST	PT51B	1	A21/MPI_BURST
G21	PT27A	1	D15/MPI_DATA15	PT51A	1	D15/MPI_DATA15
H24	B_REFCLKP_L	-		B_REFCLKP_L	-	
J24	B_REFCLKN_L	-		B_REFCLKN_L	-	
L22	VCC12	-		VCC12	-	
E26	B_VDDIB3_L	-		B_VDDIB3_L	-	
G22	VCC12	-		VCC12	-	
E22	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
F22	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
L24	VCC12	-		VCC12	-	
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D22	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D23	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
K24	VCC12	-		VCC12	-	
F23	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
E23	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
D26	B_VDDIB2_L	-		B_VDDIB2_L	-	
G23	VCC12	-		VCC12	-	
D27	B_VDDIB1_L	-		B_VDDIB1_L	-	
G24	VCC12	-		VCC12	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C32	VCC12	-		VCC12	-	
E34	NC	-		PL22A	7	
F34	NC	-		PL22B	7	
F33	NC	-		PL24A	7	
G33	NC	-		PL24B	7	
K30	NC	-		PL25A	7	
L30	NC	-		PL25B	7	
G34	NC	-		PL26A	7	
H34	NC	-		PL26B	7	
M32	NC	-		PL39A	7	
N32	NC	-		PL39B	7	
P28	NC	-		PL39C	7	
R28	NC	-		PL39D	7	
J34	NC	-		PL41A	7	
K34	NC	-		PL41B	7	
P30	NC	-		PL41C	7	
R30	NC	-		PL41D	7	
W34	NC	-		PL59A	6	
Y34	NC	-		PL59B	6	
W32	NC	-		PL61A	6	
Y32	NC	-		PL61B	6	
AA34	NC	-		PL64A	6	
AB34	NC	-		PL64B	6	
AC34	NC	-		PL67A	6	
AD34	NC	-		PL67B	6	
Y30	NC	-		PL68A	6	
AA30	NC	-		PL68B	6	
AB33	NC	-		PL69A	6	
AC33	NC	-		PL69B	6	
AC2	NC	-		PR69B	3	
AB2	NC	-		PR69A	3	
AA5	NC	-		PR68B	3	
Y5	NC	-		PR68A	3	
AD1	NC	-		PR67B	3	
AC1	NC	-		PR67A	3	
AB1	NC	-		PR64B	3	
AA1	NC	-		PR64A	3	
Y3	NC	-		PR61B	3	
W3	NC	-		PR61A	3	
Y1	NC	-		PR59B	3	
W1	NC	-		PR59A	3	
R5	NC	-		PR41D	2	
P5	NC	-		PR41C	2	
K1	NC	-		PR41B	2	
J1	NC	-		PR41A	2	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
L21	PT55D	1	A16/MPI_ADDR30
L20	PT55C	1	D13/MPI_DATA13
D20	PT55B	1	A15/MPI_ADDR29
E20	PT55A	1	A17/MPI_ADDR31
L19	PT54D	1	A19/MPI_TSI_Z1
K19	PT54C	1	A20/MPI_BDIP
D21	PT54B	1	A18/MPI_TSI_Z0
E21	PT54A	1	MPI_TEA
M20	PT51D	1	D14/MPI_DATA14
M19	PT51C	1	DP1/MPI_PAR1
F21	PT51B	1	A21/MPI_BURST
G21	PT51A	1	D15/MPI_DATA15
H24	B_REFCLKP_L	-	
J24	B_REFCLKN_L	-	
L22	VCC12	-	
E26	B_VDDIB3_L	-	
G22	VCC12	-	
E22	B_HDINP3_L	-	PCS 361 CH 3 IN P
F22	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
L24	VCC12	-	
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D22	B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D23	B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
K24	VCC12	-	
F23	B_HDINN2_L	-	PCS 361 CH 2 IN N
E23	B_HDINP2_L	-	PCS 361 CH 2 IN P
D26	B_VDDIB2_L	-	
G23	VCC12	-	
D27	B_VDDIB1_L	-	
G24	VCC12	-	
E24	B_HDINP1_L	-	PCS 361 CH 1 IN P
F24	B_HDINN1_L	-	PCS 361 CH 1 IN N
A23	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L25	VCC12	-	
B23	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-	
B24	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-	
A24	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
K25	VCC12	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BB12	PB88B	4		PB102B	4	
AM17	PB88C	4		PB102C	4	
AL17	PB88D	4		PB102D	4	
AW14	PB89A	4		PB103A	4	
AW13	PB89B	4		PB103B	4	
AP16	PB89C	4		PB103C	4	
AN16	PB89D	4		PB103D	4	
BA13	PB91A	4		PB105A	4	
BA12	PB91B	4		PB105B	4	
AU13	PB91C	4		PB105C	4	
AU12	PB91D	4		PB105D	4	
BB11	PB92A	4		PB106A	4	
BB10	PB92B	4		PB106B	4	
AP15	PB92C	4		PB106C	4	
AN15	PB92D	4		PB106D	4	
AV13	PB93A	4		PB107A	4	
AV12	PB93B	4		PB107B	4	
AT13	PB93C	4		PB107C	4	
AT12	PB93D	4		PB107D	4	
BA11	PB95A	4		PB109A	4	
BA10	PB95B	4		PB109B	4	
AR13	PB95C	4		PB109C	4	
AR12	PB95D	4		PB109D	4	
AY11	PB96A	4		PB110A	4	
AY10	PB96B	4		PB110B	4	
AP14	PB96C	4		PB110C	4	
AN14	PB96D	4		PB110D	4	
BB9	PB97A	4		PB111A	4	
BB8	PB97B	4		PB111B	4	
AU11	PB97C	4		PB111C	4	
AU10	PB97D	4		PB111D	4	
AW11	PB99A	4		PB113A	4	
AW10	PB99B	4		PB113B	4	
AJ16	PB99C	4		PB113C	4	
AJ17	PB99D	4		PB113D	4	
BA9	PB100A	4		PB114A	4	
BA8	PB100B	4		PB114B	4	
AM15	PB100C	4		PB114C	4	
AL15	PB100D	4		PB114D	4	
AV11	PB101A	4		PB115A	4	
AV10	PB101B	4		PB115B	4	
AP13	PB101C	4		PB115C	4	
AP12	PB101D	4		PB115D	4	
BB7	PB103A	4		PB117A	4	
BB6	PB103B	4		PB117B	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP1	PR90B	3		PR109B	3	
AN1	PR90A	3		PR109A	3	
AK10	PR89D	3	VREF2_3	PR107D	3	VREF2_3
AJ10	PR89C	3		PR107C	3	
AM5	PR89B	3		PR107B	3	
AL5	PR89A	3		PR107A	3	
AL7	PR86D	3		PR104D	3	
AK7	PR86C	3		PR104C	3	
AM1	PR86B	3		PR104B	3	
AL1	PR86A	3		PR104A	3	
AJ11	PR85D	3		PR103D	3	
AH11	PR85C	3		PR103C	3	
AK5	PR85B	3		PR103B	3	
AJ5	PR85A	3		PR103A	3	
AK9	PR84D	3		PR99D	3	
AJ9	PR84C	3		PR99C	3	
AK3	PR84B	3		PR99B	3	
AJ3	PR84A	3		PR99A	3	
AK6	PR82D	3		PR98D	3	
AJ6	PR82C	3		PR98C	3	
AK2	PR82B	3		PR98B	3	
AJ2	PR82A	3		PR98A	3	
AH10	PR81D	3		PR96D	3	
AG10	PR81C	3		PR96C	3	
AK1	PR81B	3		PR96B	3	
AJ1	PR81A	3		PR96A	3	
AH9	PR80D	3		PR94D	3	
AG9	PR80C	3		PR94C	3	
AH2	PR80B	3		PR94B	3	
AG2	PR80A	3		PR94A	3	
AH8	PR78D	3		PR92D	3	
AG8	PR78C	3		PR92C	3	
AG1	PR78B	3		PR92B	3	
AH1	PR78A	3		PR92A	3	
AG14	PR77D	3		PR91D	3	
AF14	PR77C	3		PR91C	3	
AG4	PR77B	3		PR91B	3	
AF4	PR77A	3		PR91A	3	
AH7	PR76D	3	DIFFR_3	PR90D	3	DIFFR_3
AG7	PR76C	3		PR90C	3	
AG3	PR76B	3		PR90B	3	
AF3	PR76A	3		PR90A	3	
AH6	PR74D	3		PR88D	3	
AG6	PR74C	3		PR88C	3	
AF1	PR74B	3		PR88B	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D1	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
F1	VCC12	-		VCC12	-	
A3	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
E1	A_VDDOB0_R	-		A_VDDOB0_R	-	
B3	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
C2	A_VDDOB1_R	-		A_VDDOB1_R	-	
A4	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
B2	VCC12	-		VCC12	-	
B4	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
E3	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
D3	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
M10	VCC12	-		VCC12	-	
E2	A_VDDIB1_R	-		A_VDDIB1_R	-	
J11	VCC12	-		VCC12	-	
M11	A_VDDIB2_R	-		A_VDDIB2_R	-	
D4	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
E4	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
K9	VCC12	-		VCC12	-	
A5	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
D2	A_VDDOB2_R	-		A_VDDOB2_R	-	
B5	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
L10	A_VDDOB3_R	-		A_VDDOB3_R	-	
B6	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
G6	VCC12	-		VCC12	-	
A6	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
E5	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
D5	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
K12	VCC12	-		VCC12	-	
L13	A_VDDIB3_R	-		A_VDDIB3_R	-	
N14	VCC12	-		VCC12	-	
F9	B_VDDIB0_R	-		B_VDDIB0_R	-	
D6	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
E6	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
J8	VCC12	-		VCC12	-	
B7	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
G4	B_VDDOB0_R	-		B_VDDOB0_R	-	
A7	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
K8	B_VDDOB1_R	-		B_VDDOB1_R	-	
A8	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L9	VCC12	-		VCC12	-	
B8	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
E7	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
D7	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
F10	VCC12	-		VCC12	-	
K13	B_VDDIB1_R	-		B_VDDIB1_R	-	

Conventional Packaging**Commercial**

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7F256C	-7	fpBGA	256	COM	15.2
LFSC3GA15E-6F256C	-6	fpBGA	256	COM	15.2
LFSC3GA15E-5F256C	-5	fpBGA	256	COM	15.2
LFSC3GA15E-7F900C	-7	fpBGA	900	COM	15.2
LFSC3GA15E-6F900C	-6	fpBGA	900	COM	15.2
LFSC3GA15E-5F900C	-5	fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7F256C	-7	fpBGA	256	COM	15.2
LFSCM3GA15EP1-6F256C	-6	fpBGA	256	COM	15.2
LFSCM3GA15EP1-5F256C	-5	fpBGA	256	COM	15.2
LFSCM3GA15EP1-7F900C	-7	fpBGA	900	COM	15.2
LFSCM3GA15EP1-6F900C	-6	fpBGA	900	COM	15.2
LFSCM3GA15EP1-5F900C	-5	fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7F900C	-7	fpBGA	900	COM	25.4
LFSC3GA25E-6F900C	-6	fpBGA	900	COM	25.4
LFSC3GA25E-5F900C	-5	fpBGA	900	COM	25.4
LFSC3GA25E-7FF1020C ¹	-7	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FF1020C ¹	-6	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FF1020C ¹	-5	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7F900C	-7	fpBGA	900	COM	25.4
LFSCM3GA25EP1-6F900C	-6	fpBGA	900	COM	25.4
LFSCM3GA25EP1-5F900C	-5	fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FF1020C ¹	-7	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FF1020C ¹	-6	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FF1020C ¹	-5	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	115.2
LFSC3GA115E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	115.2
LFSC3GA115E-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	115.2
LFSC3GA115E-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).