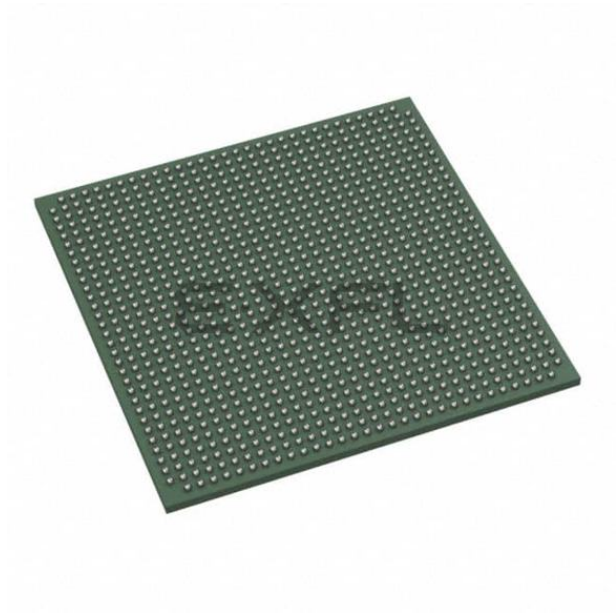
Lattice Semiconductor Corporation - LFSC3GA25E-5FF1020I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

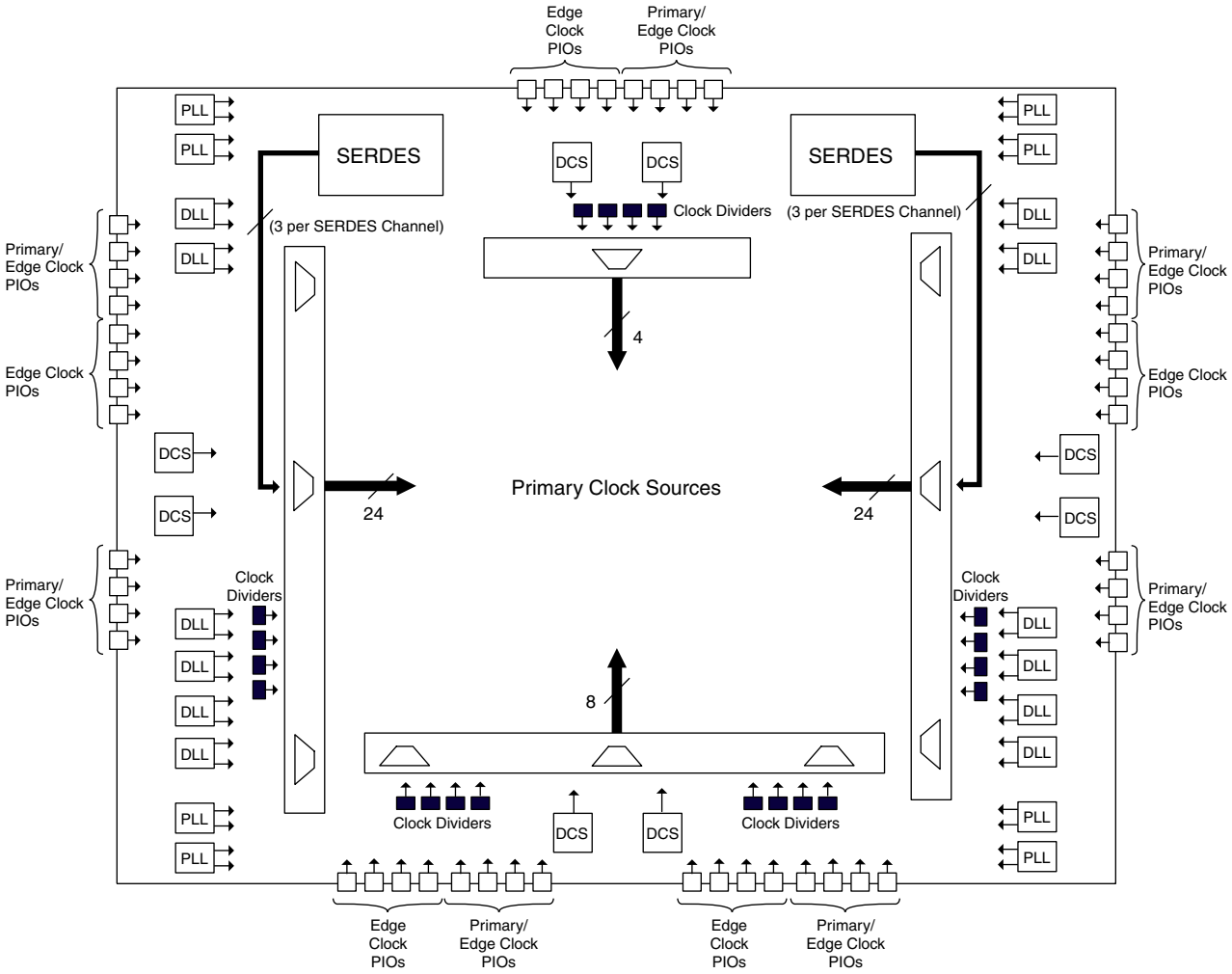
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	476
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga25e-5ff1020i

- Two outputs per PLL
- Clock divider outputs
- Digital Clock Select (DCS) block outputs
- Three outputs per SERDES quad

Figure 2-5 shows the arrangement of the primary clock sources.

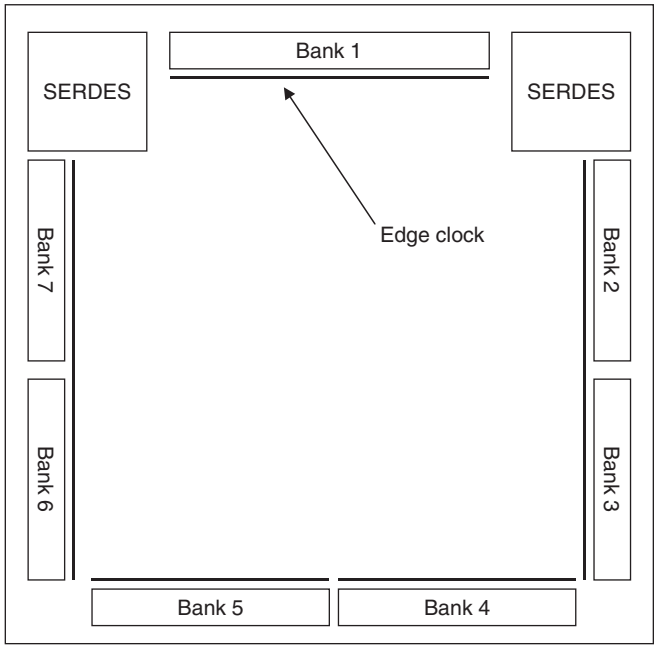
Figure 2-5. Clock Sources



Primary Clock Routing

The clock routing structure in LatticeSC devices consists of 12 Primary Clock lines per quadrant. The primary clocks are generated from 64:1 MUXs located in each quadrant. Three of the inputs to each 64:1 MUX comes from local routing, one is connected to GND and rest of the 60 inputs are from the primary clock sources. Figure 2-6 shows this clock routing.

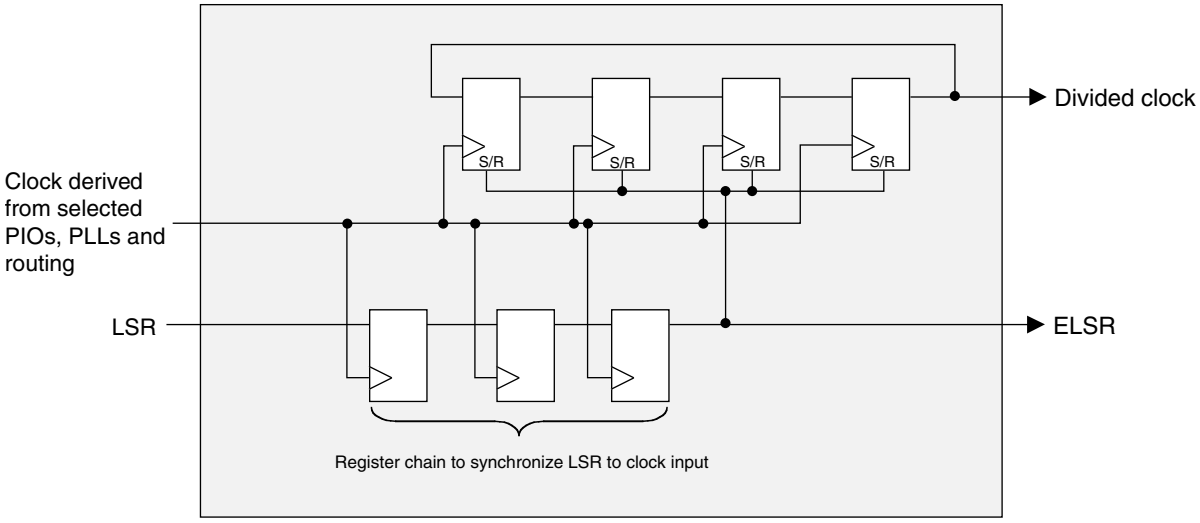
Figure 2-7. Edge Clock Resources



Precision Clock Divider

Each set of edge clocks has four high-speed dividers associated with it. These are intended for generating a slower speed system clock from the high-speed edge clock. The block operates in a DIV2 or DIV4 mode and maintains a known phase relationship between the divided down clock and high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PIOs, PLLs and routing. The clock divider outputs serve as primary clock sources. This circuit also generates an edge local set/reset (ELSR) signal which is fed to the PIOs via the edge clock network and is used for the rest of the I/O gearing logic.

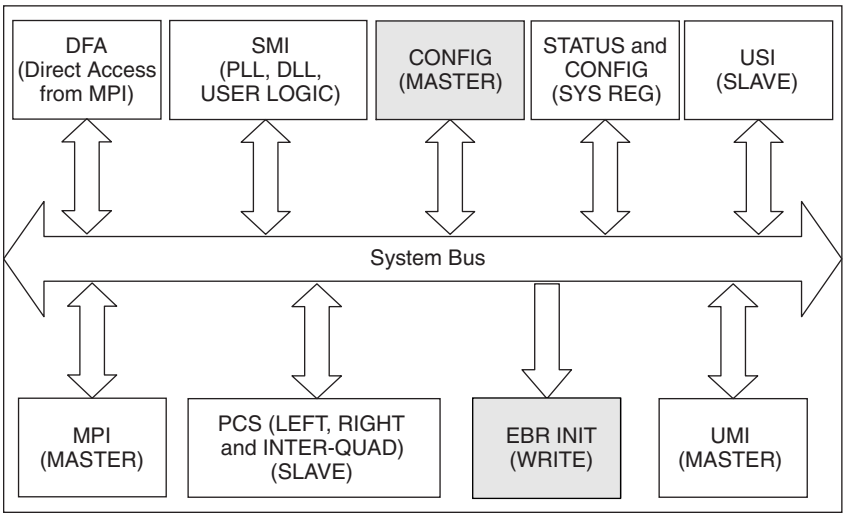
Figure 2-8. Clock Divider Circuit



Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is

Figure 2-31. LatticeSC System Bus Interfaces



Several interfaces exist between the System Bus and other FPGA elements. The MPI interface acts as a bridge between the external microprocessor bus and System Bus. The MPI may work in an independent clock domain from the System Bus if the System Bus clock is not sourced from the external microprocessor clock. Pipelined operation allows high-speed memory interface to the EBR and peripheral access without the requirement for additional cycles on the bus. Burst transfers allow optimal use of the memory interface by giving advance information of the nature of the transfers.

Details for the majority of the peripherals can be found in the associated technical documentation, see details at the end of this data sheet. Additional details of the MPI are provided below.

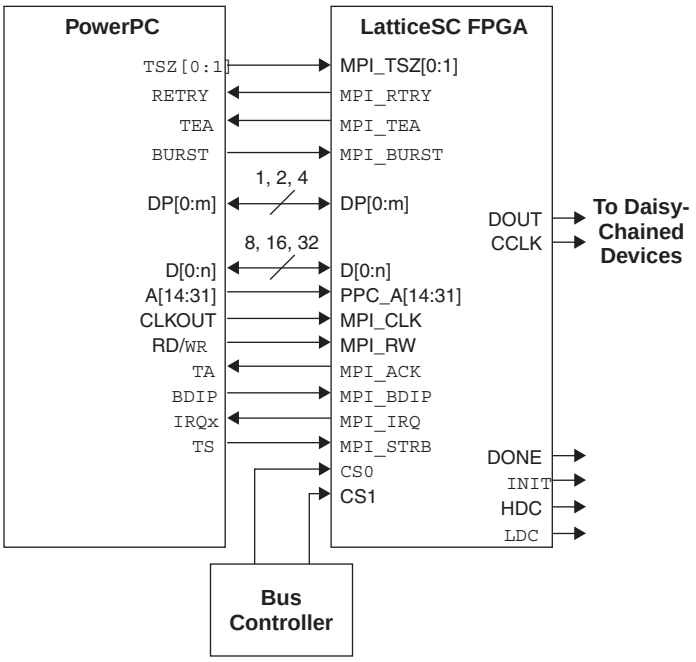
Microprocessor Interface (MPI)

The LatticeSC family devices have a dedicated synchronous MPI function block. The MPI is programmable to operate with PowerPC/PowerQUICC MPC860/MPC8260 series microprocessors. The MPI implements an 8-, 16-, or 32-bit interface with 1-bit, 2-bit, or 4-bit parity to the host processor (PowerPC) that can be used for configuration and read-back of the FPGA as well as for user-defined data processing and general monitoring of FPGA functions.

The control portion of the MPI is available following power-up of the FPGA if the mode pins specify MPI mode, even if the FPGA is not yet configured. The width of the data port is selectable among 8-, 16-, or 32-bit and the parity bus can be 1-, 2-, or 4-bit. In configuration mode the data and parity bus width are related to the state of the M[0:3] mode pins. For post-configuration use, the MPI must be included in the configuration bit stream by using an MPI library element in your design from the ispLEVER primitive library, or by setting the bit of the MPI configuration control register prior to the start of configuration. The user can also enable and disable the parity bus through the configuration bit stream. These pads can be used as general I/O when they are not needed for MPI use.

The MPI block also provides the capability to interface directly to the FPGA fabric with a databus after configuration.The bus protocol is still handled by the MPI block but the direct FPGA access allows high-speed block data transfers such as DMA transactions. Figure 2-32 shows one of the ways a PowerPC is connected to MPI.

Figure 2-32. PowerPCI and MPI Schematic



Configuration and Testing

The following section describes the configuration and testing features of the LatticeSC family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeSC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS33, 25 and 18 standards. For additional detail refer to technical information at the end of the data sheet.

Device Configuration

All LatticeSC devices contain three possible ports that can be used for device configuration. The serial port, which supports bit-wide configuration, and the sysCONFIG port that supports both byte-wide and serial configuration. The MPI port supports 8-bit, 16-bit or 32-bit configuration.

The serial port supports both the IEEE Std. 1149.1 Boundary Scan specification and the IEEE Std. 1532 In-System Configuration specification. The sysCONFIG port is a 20-pin interface with six of the I/Os used as dedicated pins and the rest being dual-use pins. When sysCONFIG mode is not used, these dual-use pins are available for general purpose I/O. All I/Os for the sysCONFIG and MPI ports are in I/O bank #1.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port. Once a configuration port is selected, that port is locked and another configuration port cannot be activated until the next re-initialization sequence. For additional detail refer to technical information at the end of the data sheet.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		2	—	1000	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		1.5625	—	1000	MHz
f_{VCO}	PLL VCO Frequency		100	—	1000	MHz
f_{PFD}	Phase Detector Input Frequency		2	—	700	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected (at 50% levels)	45	—	55	%
t_{OPJIT}[1]	Output Clock Period Jitter	2 MHz ≤ f_{PFD} ≤ 10 MHz	—	—	200	ps
		f_{PFD} > 10 MHz	—	—	100	ps
t_{CPJIT}[1]	Output Clock Cycle-to-Cycle Jitter		—	—	100	ps
t_{SKEW}	Output Clock-to-Clock Skew (Between Two Outputs with the Same Phase Setting)		—	—	20	ps
t_{LOCK}	PLL Lock-in Time		—	—	1	ms
t_{IPJIT}	Input Clock Period Jitter		—	—	±250	ps
t_{HI}	Input Clock High Time	At 80% level	350	—	—	ps
t_{LO}	Input Clock Low Time	At 20% level	350	—	—	ps
t_{RSWA}	Analog Reset Signal Pulse Width		100	—	—	ns
t_{RSWD}	Digital Reset Signal Pulse Width		3	—	—	ns
t_{DEL}	Timeshift Delay Step Size		40	80	120	ps
t_{RANGE}	Timeshift Delay Range		—	+/- 560	—	ps
f_{SS}	Spread Spectrum Modulation Frequency		30	—	500	KHz
% Spread	Percentage Downspread for SS Mode		0.5	—	1.5	%
	VCO Clock Phase Adjustment Accuracy		-5	—	5	°

1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps

LatticeSC/M sysCONFIG Port Timing (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Asynchronous Peripheral Configuration Mode				
t_{WRAP}	WRN, CS0N and CS1 Pulse Width	5	-	ns
t_{SAP}	D[7:0] Setup Time	1.5	-	ns
t_{RDYAP}	RDY Delay	—	8	ns
t_{BAP}	RDY Low	1	8	CCLK periods
t_{WR2AP}	Earliest WRN After RDY Goes High	0	—	ns
t_{DENAP}	RDN to D[7:0] Enable/Disable	—	7.5	ns
t_{DAP}	CCLK to DOUT	—	7.5	ns
sysCONFIG Slave Serial Configuration Mode				
t_{SSS}	DIN Setup Time	5.2	—	ns
t_{HSS}	DIN Hold Time	0	—	ns
t_{CHSS}	CCLK High Time	3.75	—	ns
t_{CLSS}	CCLK Low Time	3.75	—	ns
f_{CSS}	CCLK Frequency	—	150	MHz
t_{DSS}	CCLK to DOUT	—	7.5	ns
sysCONFIG Slave Parallel Configuration Mode				
t_{S1SP}	CS0N, CS1, WRN Setup Time	5.2	—	ns
t_{H1SP}	CS0N, CS1, WRN Hold Time	0	—	ns
t_{S2SP}	D[7:0] Setup Time	5.2	—	ns
t_{H2SP}	D[7:0] Hold Time	0	—	ns
t_{CHSP}	CCLK High Time	3.75	—	ns
t_{CL}	CCLK Low Time	3.75	—	ns
f_{CSP}	CCLK Frequency	—	150	MHz

sysCONFIG MPI Port

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{MPICTRL\_SET}$	MPI Control (MPCSTRBN, MPCWRN, MPCCLK, etc.) to MPCCLK Setup Time	4.9	—	5.2	—	5.5	—	ns
t_{MPIADR_SET}	MPI Address to MPCCLK Setup Time	3.9	—	4.2	—	4.5	—	ns
t_{MPIDAT_SET}	MPI Write Data to MPCCLK Setup Time	4.9	—	5.2	—	5.5	—	ns
$t_{MPIDPAR\_SET}$	MPI Write Parity Data to MPCCLK Setup Time	3.9	—	4.2	—	4.5	—	ns
t_{MPI_HLD}	All Hold Times	0	—	0	—	0	—	ns
$t_{MPICTRL\_DEL}$	MPCCLK to MPI Control (MPCTA, MPC-TEA, MPCRETRY)	—	5.6	—	6.7	—	8.7	ns
t_{MPIDAT_DEL}	MPCCLK to MPI Data	—	5.6	—	6.7	—	8.7	ns
$t_{MPIDPAR\_DEL}$	MPCCLK to MPI Parity Data	—	4.9	—	5.7	—	7.7	ns
$f_{MPI\_CLK\_FRQ}$	MPCCLK Frequency	—	100	—	83	—	66	MHz

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
N12	PB39C	4	
T15	PB40A	4	PCLKT4_3
R16	PB40B	4	PCLKC4_3
L12	PB43A	4	
M12	PB43B	4	
P16	PB44A	4	
N16	PB44B	4	
R14	PB47C	4	VREF1_4
P15	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
M13	PB48B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
N13	PB49A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
P14	PB49B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
M16	PR45B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
L16	PR45A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
M14	PR43B	3	
M15	PR43A	3	
K16	PR41D	3	VREF2_3
J16	PR37B	3	
H16	PR37A	3	
L13	PR35D	3	DIFFR_3
L14	PR35B	3	
L15	PR35A	3	
K12	PR31C	3	VREF1_3
J13	PR28D	3	PCLKC3_2
K13	PR28C	3	PCLKT3_2
H15	PR28B	3	
F16	PR28A	3	
J11	PR26D	3	PCLKC3_1
J12	PR26C	3	PCLKT3_1
J15	PR26B	3	PCLKC3_0
J14	PR26A	3	PCLKT3_0
E16	PR24D	2	PCLKC2_2
D16	PR24C	2	PCLKT2_2
H11	PR24B	2	PCLKC2_0
H12	PR24A	2	PCLKT2_0
H13	PR23B	2	PCLKC2_1
H14	PR23A	2	PCLKT2_1
G12	PR22D	2	DIFFR_2
G13	PR22C	2	VREF1_2
F8	PR22B	2	
F9	PR22A	2	
G16	PR18D	2	VREF2_2
F15	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT24A	1	MPI_TEA	PT30A	1	MPI_TEA
J18	PT23D	1	D14/MPI_DATA14	PT28D	1	D14/MPI_DATA14
K18	PT23C	1	DP1/MPI_PAR1	PT28C	1	DP1/MPI_PAR1
E20	PT23B	1	A21/MPI_BURST	PT27B	1	A21/MPI_BURST
F20	PT23A	1	D15/MPI_DATA15	PT27A	1	D15/MPI_DATA15
C23	B_REFCLKP_L	-		B_REFCLKP_L	-	
D23	B_REFCLKN_L	-		B_REFCLKN_L	-	
B23	VCC12	-		VCC12	-	
H21	B_VDDIB3_L	-		B_VDDIB3_L	-	
F21	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
G21	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D21	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D22	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G22	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
F22	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H22	B_VDDIB2_L	-		B_VDDIB2_L	-	
H24	B_VDDIB1_L	-		B_VDDIB1_L	-	
G23	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
H23	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
A24	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
B24	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-		B_VDDOB1_L	-	
B25	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-		B_VDDOB0_L	-	
A25	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
G25	B_HDINN0_L	-	PCS 361 CH 0 IN N	B_HDINN0_L	-	PCS 361 CH 0 IN N
F25	B_HDINP0_L	-	PCS 361 CH 0 IN P	B_HDINP0_L	-	PCS 361 CH 0 IN P
H25	B_VDDIB0_L	-		B_VDDIB0_L	-	
H26	A_VDDIB3_L	-		A_VDDIB3_L	-	
F26	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
G26	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
D26	A_VDDOB3_L	-		A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
D27	A_VDDOB2_L	-		A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
G27	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
F27	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
H27	A_VDDIB2_L	-		A_VDDIB2_L	-	
F29	A_VDDIB1_L	-		A_VDDIB1_L	-	
G28	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
H28	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A29	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B29	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
D29	A_VDDOB1_L	-		A_VDDOB1_L	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L33	PL27B	7		PL35B	7	
M30	PL27C	7		PL35C	7	
N30	PL27D	7		PL35D	7	
M31	PL29A	7		PL37A	7	
N31	PL29B	7		PL37B	7	
P24	PL29C	7		PL37C	7	
R24	PL29D	7		PL37D	7	
M33	PL30A	7		PL42A	7	
N33	PL30B	7		PL42B	7	
U25	PL30C	7		PL42C	7	
T25	PL30D	7		PL42D	7	
L34	PL31A	7		PL43A	7	
M34	PL31B	7		PL43B	7	
P29	PL31C	7		PL43C	7	
R29	PL31D	7		PL43D	7	
N34	PL34A	7		PL46A	7	
P34	PL34B	7		PL46B	7	
R27	PL34C	7		PL46C	7	
T27	PL34D	7		PL46D	7	
R32	PL35A	7	PCLKT7_1	PL47A	7	PCLKT7_1
R31	PL35B	7	PCLKC7_1	PL47B	7	PCLKC7_1
U24	PL35C	7	PCLKT7_3	PL47C	7	PCLKT7_3
T24	PL35D	7	PCLKC7_3	PL47D	7	PCLKC7_3
P33	PL36A	7	PCLKT7_0	PL48A	7	PCLKT7_0
R33	PL36B	7	PCLKC7_0	PL48B	7	PCLKC7_0
T26	PL36C	7	PCLKT7_2	PL48C	7	PCLKT7_2
U26	PL36D	7	PCLKC7_2	PL48D	7	PCLKC7_2
T32	PL38A	6	PCLKT6_0	PL50A	6	PCLKT6_0
T31	PL38B	6	PCLKC6_0	PL50B	6	PCLKC6_0
U29	PL38C	6	PCLKT6_1	PL50C	6	PCLKT6_1
V29	PL38D	6	PCLKC6_1	PL50D	6	PCLKC6_1
T30	PL39A	6		PL51A	6	
U30	PL39B	6		PL51B	6	
U27	PL39C	6	PCLKT6_3	PL51C	6	PCLKT6_3
V27	PL39D	6	PCLKC6_3	PL51D	6	PCLKC6_3
R34	PL40A	6		PL52A	6	
T34	PL40B	6		PL52B	6	
U28	PL40C	6	PCLKT6_2	PL52C	6	PCLKT6_2
V28	PL40D	6	PCLKC6_2	PL52D	6	PCLKC6_2
V30	PL43A	6		PL55A	6	
W30	PL43B	6		PL55B	6	
W27	PL43C	6	VREF1_6	PL55C	6	VREF1_6
Y27	PL43D	6		PL55D	6	
T33	PL44A	6		PL56A	6	
U33	PL44B	6		PL56B	6	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD29	PL60D	6		PL84D	6	
AE31	PL61A	6		PL85A	6	
AF31	PL61B	6		PL85B	6	
AF30	PL61C	6		PL85C	6	
AF29	PL61D	6		PL85D	6	
AH33	PL62A	6		PL86A	6	
AJ33	PL62B	6		PL86B	6	
AC28	PL62C	6		PL86C	6	
AD28	PL62D	6		PL86D	6	
AH32	PL65A	6		PL89A	6	
AJ32	PL65B	6		PL89B	6	
AD27	PL65C	6		PL89C	6	
AE27	PL65D	6	VREF2_6	PL89D	6	VREF2_6
AG34	PL66A	6		PL90A	6	
AH34	PL66B	6		PL90B	6	
AC26	PL66C	6		PL90C	6	
AB26	PL66D	6		PL90D	6	
AK33	PL67A	6		PL91A	6	
AL33	PL67B	6		PL91B	6	
AG30	PL67C	6		PL91C	6	
AH30	PL67D	6		PL91D	6	
AL34	PL69A	6		PL93A	6	
AM34	PL69B	6		PL93B	6	
AJ30	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL93C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL93D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL70A	6		PL94A	6	
AH31	PL70B	6		PL94B	6	
AD26	PL70C	6		PL94C	6	
AD25	PL70D	6		PL94D	6	
AL32	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL95A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL95B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL95C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL95D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-		XRES	-	
AF27	TEMP	6		TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AN33	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AH29	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AJ29	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AM32	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AM31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AG27	PB4C	5		PB4C	5	
AG26	PB4D	5		PB4D	5	
AL29	PB5A	5		PB5A	5	
AL28	PB5B	5		PB5B	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C2	VCCJ	-		VCCJ	-	
M9	TDO	-	TDO	TDO	-	TDO
L9	TMS	-		TMS	-	
D1	TCK	-		TCK	-	
C1	TDI	-		TDI	-	
J8	PROGRAMN	1		PROGRAMN	1	
K8	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
B2	CCLK	1		CCLK	1	
H9	RESP_URC	-		RESP_URC	-	
H10	VCC12	-		VCC12	-	
H8	A_REFCLKN_R	-		A_REFCLKN_R	-	
G8	A_REFCLKP_R	-		A_REFCLKP_R	-	
C3	VCC12	-		VCC12	-	
D3	A_VDDIB0_R	-		A_VDDIB0_R	-	
A3	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B3	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E5	VCC12	-		VCC12	-	
A4	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
F6	A_VDDOB0_R	-		A_VDDOB0_R	-	
B4	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
F7	A_VDDOB1_R	-		A_VDDOB1_R	-	
B5	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
E6	VCC12	-		VCC12	-	
A5	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
B6	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
A6	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
C6	VCC12	-		VCC12	-	
D4	A_VDDIB1_R	-		A_VDDIB1_R	-	
C7	VCC12	-		VCC12	-	
D5	A_VDDIB2_R	-		A_VDDIB2_R	-	
A7	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
B7	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
E7	VCC12	-		VCC12	-	
A8	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
F8	A_VDDOB2_R	-		A_VDDOB2_R	-	
B8	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
F9	A_VDDOB3_R	-		A_VDDOB3_R	-	
B9	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
E8	VCC12	-		VCC12	-	
A9	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
B10	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
A10	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
C10	VCC12	-		VCC12	-	
D6	A_VDDIB3_R	-		A_VDDIB3_R	-	
G10	VCC12	-		VCC12	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H21	PT38D	1	D28/PCLKC1_6/MPI_DATA28	PT57D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT38C	1	D29/PCLKT1_6/MPI_DATA29	PT57C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT38B	1	A9/MPI_ADDR23	PT57B	1	A9/MPI_ADDR23
B19	PT38A	1	A10/MPI_ADDR24	PT57A	1	A10/MPI_ADDR24
H22	PT37D	1	D30/PCLKC1_7/MPI_DATA30	PT56D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT37C	1	D31/PCLKT1_7/MPI_DATA31	PT56C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT37B	1	A11/MPI_ADDR25	PT56B	1	A11/MPI_ADDR25
G20	PT37A	1	A12/MPI_ADDR26	PT56A	1	A12/MPI_ADDR26
K21	PT35D	1	D11/MPI_DATA11	PT55D	1	D11/MPI_DATA11
K22	PT35C	1	D12/MPI_DATA12	PT55C	1	D12/MPI_DATA12
A20	PT35B	1	A13/MPI_ADDR27	PT55B	1	A13/MPI_ADDR27
B20	PT35A	1	A14/MPI_ADDR28	PT55A	1	A14/MPI_ADDR28
L21	PT33D	1	A16/MPI_ADDR30	PT53D	1	A16/MPI_ADDR30
L20	PT33C	1	D13/MPI_DATA13	PT53C	1	D13/MPI_DATA13
D20	PT33B	1	A15/MPI_ADDR29	PT53B	1	A15/MPI_ADDR29
E20	PT33A	1	A17/MPI_ADDR31	PT53A	1	A17/MPI_ADDR31
L19	PT30D	1	A19/MPI_TSIZ1	PT52D	1	A19/MPI_TSIZ1
K19	PT30C	1	A20/MPI_BDIP	PT52C	1	A20/MPI_BDIP
D21	PT30B	1	A18/MPI_TSIZ0	PT52B	1	A18/MPI_TSIZ0
E21	PT30A	1	MPI_TEA	PT52A	1	MPI_TEA
M20	PT28D	1	D14/MPI_DATA14	PT51D	1	D14/MPI_DATA14
M19	PT28C	1	DP1/MPI_PAR1	PT51C	1	DP1/MPI_PAR1
F21	PT27B	1	A21/MPI_BURST	PT51B	1	A21/MPI_BURST
G21	PT27A	1	D15/MPI_DATA15	PT51A	1	D15/MPI_DATA15
H24	B_REFCLKP_L	-		B_REFCLKP_L	-	
J24	B_REFCLKN_L	-		B_REFCLKN_L	-	
L22	VCC12	-		VCC12	-	
E26	B_VDDIB3_L	-		B_VDDIB3_L	-	
G22	VCC12	-		VCC12	-	
E22	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
F22	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
L24	VCC12	-		VCC12	-	
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D22	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D23	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
K24	VCC12	-		VCC12	-	
F23	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
E23	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
D26	B_VDDIB2_L	-		B_VDDIB2_L	-	
G23	VCC12	-		VCC12	-	
D27	B_VDDIB1_L	-		B_VDDIB1_L	-	
G24	VCC12	-		VCC12	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB15	VCC12	-		VCC12	-	
AB20	VCC12	-		VCC12	-	
N15	VCC12	-		VCC12	-	
N20	VCC12	-		VCC12	-	
R13	VCC12	-		VCC12	-	
R22	VCC12	-		VCC12	-	
Y13	VCC12	-		VCC12	-	
Y22	VCC12	-		VCC12	-	
AA12	VCCAUX	-		VCCAUX	-	
AA23	VCCAUX	-		VCCAUX	-	
AB12	VCCAUX	-		VCCAUX	-	
AB16	VCCAUX	-		VCCAUX	-	
AB17	VCCAUX	-		VCCAUX	-	
AB18	VCCAUX	-		VCCAUX	-	
AB19	VCCAUX	-		VCCAUX	-	
AB23	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
Y19	GND	-		GND	-	
AC14	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC21	VCCAUX	-		VCCAUX	-	
AC22	VCCAUX	-		VCCAUX	-	
AC23	VCCAUX	-		VCCAUX	-	
M13	VCCAUX	-		VCCAUX	-	
M14	VCCAUX	-		VCCAUX	-	
M18	VCCAUX	-		VCCAUX	-	
M21	VCCAUX	-		VCCAUX	-	
M22	VCCAUX	-		VCCAUX	-	
N12	VCCAUX	-		VCCAUX	-	
N16	VCCAUX	-		VCCAUX	-	
N17	VCCAUX	-		VCCAUX	-	
N18	VCCAUX	-		VCCAUX	-	
N19	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
P12	VCCAUX	-		VCCAUX	-	
P23	VCCAUX	-		VCCAUX	-	
T13	VCCAUX	-		VCCAUX	-	
T22	VCCAUX	-		VCCAUX	-	
U12	VCCAUX	-		VCCAUX	-	
U13	VCCAUX	-		VCCAUX	-	
U22	VCCAUX	-		VCCAUX	-	
V13	VCCAUX	-		VCCAUX	-	
V22	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP27	PB26A	5	
AP26	PB26B	5	
AK25	PB26C	5	
AK24	PB26D	5	
AN25	PB29A	5	
AN24	PB29B	5	
AE22	PB29C	5	
AE21	PB29D	5	
AM26	PB31A	5	
AM25	PB31B	5	
AF22	PB31C	5	
AF21	PB31D	5	
AN23	PB47A	5	
AN22	PB47B	5	
AP23	PB57A	5	
AP22	PB57B	5	
AG21	PB57C	5	
AG20	PB57D	5	
AP25	PB50A	5	PCLKT5_3
AP24	PB50B	5	PCLKC5_3
AD21	PB50C	5	PCLKT5_4
AD20	PB50D	5	PCLKC5_4
AL23	PB51A	5	PCLKT5_5
AL22	PB51B	5	PCLKC5_5
AH24	PB51C	5	
AH23	PB51D	5	
AM23	PB53A	5	PCLKT5_0
AM22	PB53B	5	PCLKC5_0
AJ24	PB53C	5	
AJ23	PB53D	5	VREF2_5
AN21	PB54A	5	PCLKT5_1
AN20	PB54B	5	PCLKC5_1
AE19	PB54C	5	PCLKT5_6
AD19	PB54D	5	PCLKC5_6
AK21	PB55A	5	PCLKT5_2
AK20	PB55B	5	PCLKC5_2
AK23	PB55C	5	PCLKT5_7
AK22	PB55D	5	PCLKC5_7
AL20	PB58A	5	
AL19	PB58B	5	
AG19	PB58C	5	
AF19	PB58D	5	
AP21	PB61A	5	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
W7	GND	-	
AA14	VCC	-	
AA16	VCC	-	
AA17	VCC	-	
AA18	VCC	-	
AA19	VCC	-	
AA21	VCC	-	
AB13	VCC	-	
AB22	VCC	-	
N13	VCC	-	
N22	VCC	-	
P14	VCC	-	
P16	VCC	-	
P17	VCC	-	
P18	VCC	-	
P19	VCC	-	
P21	VCC	-	
R15	VCC	-	
R17	VCC	-	
R18	VCC	-	
R20	VCC	-	
T14	VCC	-	
T16	VCC	-	
T19	VCC	-	
T21	VCC	-	
U14	VCC	-	
U15	VCC	-	
U17	VCC	-	
U18	VCC	-	
U20	VCC	-	
U21	VCC	-	
V14	VCC	-	
V15	VCC	-	
V17	VCC	-	
V18	VCC	-	
V20	VCC	-	
V21	VCC	-	
W14	VCC	-	
W16	VCC	-	
W19	VCC	-	
W21	VCC	-	
Y15	VCC	-	
Y17	VCC	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
R12	VTT_2	2	
T12	VTT_2	2	
AB11	VTT_3	3	
W12	VTT_3	3	
Y12	VTT_3	3	
AC15	VTT_4	4	
AC16	VTT_4	4	
AD13	VTT_4	4	
AC19	VTT_5	5	
AC20	VTT_5	5	
AD22	VTT_5	5	
AB24	VTT_6	6	
W23	VTT_6	6	
Y23	VTT_6	6	
N24	VTT_7	7	
R23	VTT_7	7	
T23	VTT_7	7	
M12	VDDAX25_R	-	
M23	VDDAX25_L	-	
Y16	GND	-	
Y14	GND	-	
N21	VCC12	-	
P22	VCC12	-	
AA22	VCC12	-	
AB21	VCC12	-	
AB14	VCC12	-	
AA13	VCC12	-	
P13	VCC12	-	
N14	VCC12	-	
G26	NC	-	
G9	NC	-	
J12	NC	-	
H12	NC	-	
H23	NC	-	
J23	NC	-	

1. Differential pair grouping within a PCI is A (True) and B (complement) and C (True) and D (Complement).
2. The LatticeSC/M115 in an 1152-pin package supports a 32-bit MPI interface.

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D32	C_HDINP1_L	-	PCS 362 CH 1 IN P	C_HDINP1_L	-	PCS 362 CH 1 IN P
E32	C_HDINN1_L	-	PCS 362 CH 1 IN N	C_HDINN1_L	-	PCS 362 CH 1 IN N
B31	C_HDOUTP1_L	-	PCS 362 CH 1 OUT P	C_HDOUTP1_L	-	PCS 362 CH 1 OUT P
K32	VCC12	-		VCC12	-	
A31	C_HDOUTN1_L	-	PCS 362 CH 1 OUT N	C_HDOUTN1_L	-	PCS 362 CH 1 OUT N
L32	C_VDDOB1_L	-		C_VDDOB1_L	-	
A32	C_HDOUTN0_L	-	PCS 362 CH 0 OUT N	C_HDOUTN0_L	-	PCS 362 CH 0 OUT N
M31	C_VDDOB0_L	-		C_VDDOB0_L	-	
B32	C_HDOUTP0_L	-	PCS 362 CH 0 OUT P	C_HDOUTP0_L	-	PCS 362 CH 0 OUT P
H37	VCC12	-		VCC12	-	
E33	C_HDINN0_L	-	PCS 362 CH 0 IN N	C_HDINN0_L	-	PCS 362 CH 0 IN N
D33	C_HDINP0_L	-	PCS 362 CH 0 IN P	C_HDINP0_L	-	PCS 362 CH 0 IN P
G31	C_VDDIB0_L	-		C_VDDIB0_L	-	
J29	VCC12	-		VCC12	-	
L29	B_REFCLKP_L	-		B_REFCLKP_L	-	
M29	B_REFCLKN_L	-		B_REFCLKN_L	-	
J31	VCC12	-		VCC12	-	
H31	B_VDDIB3_L	-		B_VDDIB3_L	-	
J30	VCC12	-		VCC12	-	
D34	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
E34	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
B33	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
H38	VCC12	-		VCC12	-	
A33	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
C38	B_VDDOB3_L	-		B_VDDOB3_L	-	
A34	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
L31	B_VDDOB2_L	-		B_VDDOB2_L	-	
B34	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G38	VCC12	-		VCC12	-	
E35	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
D35	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H32	B_VDDIB2_L	-		B_VDDIB2_L	-	
K29	VCC12	-		VCC12	-	
K30	B_VDDIB1_L	-		B_VDDIB1_L	-	
F33	VCC12	-		VCC12	-	
D36	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
E36	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
B35	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L34	VCC12	-		VCC12	-	
A35	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
K35	B_VDDOB1_L	-		B_VDDOB1_L	-	
A36	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
G39	B_VDDOB0_L	-		B_VDDOB0_L	-	
B36	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
J35	VCC12	-		VCC12	-	

Industrial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-6F256I	-6	fpBGA	256	IND	15.2
LFSC3GA15E-5F256I	-5	fpBGA	256	IND	15.2
LFSC3GA15E-6F900I	-6	fpBGA	900	IND	15.2
LFSC3GA15E-5F900I	-5	fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-6F256I	-6	fpBGA	256	IND	15.2
LFSCM3GA15EP1-5F256I	-5	fpBGA	256	IND	15.2
LFSCM3GA15EP1-6F900I	-6	fpBGA	900	IND	15.2
LFSCM3GA15EP1-5F900I	-5	fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-6F900I	-6	fpBGA	900	IND	25.4
LFSC3GA25E-5F900I	-5	fpBGA	900	IND	25.4
LFSC3GA25E-6FF1020I[1]	-6	Organic fcBGA	1020	IND	25.4
LFSC3GA25E-5FF1020I[1]	-5	Organic fcBGA	1020	IND	25.4
LFSC3GA25E-6FFA1020I	-6	Organic fcBGA Revision 2	1020	IND	25.4
LFSC3GA25E-5FFA1020I	-5	Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-6F900I	-6	fpBGA	900	IND	25.4
LFSCM3GA25EP1-5F900I	-5	fpBGA	900	IND	25.4
LFSCM3GA25EP1-6FF1020I[1]	-6	Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-5FF1020I[1]	-5	Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-6FFA1020I	-6	Organic fcBGA Revision 2	1020	IND	25.4
LFSCM3GA25EP1-5FFA1020I	-5	Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-6FF1020I[1]	-6	Organic fcBGA	1020	IND	40.4
LFSC3GA40E-5FF1020I[1]	-5	Organic fcBGA	1020	IND	40.4
LFSC3GA40E-6FFA1020I	-6	Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-5FFA1020I	-5	Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-6FC1152I[2]	-6	Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-5FC1152I[2]	-5	Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-6FF1152I	-6	Organic fcBGA	1152	IND	40.4
LFSC3GA40E-5FF1152I	-5	Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Date	Version	Section	Change Summary
December 2011	02.4	DC and Switching Characteristics	Updated JTAG Port Timing Specifications table.