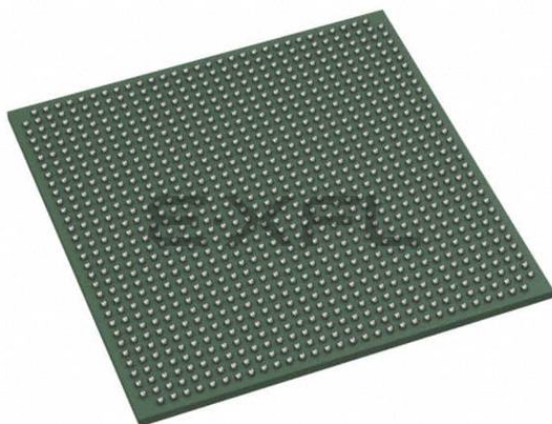




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	476
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga25e-5ffn1020c

Table 1-1. LatticeSC Family Selection Guide¹

Device	SC15	SC25	SC40	SC80	SC115
LUT4s (K)	15	25	40	80	115
sysMEM Blocks (18Kb)	56	104	216	308	424
Embedded Memory (Mbits)	1.03	1.92	3.98	5.68	7.8
Max. Distributed Memory (Mbits)	0.24	0.41	0.65	1.28	1.84
Number of 3.8Gbps SERDES (Max.)	8	16	16	32	32
DLLs	12	12	12	12	12
Analog PLLs	8	8	8	8	8
MACO Blocks	4	6	10	10	12
Package I/O/SERDES Combinations (1mm ball pitch)					
256-ball fpBGA (17 x 17mm)	139/4				
900-ball fpBGA (31 x 31mm)	300/8	378/8			
1020-ball fcBGA (33 x 33mm) ²		476/16	562/16		
1152-ball fcBGA (35 x 35mm) ³			604/16	660/16	660/16
1704-ball fcBGA (42.5 x 42.5mm) ³				904/32	942/32

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per [PCN #02A-10](#).
3. Ceramic fcBGA converted to organic fcBGA per [PCN #01A-10](#).

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

Table 1-2. LatticeSCM Family

Device	SCM15	SCM25	SCM40	SCM80	SCM115
flexiMAC Blocks • 1GbE Mode • 10GbE Mode • PCI Express Mode	1	2	2	2	4
SPI4.2 Blocks	1	2	2	2	2
Memory Controller Blocks • DDR/DDR2 DRAM Mode • QDR II/II+ SRAM Mode • RLDRAM I • RLDRAM II CIO/SIO	1	2	2	2	2
Low-Speed CDR Blocks	0	0	2	2	2
PCI Express LTSSM (PHY) Blocks	1	0	2	2	2

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

Introduction

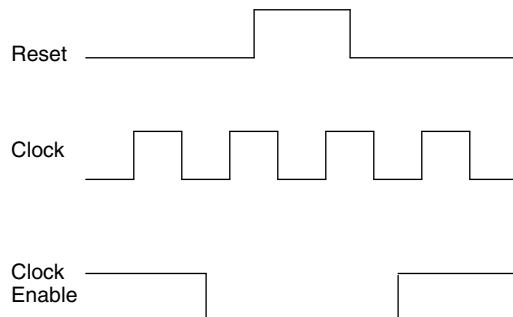
The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset, as shown in Figure 2-16.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM, FIFO and shift register implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-16. The reset timing rules apply to the RPRreset input vs. the RE input and the RST input vs. the WE and RE inputs. Both RST and RPRreset are always asynchronous EBR inputs. For the EBR shift register mode, the GSR signal is always enabled and the local RESET pin is always asynchronous.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled. For more information about on-chip memory, see TN1094, [On-Chip Memory Usage Guide for LatticeSC Devices](#).

Programmable I/O Cells (PIC)

Each PIC contains four PIOs connected to their respective PURESPEED I/O Buffer which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to PURESPEED I/O buffer, and receives input (DI) from the buffer. The PIO contains advanced capabilities to allow the support of speeds up to 2Gbps. These include dedicated shift and DDR logic and adaptive input logic. The dedicated resources simplify the design of robust interfaces.

Figure 2-26. LatticeSC Banks

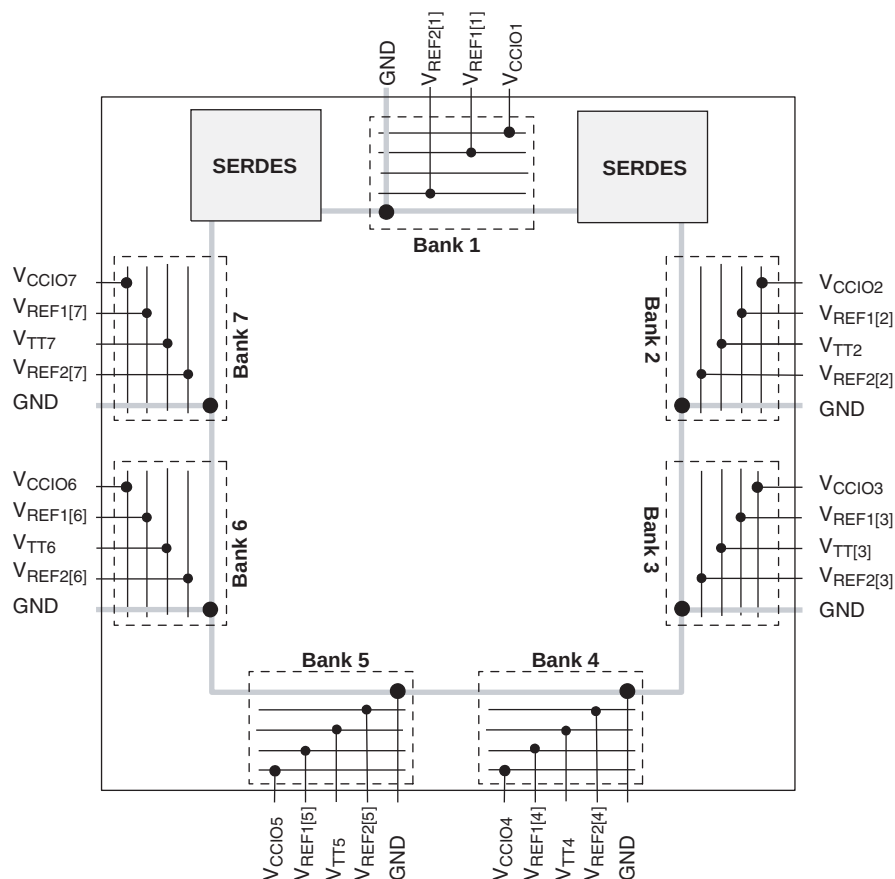


Table 2-7. Maximum Number of I/Os Per Bank in LatticeSC Family

Device	LFSC/M15	LFSC/M25	LFSC/M40	LFSC/M80	LFSC/M115
Bank1	104	80	136	80	136
Bank2	28	36	60	96	136
Bank3	60	84	96	132	156
Bank4	72	100	124	184	208
Bank5	72	100	124	184	208
Bank6	60	84	96	132	156
Bank7	28	36	60	96	136

Note: Not all the I/Os of the Banks are available in all the packages

The LatticeSC devices contain three types of PURESPEED I/O buffers:

1. **Left and Right Sides (Banks 2, 3, 6 and 7)**

These buffers can support LVCMOS standards up to 2.5V. A differential output driver (for LVDS and RSFS) is provided on all primary PIO pairs (A and B) and differential receivers are available on all pairs. Complimentary drivers are available. Adaptive input logic is available on PIOs A or C.

2. **Top Side (Bank 1)**

These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but differential drivers for LVDS and RSFS are not available. Adaptive input logic is not available on this side. Complimentary output drivers are available.

PURESPEED I/O Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V _{IL}		V _{IH}		V _{OL} Max. (V)	V _{OH} Min. (V)	I _{OL} (mA)	I _{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 33	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 25	-0.3	0.7	1.7	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 18	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 15	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 12	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.3	VCCIO - 0.3	12, 8, 4, 2	-12, -8, -4, -2
					0.2	VCCIO - 0.2	0.1	-0.1
PCIX15	-0.3	0.3VCCIO	0.5VCCIO	1.5	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCI33	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCIX33	-0.3	0.35VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
AGP-1X, AGP-2X	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
SSTL3_I	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.7	VCCIO - 1.1	8	-8
SSTS3_I OST ²	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 1.3	8	-8
SSTL3_II	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.5	VCCIO - 0.9	16	-16
SSTL3_II OST ²	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 0.13	16	-16
SSTL2_I	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.54	VCCIO - 0.62	7.6	-7.6
SSTL2_I OST ²	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	7.6	-7.6
SSTL2_II	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.35	VCCIO - 0.43	15.2	-15.2
SSTL2_II OST ²	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	15.2	-15.2
SSTL18_I	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
SSTL18_II	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
HSTL15_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	8	-8
HSTL15_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	16	-16
HSTL15_III ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL15_IV ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	9.6	-9.6
HSTL18_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	19.2	-19.2
HSTL18_III ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_IV ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
GTL12 ¹ , GTLPLUS15 ¹	-0.3	VREF - 0.2	VREF + 0.2	N/A	N/A	N/A	N/A	N/A

1. Input only.

2. Input with on-chip series termination.

Switching Characteristics

All devices are 100% functionally tested. Listed below are representative values of internal and external timing parameters. For more specific, more precise, and worst-case guaranteed data at a particular temperature and voltage, use the values reported by the static timing analyzer in the ispLEVER design tool from Lattice and back-annotate to the simulation net list.

Figure 3-12. Waveforms First Read after Full Flag

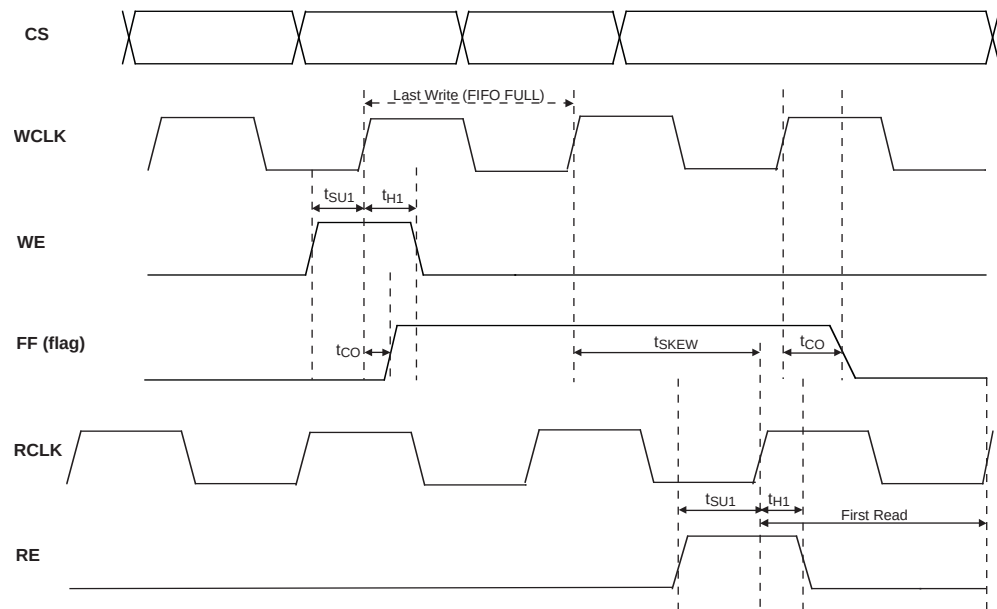
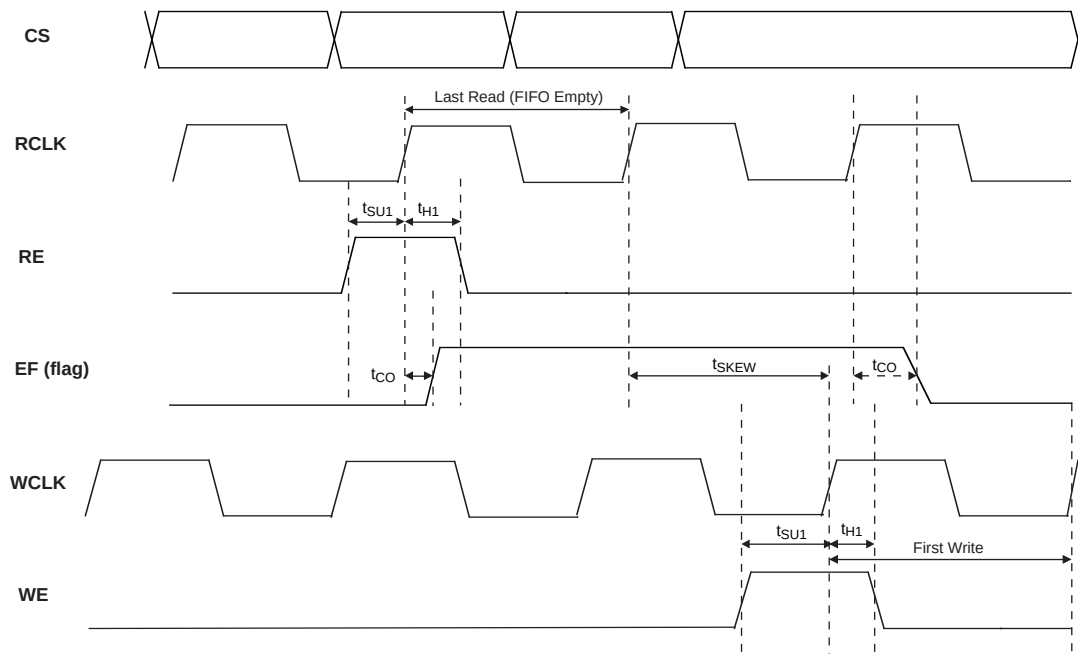


Figure 3-13. Waveform First Write after Empty Flag



Pin Information Summary

Pin Type		256 fpBGA	900 fpBGA		1020 fcBGA	
		LFSC/M15	LFSC/M15	LFSC/M25	LFSC/M25	LFSC/M40
Single Ended User I/O		139	300	378	476	562
Differential Pair User I/O		60	141	182	235	277
LVDS Output Pairs		22	44	60	60	78
Configuration	Dedicated	9	11	11	11	11
	Muxes/MPI sysBus	0	55	55	55	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		2	4	4	4	4
VCC		10	46	46	40	40
VCC12		10	35	35	36	36
VCCAUX		10	36	36	32	32
VCCIO	Bank 1	3	18	18	10	10
	Bank 2	2	14	14	8	8
	Bank 3	2	15	15	10	10
	Bank 4	3	15	15	10	10
	Bank 5	3	15	15	10	10
	Bank 6	2	15	15	10	10
	Bank 7	2	16	16	8	8
VTT	Bank 2	0	2	2	2	2
	Bank 3	0	3	3	3	3
	Bank 4	0	3	3	3	3
	Bank 5	0	3	3	3	3
	Bank 6	0	3	3	3	3
	Bank 7	0	2	2	2	2
GND		26	177	177	134	134
NC		0	102	24	92	6
Single Ended User / Differential I/O per Bank	Bank 1	21/8	63/30	63/30	68/32	68/32
	Bank 2	15/7	26/13	30/15	34/17	54/27
	Bank 3	19/8	43/20	62/29	84/42	94/47
	Bank 4	25/11	50/22	66/32	84/41	99/48
	Bank 5	25/11	49/23	65/32	88/44	99/49
	Bank 6	19/8	43/20	62/29	84/42	94/47
	Bank 7	15/7	26/13	30/15	34/17	54/27
LVDS Output Pairs Per Bank	Bank 2	5	7	9	9	15
	Bank 3	6	15	21	21	24
	Bank 6	6	15	21	21	24
	Bank 7	5	7	9	9	15
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		28	60	60	108	108
Total		256	900	900	1020	1152

Pin Information Summary (Cont.)

Pin Type		1152 fcBGA			1704 fcBGA	
		LFSC/M40	LFSC/M80	LFSC/M115	LFSC/M80	LFSC/M115
Single Ended User I/O		604	660	660	904	942
Differential Pair User I/O		302	330	330	452	470
LVDS Output Pairs		78	102	102	114	132
Configuration	Dedicated	11	11	11	11	11
	Muxes/MPI sysBus	72	72	72	72	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		4	4	4	4	4
VCC		44	44	44	76	76
VCC12		52	52	52	88	88
VCCAUX		38	38	38	52	52
VCCIO	Bank 1	10	10	10	10	10
	Bank 2	9	9	9	12	12
	Bank 3	12	12	12	14	14
	Bank 4	12	12	12	14	14
	Bank 5	12	12	12	14	14
	Bank 6	12	12	12	14	14
	Bank 7	9	9	9	12	12
VTT	Bank 2	3	3	3	4	4
	Bank 3	3	3	3	4	4
	Bank 4	3	3	3	5	5
	Bank 5	3	3	3	5	5
	Bank 6	3	3	3	4	4
	Bank 7	3	3	3	4	4
GND		130	130	130	184	184
NC		62	6	6	52	14
Single Ended User / Differential I/O per Bank	Bank 1	80/40	80/40	80/40	80/40	80/40
	Bank 2	60/30	76/38	76/38	96/48	103/51
	Bank 3	96/48	108/54	108/54	132/66	144/72
	Bank 4	106/53	106/53	106/53	184/92	184/92
	Bank 5	106/53	106/53	106/53	184/92	184/92
	Bank 6	96/48	108/54	108/54	132/66	144/72
	Bank 7	60/30	76/38	76/38	96/48	103/51
LVDS Output Pairs Per Bank	Bank 2	15	21	21	24	27
	Bank 3	24	30	30	33	39
	Bank 6	24	30	30	33	39
	Bank 7	15	21	21	24	27
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		108	108	108	212	212
Total		1152	1152	1152	1704	1704

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2}

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F7	A_VDDAX25_L	-		A_VDDAX25_L	-	
B1	A_REFCLKP_L	-		A_REFCLKP_L	-	
C1	A_REFCLKN_L	-		A_REFCLKN_L	-	
D5	VCC12	-		VCC12	-	
A2	RESP_ULC	-		RESP_ULC	-	
E5	VCC12	-		VCC12	-	
D4	VCC12	-		VCC12	-	
H5	RESETN	1		RESETN	1	
H6	TSALLN	1		TSALLN	1	
G6	DONE	1		DONE	1	
G5	INITN	1		INITN	1	
F5	M0	1		M0	1	
F6	M1	1		M1	1	
F4	M2	1		M2	1	
E4	M3	1		M3	1	
D3	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
D2	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
J6	PL15C	7		PL16C	7	
J5	PL15D	7		PL16D	7	
E3	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
E2	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
K4	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
J4	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
F3	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
G3	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
K5	PL18C	7		PL18C	7	
K6	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F2	PL19A	7		PL22A	7	
F1	PL19B	7		PL22B	7	
E1	PL19C	7		PL22C	7	
D1	PL19D	7		PL22D	7	
K3	PL22A	7		PL25A	7	
L3	PL22B	7		PL25B	7	
L6	PL22C	7	VREF1_7	PL25C	7	VREF1_7
M6	PL22D	7	DIFFR_7	PL25D	7	DIFFR_7
J1	PL23A	7	PCLKT7_1	PL26A	7	PCLKT7_1
K1	PL23B	7	PCLKC7_1	PL26B	7	PCLKC7_1
L1	PL24A	7	PCLKT7_0	PL27A	7	PCLKT7_0
M1	PL24B	7	PCLKC7_0	PL27B	7	PCLKC7_0
P8	PL24C	7	PCLKT7_2	PL27C	7	PCLKT7_2
R8	PL24D	7	PCLKC7_2	PL27D	7	PCLKC7_2
N2	PL26A	6	PCLKT6_0	PL29A	6	PCLKT6_0
N1	PL26B	6	PCLKC6_0	PL29B	6	PCLKC6_0
R7	PL26C	6	PCLKT6_1	PL29C	6	PCLKT6_1
R6	PL26D	6	PCLKC6_1	PL29D	6	PCLKC6_1

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
U18	GND	-		GND	-	
U19	GND	-		GND	-	
U20	GND	-		GND	-	
V11	GND	-		GND	-	
V12	GND	-		GND	-	
V13	GND	-		GND	-	
V14	GND	-		GND	-	
V15	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V18	GND	-		GND	-	
V19	GND	-		GND	-	
V20	GND	-		GND	-	
W11	GND	-		GND	-	
W12	GND	-		GND	-	
W13	GND	-		GND	-	
W14	GND	-		GND	-	
W15	GND	-		GND	-	
W16	GND	-		GND	-	
W17	GND	-		GND	-	
W18	GND	-		GND	-	
W19	GND	-		GND	-	
W20	GND	-		GND	-	
Y11	GND	-		GND	-	
Y12	GND	-		GND	-	
Y13	GND	-		GND	-	
Y14	GND	-		GND	-	
Y15	GND	-		GND	-	
Y16	GND	-		GND	-	
Y17	GND	-		GND	-	
Y18	GND	-		GND	-	
Y19	GND	-		GND	-	
Y20	GND	-		GND	-	
H2	VCCIO7	-		VCCIO7	-	
N4	VCCIO7	-		VCCIO7	-	
N6	VCCIO7	-		VCCIO7	-	
J2	VCCIO7	-		VCCIO7	-	
L2	VCCIO7	-		VCCIO7	-	
H4	VCCIO7	-		VCCIO7	-	
AB2	VCCIO6	-		VCCIO6	-	
AD1	VCCIO6	-		VCCIO6	-	
W4	VCCIO6	-		VCCIO6	-	
AA4	VCCIO6	-		VCCIO6	-	
AE7	VCCIO5	-		VCCIO5	-	
AH6	VCCIO5	-		VCCIO5	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ31	PB9A	5		PB9A	5	
AH30	PB9B	5		PB9B	5	
AM30	PB11A	5		PB11A	5	
AM29	PB11B	5		PB11B	5	
AH29	PB11C	5		PB11C	5	
AH28	PB11D	5		PB11D	5	
AJ27	PB12A	5		PB13A	5	
AK27	PB12B	5		PB13B	5	
AE22	PB12C	5		PB13C	5	
AF23	PB12D	5		PB13D	5	
AL28	PB13A	5		PB15A	5	
AL27	PB13B	5		PB15B	5	
AC21	PB13C	5		PB15C	5	
AD21	PB13D	5		PB15D	5	
AM28	PB15A	5		PB17A	5	
AM27	PB15B	5		PB17B	5	
AG23	PB15C	5		PB17C	5	
AF22	PB15D	5		PB17D	5	
AG26	PB16A	5		PB19A	5	
AG25	PB16B	5		PB19B	5	
AL26	PB17A	5		PB22A	5	
AM26	PB17B	5		PB22B	5	
AJ24	PB19A	5		PB25A	5	
AK24	PB19B	5		PB25B	5	
AE21	PB19C	5		PB25C	5	
AE20	PB19D	5		PB25D	5	
AJ22	PB20A	5	PCLKT5_3	PB30A	5	PCLKT5_3
AK22	PB20B	5	PCLKC5_3	PB30B	5	PCLKC5_3
AG22	PB20C	5	PCLKT5_4	PB30C	5	PCLKT5_4
AH22	PB20D	5	PCLKC5_4	PB30D	5	PCLKC5_4
AL23	PB21A	5	PCLKT5_5	PB31A	5	PCLKT5_5
AL22	PB21B	5	PCLKC5_5	PB31B	5	PCLKC5_5
AH23	PB21C	5		PB31C	5	
AH24	PB21D	5		PB31D	5	
AJ21	PB23A	5	PCLKT5_0	PB33A	5	PCLKT5_0
AK21	PB23B	5	PCLKC5_0	PB33B	5	PCLKC5_0
AE19	PB23C	5		PB33C	5	
AF19	PB23D	5	VREF2_5	PB33D	5	VREF2_5
AM23	PB24A	5	PCLKT5_1	PB34A	5	PCLKT5_1
AM22	PB24B	5	PCLKC5_1	PB34B	5	PCLKC5_1
AH25	PB24C	5	PCLKT5_6	PB34C	5	PCLKT5_6
AH26	PB24D	5	PCLKC5_6	PB34D	5	PCLKC5_6
AL21	PB25A	5	PCLKT5_2	PB35A	5	PCLKT5_2
AL20	PB25B	5	PCLKC5_2	PB35B	5	PCLKC5_2
AG20	PB25C	5	PCLKT5_7	PB35C	5	PCLKT5_7
AG19	PB25D	5	PCLKC5_7	PB35D	5	PCLKC5_7
AJ19	PB28A	5		PB37A	5	
AK19	PB28B	5		PB37B	5	
AD18	PB28C	5		PB37C	5	
AE18	PB28D	5		PB37D	5	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ1	PB69A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AK1	PB69B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ2	PB69C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH3	PB69D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AH1	PROBE_VCC	-		PROBE_VCC	-	
AH2	PROBE_GND	-		PROBE_GND	-	
AD9	PR57D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AC10	PR57C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AG2	PR57B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AG1	PR57A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD8	PR56D	3		PR70D	3	
AC9	PR56C	3		PR70C	3	
AF2	PR56B	3		PR70B	3	
AF1	PR56A	3		PR70A	3	
AE6	PR55D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AE7	PR55C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AE1	PR55B	3		PR69B	3	
AE2	PR55A	3		PR69A	3	
AB8	PR53D	3		PR67D	3	
AC8	PR53C	3		PR67C	3	
AE4	PR53B	3		PR67B	3	
AE3	PR53A	3		PR67A	3	
AA10	PR52D	3		PR66D	3	
AA9	PR52C	3		PR66C	3	
AD1	PR52B	3		PR66B	3	
AC1	PR52A	3		PR66A	3	
AC7	PR51D	3	VREF2_3	PR65D	3	VREF2_3
AB7	PR51C	3		PR65C	3	
AD5	PR51B	3		PR65B	3	
AC5	PR51A	3		PR65A	3	
AE5	PR49D	3		PR62D	3	
AF5	PR49C	3		PR62C	3	
AD3	PR49B	3		PR62B	3	
AD4	PR49A	3		PR62A	3	
Y10	PR48D	3		PR61D	3	
Y9	PR48C	3		PR61C	3	
AC2	PR48B	3		PR61B	3	
AD2	PR48A	3		PR61A	3	
AC6	PR47D	3		PR60D	3	
AB6	PR47C	3		PR60C	3	
AA1	PR47B	3		PR60B	3	
AB1	PR47A	3		PR60A	3	
AA5	PR44D	3		PR53D	3	
AB5	PR44C	3		PR53C	3	
Y1	PR44B	3		PR53B	3	
W1	PR44A	3		PR53A	3	
W8	PR43D	3		PR52D	3	
Y7	PR43C	3		PR52C	3	
Y5	PR43B	3		PR52B	3	
W5	PR43A	3		PR52A	3	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AA7	VCCIO3	-		VCCIO3	-	
AB9	VCCIO3	-		VCCIO3	-	
AC4	VCCIO3	-		VCCIO3	-	
AD6	VCCIO3	-		VCCIO3	-	
AF3	VCCIO3	-		VCCIO3	-	
T3	VCCIO3	-		VCCIO3	-	
U4	VCCIO3	-		VCCIO3	-	
V6	VCCIO3	-		VCCIO3	-	
W10	VCCIO3	-		VCCIO3	-	
Y3	VCCIO3	-		VCCIO3	-	
AC11	VCCIO4	-		VCCIO4	-	
AD14	VCCIO4	-		VCCIO4	-	
AF15	VCCIO4	-		VCCIO4	-	
AF9	VCCIO4	-		VCCIO4	-	
AG12	VCCIO4	-		VCCIO4	-	
AJ13	VCCIO4	-		VCCIO4	-	
AJ7	VCCIO4	-		VCCIO4	-	
AK10	VCCIO4	-		VCCIO4	-	
AK16	VCCIO4	-		VCCIO4	-	
AK4	VCCIO4	-		VCCIO4	-	
AC19	VCCIO5	-		VCCIO5	-	
AD22	VCCIO5	-		VCCIO5	-	
AF21	VCCIO5	-		VCCIO5	-	
AG18	VCCIO5	-		VCCIO5	-	
AG24	VCCIO5	-		VCCIO5	-	
AJ17	VCCIO5	-		VCCIO5	-	
AJ23	VCCIO5	-		VCCIO5	-	
AJ30	VCCIO5	-		VCCIO5	-	
AK20	VCCIO5	-		VCCIO5	-	
AK26	VCCIO5	-		VCCIO5	-	
AA27	VCCIO6	-		VCCIO6	-	
AB23	VCCIO6	-		VCCIO6	-	
AC30	VCCIO6	-		VCCIO6	-	
AD26	VCCIO6	-		VCCIO6	-	
AF29	VCCIO6	-		VCCIO6	-	
T29	VCCIO6	-		VCCIO6	-	
U30	VCCIO6	-		VCCIO6	-	
V26	VCCIO6	-		VCCIO6	-	
W24	VCCIO6	-		VCCIO6	-	
Y29	VCCIO6	-		VCCIO6	-	
G30	VCCIO7	-		VCCIO7	-	
J27	VCCIO7	-		VCCIO7	-	
K29	VCCIO7	-		VCCIO7	-	
L24	VCCIO7	-		VCCIO7	-	
M26	VCCIO7	-		VCCIO7	-	
N30	VCCIO7	-		VCCIO7	-	
P23	VCCIO7	-		VCCIO7	-	
R27	VCCIO7	-		VCCIO7	-	
AA11	VCCAUX	-		VCCAUX	-	
AA12	VCCAUX	-		VCCAUX	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ9	PB78C	4		PB117C	4	
AJ8	PB78D	4		PB117D	4	
AP3	PB79A	4		PB119A	4	
AN3	PB79B	4		PB119B	4	
AF10	PB79C	4		PB119C	4	
AE10	PB79D	4		PB119D	4	
AL7	PB81A	4		PB121A	4	
AL6	PB81B	4		PB121B	4	
AK7	PB81C	4		PB121C	4	
AK6	PB81D	4		PB121D	4	
AN5	PB82A	4		PB123A	4	
AN4	PB82B	4		PB123B	4	
AH9	PB82C	4	VREF1_4	PB123C	4	VREF1_4
AH8	PB82D	4		PB123D	4	
AM3	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB124A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB124B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB83C	4		PB124C	4	
AG8	PB83D	4		PB124D	4	
AN2	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB125A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB125B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB125C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB125D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-		PROBE_VCC	-	
AF8	PROBE_GND	-		PROBE_GND	-	
AG7	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR95D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR95C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AL4	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR95B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR95A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR70D	3		PR94D	3	
AD9	PR70C	3		PR94C	3	
AH4	PR70B	3		PR94B	3	
AJ4	PR70A	3		PR94A	3	
AK5	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR93D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR93C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR69B	3		PR93B	3	
AL1	PR69A	3		PR93A	3	
AH5	PR67D	3		PR91D	3	
AG5	PR67C	3		PR91C	3	
AL2	PR67B	3		PR91B	3	
AK2	PR67A	3		PR91A	3	
AB9	PR66D	3		PR90D	3	
AC9	PR66C	3		PR90C	3	
AH1	PR66B	3		PR90B	3	
AG1	PR66A	3		PR90A	3	
AE8	PR65D	3	VREF2_3	PR89D	3	VREF2_3

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN8	PB123B	4	
AG11	PB123C	4	
AG10	PB123D	4	
AP7	PB125A	4	
AP6	PB125B	4	
AG13	PB125C	4	
AG12	PB125D	4	
AN7	PB127A	4	
AN6	PB127B	4	
AK9	PB127C	4	
AK8	PB127D	4	
AP5	PB129A	4	
AP4	PB129B	4	
AD11	PB129C	4	
AE11	PB129D	4	
AM7	PB131A	4	
AM6	PB131B	4	
AJ9	PB131C	4	
AJ8	PB131D	4	
AP3	PB133A	4	
AN3	PB133B	4	
AF10	PB133C	4	
AE10	PB133D	4	
AL7	PB135A	4	
AL6	PB135B	4	
AK7	PB135C	4	
AK6	PB135D	4	
AN5	PB138A	4	
AN4	PB138B	4	
AH9	PB138C	4	VREF1_4
AH8	PB138D	4	
AM3	PB139A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB139B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB139C	4	
AG8	PB139D	4	
AN2	PB141A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB141B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB141C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB141D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-	
AF8	PROBE_GND	-	
AG7	PR117D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR117C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL4	PR117B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR117A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR116D	3	
AD9	PR116C	3	
AH4	PR116B	3	
AJ4	PR116A	3	
AK5	PR115D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR115C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR115B	3	
AL1	PR115A	3	
AH5	PR112D	3	
AG5	PR112C	3	
AL2	PR112B	3	
AK2	PR112A	3	
AB9	PR109D	3	
AC9	PR109C	3	
AH1	PR109B	3	
AG1	PR109A	3	
AE8	PR107D	3	VREF2_3
AD8	PR107C	3	
AJ3	PR107B	3	
AH3	PR107A	3	
AD7	PR104D	3	
AC7	PR104C	3	
AJ2	PR104B	3	
AH2	PR104A	3	
AF6	PR103D	3	
AF5	PR103C	3	
AF4	PR103B	3	
AE4	PR103A	3	
AD6	PR99D	3	
AC6	PR99C	3	
AG2	PR99B	3	
AF2	PR99A	3	
AC8	PR98D	3	
AB8	PR98C	3	
AK1	PR98B	3	
AJ1	PR98A	3	
AB10	PR96D	3	
AA10	PR96C	3	
AF3	PR96B	3	
AE3	PR96A	3	
AE5	PR94D	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AD5	PR94C	3	
AE2	PR94B	3	
AD2	PR94A	3	
AC5	PR92D	3	
AB5	PR92C	3	
AF1	PR92B	3	
AE1	PR92A	3	
AA11	PR91D	3	
Y11	PR91C	3	
AC4	PR91B	3	
AB4	PR91A	3	
AA8	PR90D	3	DIFFR_3
AA9	PR90C	3	
AC3	PR90B	3	
AB3	PR90A	3	
AA7	PR79D	3	
Y7	PR79C	3	
AA2	PR79B	3	
Y2	PR79A	3	
AA6	PR77D	3	
Y6	PR77C	3	
Y4	PR77B	3	
W4	PR77A	3	
W11	PR74D	3	
V11	PR74C	3	
W2	PR74B	3	
V2	PR74A	3	
W9	PR71D	3	
V9	PR71C	3	
V1	PR71B	3	
U1	PR71A	3	
W10	PR70D	3	
V10	PR70C	3	
U2	PR70B	3	
T2	PR70A	3	
Y8	PR69D	3	
W8	PR69C	3	VREF1_3
W5	PR69B	3	
V5	PR69A	3	
V7	PR66D	3	PCLKC3_2
U7	PR66C	3	PCLKT3_2
T1	PR66B	3	
R1	PR66A	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL5	GND	-	
AM14	GND	-	
AM18	GND	-	
AM24	GND	-	
AM30	GND	-	
AM8	GND	-	
AN1	GND	-	
AN34	GND	-	
AP2	GND	-	
AP33	GND	-	
B1	GND	-	
B34	GND	-	
C11	GND	-	
C12	GND	-	
C13	GND	-	
C14	GND	-	
C17	GND	-	
C21	GND	-	
C22	GND	-	
C23	GND	-	
C24	GND	-	
C26	GND	-	
C27	GND	-	
C30	GND	-	
C31	GND	-	
C4	GND	-	
C5	GND	-	
C8	GND	-	
C9	GND	-	
D18	GND	-	
E32	GND	-	
E4	GND	-	
F19	GND	-	
G16	GND	-	
G29	GND	-	
G7	GND	-	
H3	GND	-	
H31	GND	-	
J10	GND	-	
J15	GND	-	
J26	GND	-	
K20	GND	-	
K23	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF40	PL76A	6		PL90A	6	
AG40	PL76B	6		PL90B	6	
AG36	PL76C	6		PL90C	6	
AH36	PL76D	6	DIFFR_6	PL90D	6	DIFFR_6
AF39	PL77A	6		PL91A	6	
AG39	PL77B	6		PL91B	6	
AF29	PL77C	6		PL91C	6	
AG29	PL77D	6		PL91D	6	
AH42	PL78A	6		PL92A	6	
AG42	PL78B	6		PL92B	6	
AG35	PL78C	6		PL92C	6	
AH35	PL78D	6		PL92D	6	
AG41	PL80A	6		PL94A	6	
AH41	PL80B	6		PL94B	6	
AG34	PL80C	6		PL94C	6	
AH34	PL80D	6		PL94D	6	
AJ42	PL81A	6		PL96A	6	
AK42	PL81B	6		PL96B	6	
AG33	PL81C	6		PL96C	6	
AH33	PL81D	6		PL96D	6	
AJ41	PL82A	6		PL98A	6	
AK41	PL82B	6		PL98B	6	
AJ37	PL82C	6		PL98C	6	
AK37	PL82D	6		PL98D	6	
AJ40	PL84A	6		PL99A	6	
AK40	PL84B	6		PL99B	6	
AJ34	PL84C	6		PL99C	6	
AK34	PL84D	6		PL99D	6	
AJ38	PL85A	6		PL103A	6	
AK38	PL85B	6		PL103B	6	
AH32	PL85C	6		PL103C	6	
AJ32	PL85D	6		PL103D	6	
AL42	PL86A	6		PL104A	6	
AM42	PL86B	6		PL104B	6	
AK36	PL86C	6		PL104C	6	
AL36	PL86D	6		PL104D	6	
AL38	PL89A	6		PL107A	6	
AM38	PL89B	6		PL107B	6	
AJ33	PL89C	6		PL107C	6	
AK33	PL89D	6	VREF2_6	PL107D	6	VREF2_6
AN42	PL90A	6		PL109A	6	
AP42	PL90B	6		PL109B	6	
AH31	PL90C	6		PL109C	6	
AJ31	PL90D	6		PL109D	6	
AN41	PL91A	6		PL112A	6	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).