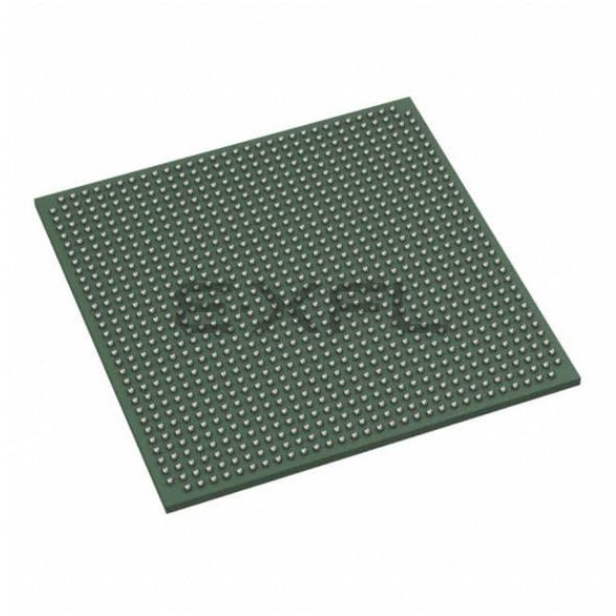
Lattice Semiconductor Corporation - LFSC3GA25E-5FFN1020I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	476
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga25e-5ffn1020i

Figure 2-3. Slice Diagram

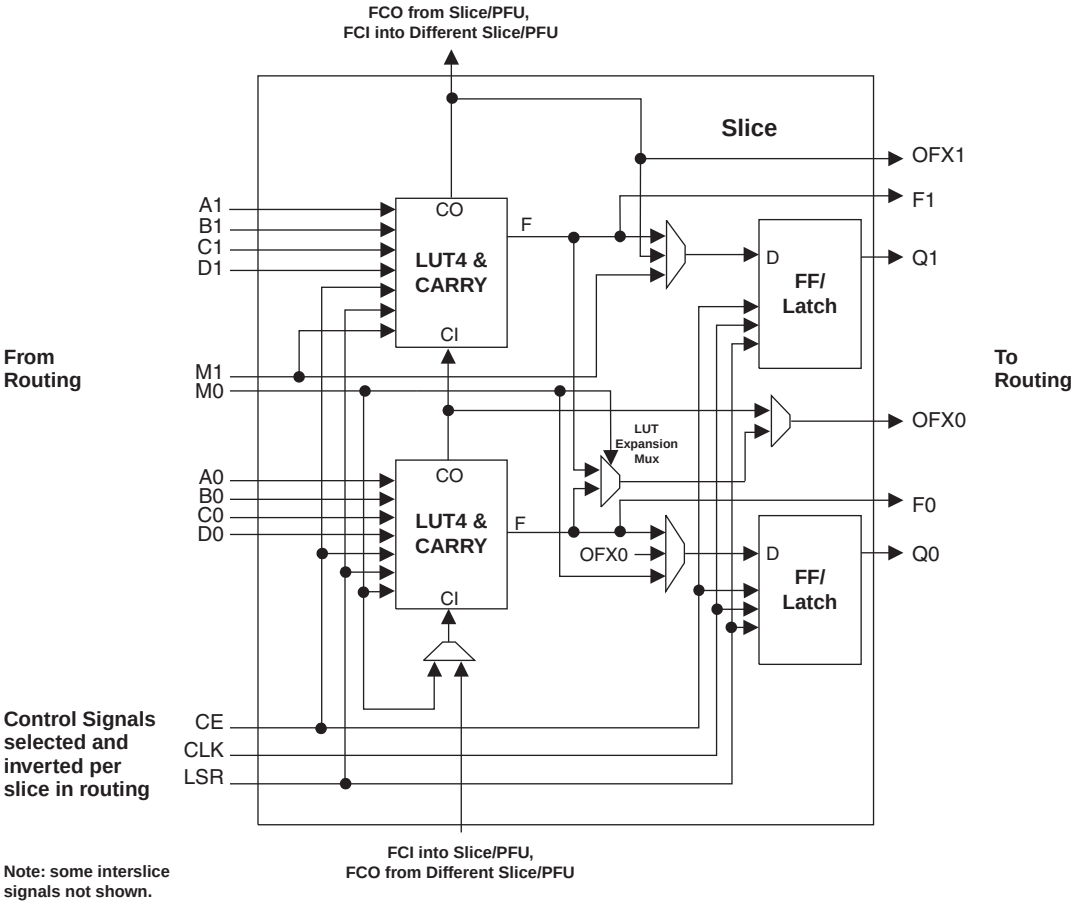


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[2]

1. See Figure 2-2 for connection details.
2. Requires two PFUs.

Figure 2-13. DLL to PLL

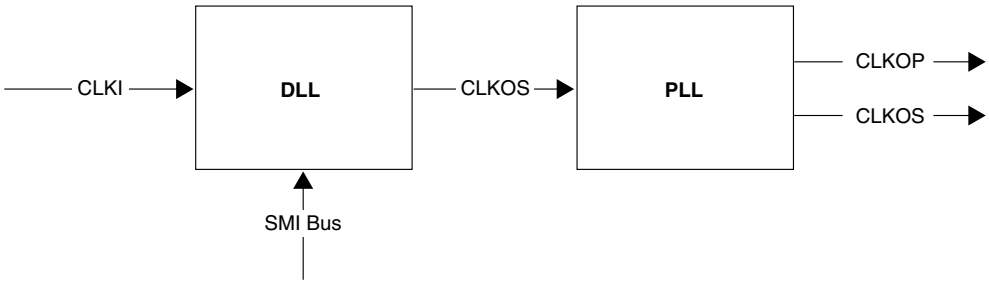


Figure 2-14 shows a shift of only CLKOP out in time.

Figure 2-14. PLL to DLL

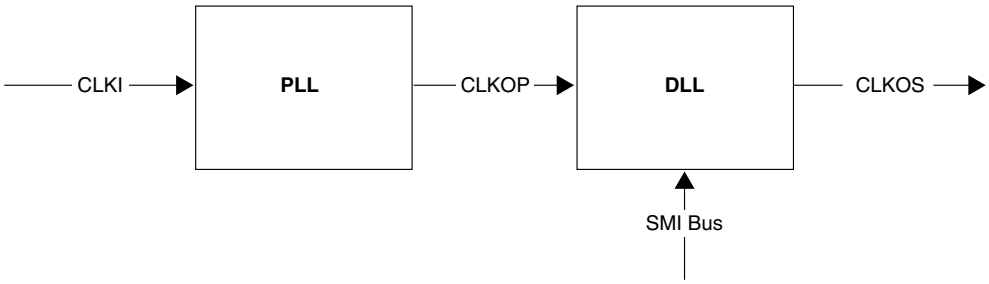
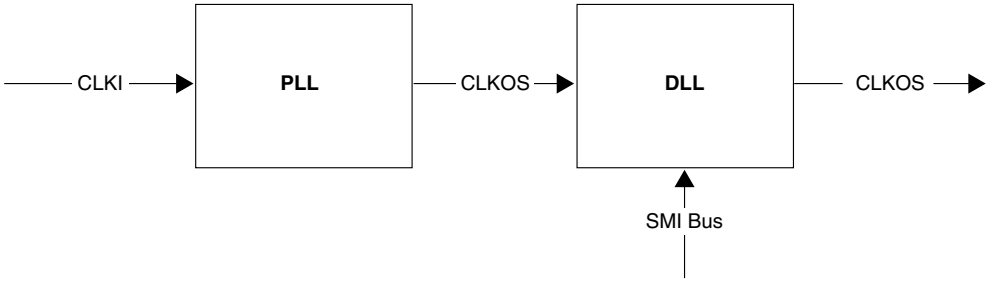


Figure 2-15 shows a shift of only CLKOS out in time.

Figure 2-15. PLL to DLL



For further information on the DLL, please see details of additional technical documentation at the end of this data sheet.

sysMEM Memory Block

The sysMEM block can implement single port, true dual port, pseudo dual port or FIFO memories. Dedicated FIFO support logic allows the LatticeSC devices to efficiently implement FIFOs without consuming LUTs or routing resources for flag generation. Each block can be used in a variety of depths and widths as shown in Table 2-5. Memory with ranges from x1 to x18 in all modes: single port, pseudo-dual port and FIFO also providing x36.

Power Supply Ramp Rates

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
t_{RAMP}	Power supply ramp rates for all power supplies	Over process, voltage, temperature	3.45	—	—	mV/µs
			—	—	75	ms

1. See the Power-up and Power-Down requirements section for more details on power sequencing.
2. From 0.5V to minimum operating voltage.

Hot Socketing Specifications[1]

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Programmable and dedicated Input or I/O leakage current[2, 3, 4, 5, 6]	0 <= V_{IN} <= V_{IH} (MAX)	—	—	±1500	µA
I_{HDIN}	SERDES average input current when device powered down and inputs driven[7]		—	—	4	mA

1. See Hot Socket power up/down information in Chapter 2 of this document.
2. Assumes monotonic rise/fall rates for all power supplies.
3. Sensitive to power supply sequencing as described in hot socketing section.
4. Assumes power supplies are between 0 and maximum recommended operations conditions.
5. IDK is additive to I_{PU}, I_{PD} or I_{BH}.
6. Represents DC conditions. For the first 20ns after hot insertion, current specification is 8 mA.
7. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed VDDOB of 1.575V, 8b/10b data and internal AC coupling.

DC Electrical Characteristics[5]

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.[3]	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low leakage	0 ≤ V_{IN} ≤ V_{IH} (MAX)	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0 ≤ V_{IN} ≤ 0.7 V_{CCIO}	-30	—	-210	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) ≤ V_{IN} ≤ V_{IH} (MAX)	30	—	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7V_{CCIO}	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ≤ V_{IN} ≤ V_{IH} (MAX)	—	—	210	µA
I_{BHLH}	Bus Hold High Overdrive Current	0 ≤ V_{IN} ≤ V_{IH} (MAX)	—	—	-210	µA
I_{CL}	PCI Low Clamp Current	-3 < V_{IN} ≤ -1	-25 + (V_{IN} + 1)/0.015	—	—	mA
I_{CH}	PCI High Clamp Current	V_{CC} + 4 > V_{IN} ≥ V_{CC} + 1	25 + (V_{IN} - V_{CC} -1)/ 0.015	—	—	mA
V_{BHT}	Bus Hold trip Points	0 ≤ V_{IN} ≤ V_{IH} (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{CCIP2} = 1.2V, V_{CCAUX} = 2.5, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C3[2]	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{CCIP2} = 1.2V, V_{CCAUX} = 2.5, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. I_{PU}, I_{PD}, I_{BHLS} and I_{BHHS} have minimum values of 15 or -15µA if V_{CCIO} is set to 1.2V nominal.
4. This table does not apply to SERDES pins.
5. For programmable I/Os.

BLVDS

The LatticeSC devices support BLVDS standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

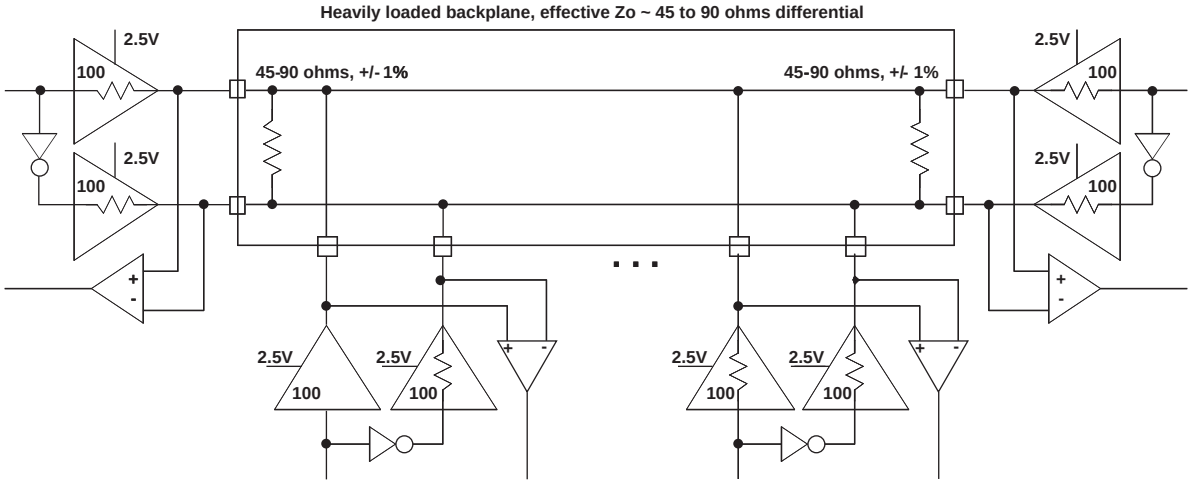


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	ohm
R_{TLEFT}	Left end termination	45	90	ohm
R_{TRIGHT}	Right end termination	45	90	ohm
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

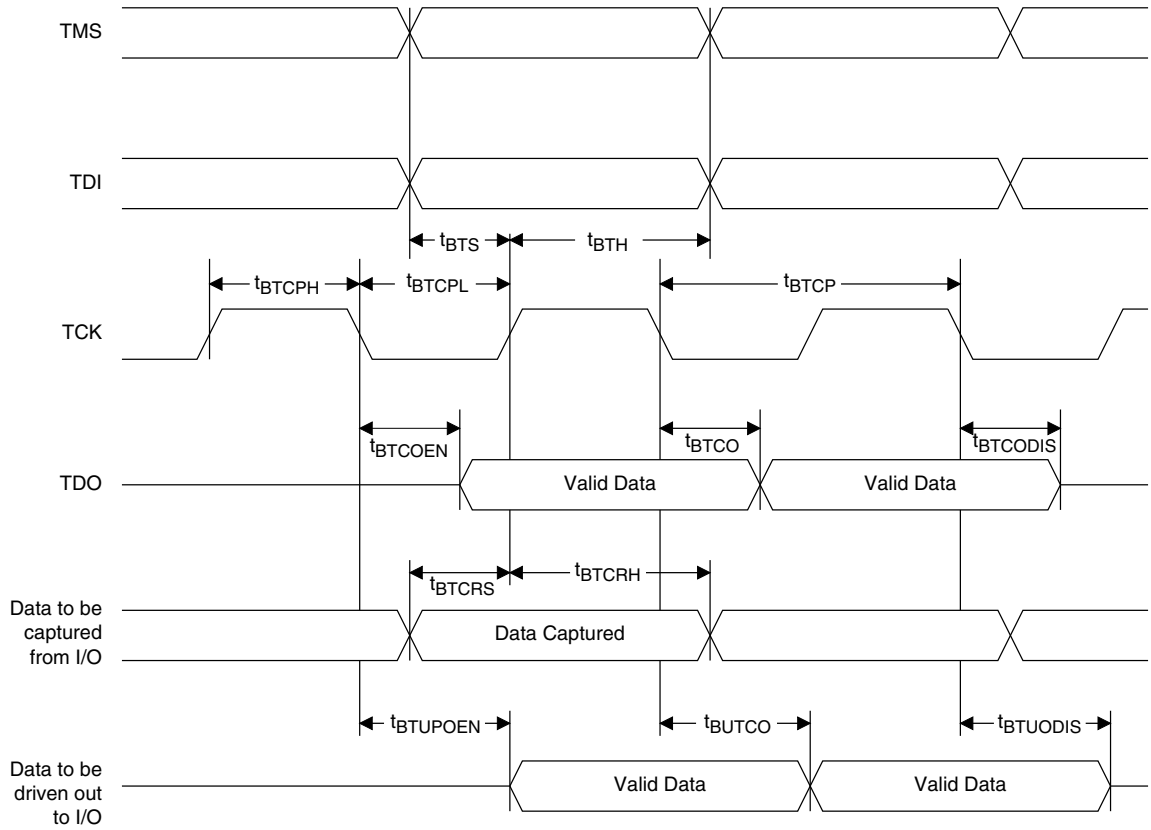
1. For input buffer, see LVDS table.

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	10	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	10	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	25	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	25	ns

Figure 3-14. JTAG Port Timing Waveforms



Signal Descriptions (Cont.)

Signal Name	I/O	Description
RESP_[ULC/URC]	—	Calibration resistor to be placed between this pin and either ground or RESPN_[ULC/URC]. RESPN_[ULC/URC] is available on select packages. If available, connection of calibration resistor between RESP_[ULC/URC] and RESPN_[ULC/URC] takes precedence over connection of calibration resistor between RESP_[ULC/URC] and ground. Note: only one per side of the device. Value: 4.02K ohm +/- 1% ohm.
RESPN_[ULC/URC]	—	Available on selected packages. If available, calibration resistor should be placed between RESP_[ULC/URC] and RESPN_[ULC/URC] instead of between RESP_[ULC/URC] and ground. Note: only one per side of the device. Value: 4.02K ohm +/- 1% ohm.
[A:D]_VDDIBx_[L/R]	—	Input buffer power supply for channel x (1.2V/1.5V) on left [L] or right [R] side of device.
[A:D]_VDDOBx_[L/R]	—	Output buffer power supply for channel x (1.2V/1.5V) on left [L] or right [R] side of device.
[A:D]_VDDAX25_[L/R]	—	Auxiliary power for input and output termination (2.5V) on left [L] or right [R] side of device.

1. The ispLEVER software tools may specify VDDRX, VDDTX, VDDP and VCCL pins. These pins should be considered VCC12 pins.
Note: Signals listed as Signal A / Signal B define the same physical pin that is used for different functions based on configuration mode.

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM21	PB29A	5		PB38A	5	
AM20	PB29B	5		PB38B	5	
AH21	PB29C	5		PB38C	5	
AH20	PB29D	5		PB38D	5	
AJ18	PB31A	5		PB39A	5	
AK18	PB31B	5		PB39B	5	
AH19	PB31C	5		PB39C	5	
AH18	PB31D	5		PB39D	5	
AL19	PB32A	5		PB41A	5	
AM19	PB32B	5		PB41B	5	
AH17	PB32C	5		PB41C	5	
AG17	PB32D	5		PB41D	5	
AL18	PB33A	5		PB42A	5	
AM18	PB33B	5		PB42B	5	
AC17	PB33C	5		PB42C	5	
AD17	PB33D	5		PB42D	5	
AL17	PB35A	5		PB43A	5	
AM17	PB35B	5		PB43B	5	
AE17	PB35C	5		PB43C	5	
AF17	PB35D	5		PB43D	5	
AM16	PB37A	4		PB45A	4	
AL16	PB37B	4		PB45B	4	
AF16	PB37C	4		PB45C	4	
AE16	PB37D	4		PB45D	4	
AM15	PB38A	4		PB46A	4	
AL15	PB38B	4		PB46B	4	
AD16	PB38C	4		PB46C	4	
AC16	PB38D	4		PB46D	4	
AM14	PB39A	4		PB47A	4	
AL14	PB39B	4		PB47B	4	
AG16	PB39C	4		PB47C	4	
AH16	PB39D	4		PB47D	4	
AK15	PB41A	4		PB49A	4	
AJ15	PB41B	4		PB49B	4	
AH15	PB41C	4		PB49C	4	
AH14	PB41D	4		PB49D	4	
AM13	PB42A	4		PB50A	4	
AM12	PB42B	4		PB50B	4	
AH13	PB42C	4		PB50C	4	
AH12	PB42D	4		PB50D	4	
AK14	PB43A	4		PB51A	4	
AJ14	PB43B	4		PB51B	4	
AE15	PB43C	4		PB51C	4	
AD15	PB43D	4		PB51D	4	
AL13	PB46A	4	PCLKT4_2	PB53A	4	PCLKT4_2
AL12	PB46B	4	PCLKC4_2	PB53B	4	PCLKC4_2
AG14	PB46C	4	PCLKT4_7	PB53C	4	PCLKT4_7
AG13	PB46D	4	PCLKC4_7	PB53D	4	PCLKC4_7
AM11	PB47A	4	PCLKT4_1	PB54A	4	PCLKT4_1
AM10	PB47B	4	PCLKC4_1	PB54B	4	PCLKC4_1

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y6	PR42D	3	DIFFR_3	PR51D	3	DIFFR_3
W6	PR42C	3		PR51C	3	
Y2	PR42B	3		PR51B	3	
W2	PR42A	3		PR51A	3	
W7	PR40D	3		PR49D	3	
V8	PR40C	3		PR49C	3	
W4	PR40B	3		PR49B	3	
W3	PR40A	3		PR49A	3	
V5	PR39D	3		PR48D	3	
U6	PR39C	3		PR48C	3	
V3	PR39B	3		PR48B	3	
V4	PR39A	3		PR48A	3	
V10	PR38D	3		PR47D	3	
V9	PR38C	3		PR47C	3	
V2	PR38B	3		PR47B	3	
V1	PR38A	3		PR47A	3	
U8	PR36D	3		PR45D	3	
U7	PR36C	3		PR45C	3	
U2	PR36B	3		PR45B	3	
U1	PR36A	3		PR45A	3	
U5	PR35D	3		PR44D	3	
T6	PR35C	3		PR44C	3	
T1	PR35B	3		PR44B	3	
T2	PR35A	3		PR44A	3	
U9	PR34D	3		PR43D	3	
U10	PR34C	3	VREF1_3	PR43C	3	VREF1_3
R1	PR34B	3		PR43B	3	
R2	PR34A	3		PR43A	3	
T7	PR31D	3	PCLKC3_2	PR40D	3	PCLKC3_2
T8	PR31C	3	PCLKT3_2	PR40C	3	PCLKT3_2
R4	PR31B	3		PR40B	3	
R3	PR31A	3		PR40A	3	
T5	PR30D	3	PCLKC3_3	PR39D	3	PCLKC3_3
R5	PR30C	3	PCLKT3_3	PR39C	3	PCLKT3_3
P2	PR30B	3		PR39B	3	
P1	PR30A	3		PR39A	3	
T9	PR29D	3	PCLKC3_1	PR38D	3	PCLKC3_1
T10	PR29C	3	PCLKT3_1	PR38C	3	PCLKT3_1
P4	PR29B	3	PCLKC3_0	PR38B	3	PCLKC3_0
P3	PR29A	3	PCLKT3_0	PR38A	3	PCLKT3_0
P5	PR27D	2	PCLKC2_2	PR36D	2	PCLKC2_2
P6	PR27C	2	PCLKT2_2	PR36C	2	PCLKT2_2
N1	PR27B	2	PCLKC2_0	PR36B	2	PCLKC2_0
N2	PR27A	2	PCLKT2_0	PR36A	2	PCLKT2_0
R9	PR26D	2	PCLKC2_3	PR35D	2	PCLKC2_3
R8	PR26C	2	PCLKT2_3	PR35C	2	PCLKT2_3
M1	PR26B	2	PCLKC2_1	PR35B	2	PCLKC2_1
L1	PR26A	2	PCLKT2_1	PR35A	2	PCLKT2_1
N9	PR25D	2	DIFFR_2	PR23D	2	DIFFR_2
M9	PR25C	2	VREF1_2	PR23C	2	VREF1_2

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AA7	VCCIO3	-		VCCIO3	-	
AB9	VCCIO3	-		VCCIO3	-	
AC4	VCCIO3	-		VCCIO3	-	
AD6	VCCIO3	-		VCCIO3	-	
AF3	VCCIO3	-		VCCIO3	-	
T3	VCCIO3	-		VCCIO3	-	
U4	VCCIO3	-		VCCIO3	-	
V6	VCCIO3	-		VCCIO3	-	
W10	VCCIO3	-		VCCIO3	-	
Y3	VCCIO3	-		VCCIO3	-	
AC11	VCCIO4	-		VCCIO4	-	
AD14	VCCIO4	-		VCCIO4	-	
AF15	VCCIO4	-		VCCIO4	-	
AF9	VCCIO4	-		VCCIO4	-	
AG12	VCCIO4	-		VCCIO4	-	
AJ13	VCCIO4	-		VCCIO4	-	
AJ7	VCCIO4	-		VCCIO4	-	
AK10	VCCIO4	-		VCCIO4	-	
AK16	VCCIO4	-		VCCIO4	-	
AK4	VCCIO4	-		VCCIO4	-	
AC19	VCCIO5	-		VCCIO5	-	
AD22	VCCIO5	-		VCCIO5	-	
AF21	VCCIO5	-		VCCIO5	-	
AG18	VCCIO5	-		VCCIO5	-	
AG24	VCCIO5	-		VCCIO5	-	
AJ17	VCCIO5	-		VCCIO5	-	
AJ23	VCCIO5	-		VCCIO5	-	
AJ30	VCCIO5	-		VCCIO5	-	
AK20	VCCIO5	-		VCCIO5	-	
AK26	VCCIO5	-		VCCIO5	-	
AA27	VCCIO6	-		VCCIO6	-	
AB23	VCCIO6	-		VCCIO6	-	
AC30	VCCIO6	-		VCCIO6	-	
AD26	VCCIO6	-		VCCIO6	-	
AF29	VCCIO6	-		VCCIO6	-	
T29	VCCIO6	-		VCCIO6	-	
U30	VCCIO6	-		VCCIO6	-	
V26	VCCIO6	-		VCCIO6	-	
W24	VCCIO6	-		VCCIO6	-	
Y29	VCCIO6	-		VCCIO6	-	
G30	VCCIO7	-		VCCIO7	-	
J27	VCCIO7	-		VCCIO7	-	
K29	VCCIO7	-		VCCIO7	-	
L24	VCCIO7	-		VCCIO7	-	
M26	VCCIO7	-		VCCIO7	-	
N30	VCCIO7	-		VCCIO7	-	
P23	VCCIO7	-		VCCIO7	-	
R27	VCCIO7	-		VCCIO7	-	
AA11	VCCAUX	-		VCCAUX	-	
AA12	VCCAUX	-		VCCAUX	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E24	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
F24	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
A23	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L25	VCC12	-		VCC12	-	
B23	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-		B_VDDOB1_L	-	
B24	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-		B_VDDOB0_L	-	
A24	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
K25	VCC12	-		VCC12	-	
F25	B_HDINN0_L	-	PCS 361 CH 0 IN N	B_HDINN0_L	-	PCS 361 CH 0 IN N
E25	B_HDINP0_L	-	PCS 361 CH 0 IN P	B_HDINP0_L	-	PCS 361 CH 0 IN P
D28	B_VDDIB0_L	-		B_VDDIB0_L	-	
G25	VCC12	-		VCC12	-	
D29	A_VDDIB3_L	-		A_VDDIB3_L	-	
C25	VCC12	-		VCC12	-	
A25	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
B25	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
E27	VCC12	-		VCC12	-	
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
F26	A_VDDOB3_L	-		A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
F27	A_VDDOB2_L	-		A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E28	VCC12	-		VCC12	-	
B28	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
A28	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
D30	A_VDDIB2_L	-		A_VDDIB2_L	-	
C28	VCC12	-		VCC12	-	
D31	A_VDDIB1_L	-		A_VDDIB1_L	-	
C29	VCC12	-		VCC12	-	
A29	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
B29	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A30	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
E29	VCC12	-		VCC12	-	
B30	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
F28	A_VDDOB1_L	-		A_VDDOB1_L	-	
B31	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
F29	A_VDDOB0_L	-		A_VDDOB0_L	-	
A31	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E30	VCC12	-		VCC12	-	
B32	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
A32	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
D32	A_VDDIB0_L	-		A_VDDIB0_L	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
N27	PL47C	7	
P27	PL47D	7	
K33	PL49A	7	
L33	PL49B	7	
M30	PL49C	7	
N30	PL49D	7	
M31	PL51A	7	
N31	PL51B	7	
P24	PL51C	7	
R24	PL51D	7	
M33	PL56A	7	
N33	PL56B	7	
U25	PL56C	7	
T25	PL56D	7	
L34	PL57A	7	
M34	PL57B	7	
P29	PL57C	7	
R29	PL57D	7	
N34	PL60A	7	
P34	PL60B	7	
R27	PL60C	7	
T27	PL60D	7	
R32	PL61A	7	PCLKT7_1
R31	PL61B	7	PCLKC7_1
U24	PL61C	7	PCLKT7_3
T24	PL61D	7	PCLKC7_3
P33	PL62A	7	PCLKT7_0
R33	PL62B	7	PCLKC7_0
T26	PL62C	7	PCLKT7_2
U26	PL62D	7	PCLKC7_2
T32	PL64A	6	PCLKT6_0
T31	PL64B	6	PCLKC6_0
U29	PL64C	6	PCLKT6_1
V29	PL64D	6	PCLKC6_1
T30	PL65A	6	
U30	PL65B	6	
U27	PL65C	6	PCLKT6_3
V27	PL65D	6	PCLKC6_3
R34	PL66A	6	
T34	PL66B	6	
U28	PL66C	6	PCLKT6_2
V28	PL66D	6	PCLKC6_2
V30	PL69A	6	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP20	PB61B	5	
AH21	PB61C	5	
AH20	PB61D	5	
AM20	PB63A	5	
AM19	PB63B	5	
AJ21	PB63C	5	
AJ20	PB63D	5	
AK19	PB66A	5	
AK18	PB66B	5	
AE18	PB66C	5	
AD18	PB66D	5	
AN19	PB69A	5	
AN18	PB69B	5	
AG18	PB69C	5	
AF18	PB69D	5	
AP19	PB71A	5	
AP18	PB71B	5	
AJ18	PB71C	5	
AH18	PB71D	5	
AP17	PB73A	4	
AP16	PB73B	4	
AJ17	PB73C	4	
AH17	PB73D	4	
AN17	PB75A	4	
AN16	PB75B	4	
AE17	PB75C	4	
AD17	PB75D	4	
AK17	PB78A	4	
AK16	PB78B	4	
AG17	PB78C	4	
AF17	PB78D	4	
AM16	PB81A	4	
AM15	PB81B	4	
AJ15	PB81C	4	
AJ14	PB81D	4	
AL16	PB83A	4	
AL15	PB83B	4	
AG16	PB83C	4	
AF16	PB83D	4	
AP15	PB86A	4	
AP14	PB86B	4	
AH15	PB86C	4	
AH14	PB86D	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN15	PB89A	4	PCLKT4_2
AN14	PB89B	4	PCLKC4_2
AE16	PB89C	4	PCLKT4_7
AD16	PB89D	4	PCLKC4_7
AK15	PB90A	4	PCLKT4_1
AK14	PB90B	4	PCLKC4_1
AG15	PB90C	4	PCLKT4_6
AG14	PB90D	4	PCLKC4_6
AM13	PB91A	4	PCLKT4_0
AM12	PB91B	4	PCLKC4_0
AJ12	PB91C	4	VREF2_4
AJ11	PB91D	4	
AL13	PB93A	4	PCLKT4_5
AL12	PB93B	4	PCLKC4_5
AH12	PB93C	4	
AH11	PB93D	4	
AN13	PB94A	4	PCLKT4_3
AN12	PB94B	4	PCLKC4_3
AD14	PB94C	4	PCLKT4_4
AD15	PB94D	4	PCLKC4_4
AP13	PB87A	4	
AP12	PB87B	4	
AK13	PB87C	4	
AK12	PB87D	4	
AP11	PB97A	4	
AP10	PB97B	4	
AN11	PB113A	4	
AN10	PB113B	4	
AF14	PB113C	4	
AF13	PB113D	4	
AM10	PB115A	4	
AM9	PB115B	4	
AE14	PB115C	4	
AE13	PB115D	4	
AP9	PB118A	4	
AP8	PB118B	4	
AK11	PB118C	4	
AK10	PB118D	4	
AL10	PB121A	4	
AL9	PB121B	4	
AF12	PB121C	4	
AF11	PB121D	4	
AN9	PB123A	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
K26	GND	-	
K28	GND	-	
K6	GND	-	
K9	GND	-	
L12	GND	-	
L32	GND	-	
L4	GND	-	
M10	GND	-	
M17	GND	-	
M24	GND	-	
N29	GND	-	
N7	GND	-	
P15	GND	-	
P20	GND	-	
P3	GND	-	
P31	GND	-	
R10	GND	-	
R14	GND	-	
R16	GND	-	
R19	GND	-	
R21	GND	-	
R26	GND	-	
T15	GND	-	
T17	GND	-	
T18	GND	-	
T20	GND	-	
T28	GND	-	
T6	GND	-	
U16	GND	-	
U19	GND	-	
U23	GND	-	
U32	GND	-	
U4	GND	-	
V12	GND	-	
V16	GND	-	
V19	GND	-	
V3	GND	-	
V31	GND	-	
W15	GND	-	
W17	GND	-	
W18	GND	-	
W20	GND	-	
W29	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BA19	PB73A	4		PB87A	4	
BA18	PB73B	4		PB87B	4	
AU19	PB73C	4		PB87C	4	
AU18	PB73D	4		PB87D	4	
AV19	PB74A	4	PCLKT4_2	PB89A	4	PCLKT4_2
AV18	PB74B	4	PCLKC4_2	PB89B	4	PCLKC4_2
AN19	PB74C	4	PCLKT4_7	PB89C	4	PCLKT4_7
AP19	PB74D	4	PCLKC4_7	PB89D	4	PCLKC4_7
BB17	PB75A	4	PCLKT4_1	PB90A	4	PCLKT4_1
BB16	PB75B	4	PCLKC4_1	PB90B	4	PCLKC4_1
AT19	PB75C	4	PCLKT4_6	PB90C	4	PCLKT4_6
AT18	PB75D	4	PCLKC4_6	PB90D	4	PCLKC4_6
BA17	PB77A	4	PCLKT4_0	PB91A	4	PCLKT4_0
BA16	PB77B	4	PCLKC4_0	PB91B	4	PCLKC4_0
AR19	PB77C	4	VREF2_4	PB91C	4	VREF2_4
AR18	PB77D	4		PB91D	4	
AY17	PB79A	4	PCLKT4_5	PB93A	4	PCLKT4_5
AY16	PB79B	4	PCLKC4_5	PB93B	4	PCLKC4_5
AN18	PB79C	4		PB93C	4	
AP18	PB79D	4		PB93D	4	
AW17	PB80A	4	PCLKT4_3	PB94A	4	PCLKT4_3
AW16	PB80B	4	PCLKC4_3	PB94B	4	PCLKC4_3
AU17	PB80C	4	PCLKT4_4	PB94C	4	PCLKT4_4
AU16	PB80D	4	PCLKC4_4	PB94D	4	PCLKC4_4
AV17	PB81A	4		PB95A	4	
AV16	PB81B	4		PB95B	4	
AL18	PB81C	4		PB95C	4	
AM18	PB81D	4		PB95D	4	
BB15	PB83A	4		PB97A	4	
BB14	PB83B	4		PB97B	4	
AP17	PB83C	4		PB97C	4	
AN17	PB83D	4		PB97D	4	
BA15	PB84A	4		PB98A	4	
BA14	PB84B	4		PB98B	4	
AT16	PB84C	4		PB98C	4	
AT15	PB84D	4		PB98D	4	
AV15	PB85A	4		PB99A	4	
AV14	PB85B	4		PB99B	4	
AR16	PB85C	4		PB99C	4	
AR15	PB85D	4		PB99D	4	
AY14	PB87A	4		PB101A	4	
AY13	PB87B	4		PB101B	4	
AU15	PB87C	4		PB101C	4	
AU14	PB87D	4		PB101D	4	
BB13	PB88A	4		PB102A	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F5	VCC12	-		VCC12	-	
B14	C_HDOUTP3_R	-	PCS 3E2 CH 3 OUT P	C_HDOUTP3_R	-	PCS 3E2 CH 3 OUT P
E13	C_HDINN3_R	-	PCS 3E2 CH 3 IN N	C_HDINN3_R	-	PCS 3E2 CH 3 IN N
D13	C_HDINP3_R	-	PCS 3E2 CH 3 IN P	C_HDINP3_R	-	PCS 3E2 CH 3 IN P
F12	VCC12	-		VCC12	-	
G14	C_VDDIB3_R	-		C_VDDIB3_R	-	
F11	VCC12	-		VCC12	-	
K15	C_REFCLKN_R	-		C_REFCLKN_R	-	
J15	C_REFCLKP_R	-		C_REFCLKP_R	-	
G15	VCC12	-		VCC12	-	
H16	D_VDDIB0_R	-		D_VDDIB0_R	-	
D14	D_HDINP0_R	-	PCS 3E3 CH 0 IN P	D_HDINP0_R	-	PCS 3E3 CH 0 IN P
E14	D_HDINN0_R	-	PCS 3E3 CH 0 IN N	D_HDINN0_R	-	PCS 3E3 CH 0 IN N
F6	VCC12	-		VCC12	-	
B15	D_HDOUTP0_R	-	PCS 3E3 CH 0 OUT P	D_HDOUTP0_R	-	PCS 3E3 CH 0 OUT P
M13	D_VDDOB0_R	-		D_VDDOB0_R	-	
A15	D_HDOUTN0_R	-	PCS 3E3 CH 0 OUT N	D_HDOUTN0_R	-	PCS 3E3 CH 0 OUT N
F8	D_VDDOB1_R	-		D_VDDOB1_R	-	
A16	D_HDOUTN1_R	-	PCS 3E3 CH 1 OUT N	D_HDOUTN1_R	-	PCS 3E3 CH 1 OUT N
F7	VCC12	-		VCC12	-	
B16	D_HDOUTP1_R	-	PCS 3E3 CH 1 OUT P	D_HDOUTP1_R	-	PCS 3E3 CH 1 OUT P
F15	D_HDINN1_R	-	PCS 3E3 CH 1 IN N	D_HDINN1_R	-	PCS 3E3 CH 1 IN N
E15	D_HDINP1_R	-	PCS 3E3 CH 1 IN P	D_HDINP1_R	-	PCS 3E3 CH 1 IN P
K17	VCC12	-		VCC12	-	
F13	D_VDDIB1_R	-		D_VDDIB1_R	-	
C14	VCC12	-		VCC12	-	
C15	D_VDDIB2_R	-		D_VDDIB2_R	-	
D16	D_HDINP2_R	-	PCS 3E3 CH 2 IN P	D_HDINP2_R	-	PCS 3E3 CH 2 IN P
E16	D_HDINN2_R	-	PCS 3E3 CH 2 IN N	D_HDINN2_R	-	PCS 3E3 CH 2 IN N
C11	VCC12	-		VCC12	-	
B17	D_HDOUTP2_R	-	PCS 3E3 CH 2 OUT P	D_HDOUTP2_R	-	PCS 3E3 CH 2 OUT P
C9	D_VDDOB2_R	-		D_VDDOB2_R	-	
A17	D_HDOUTN2_R	-	PCS 3E3 CH 2 OUT N	D_HDOUTN2_R	-	PCS 3E3 CH 2 OUT N
D17	D_VDDOB3_R	-		D_VDDOB3_R	-	
A18	D_HDOUTN3_R	-	PCS 3E3 CH 3 OUT N	D_HDOUTN3_R	-	PCS 3E3 CH 3 OUT N
C17	VCC12	-		VCC12	-	
B18	D_HDOUTP3_R	-	PCS 3E3 CH 3 OUT P	D_HDOUTP3_R	-	PCS 3E3 CH 3 OUT P
F17	D_HDINN3_R	-	PCS 3E3 CH 3 IN N	D_HDINN3_R	-	PCS 3E3 CH 3 IN N
E17	D_HDINP3_R	-	PCS 3E3 CH 3 IN P	D_HDINP3_R	-	PCS 3E3 CH 3 IN P
F14	VCC12	-		VCC12	-	
F16	D_VDDIB3_R	-		D_VDDIB3_R	-	
G16	VCC12	-		VCC12	-	
M17	D_REFCLKN_R	-		D_REFCLKN_R	-	
L17	D_REFCLKP_R	-		D_REFCLKP_R	-	
G18	PT77D	1	HDC/SI	PT93D	1	HDC/SI

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
T16	GND	-		GND	-	
T19	GND	-		GND	-	
T24	GND	-		GND	-	
T27	GND	-		GND	-	
T32	GND	-		GND	-	
U18	GND	-		GND	-	
U20	GND	-		GND	-	
U23	GND	-		GND	-	
U25	GND	-		GND	-	
U36	GND	-		GND	-	
U7	GND	-		GND	-	
G36	GND	-		GND	-	
G7	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V24	GND	-		GND	-	
V26	GND	-		GND	-	
V4	GND	-		GND	-	
V40	GND	-		GND	-	
W12	GND	-		GND	-	
W16	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W25	GND	-		GND	-	
W27	GND	-		GND	-	
W31	GND	-		GND	-	
Y17	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y22	GND	-		GND	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AA22	VCC	-		VCC	-	
AA24	VCC	-		VCC	-	
AA25	VCC	-		VCC	-	
AA26	VCC	-		VCC	-	
AB17	VCC	-		VCC	-	
AB18	VCC	-		VCC	-	
AB19	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
AB22	VCC	-		VCC	-	
AB24	VCC	-		VCC	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH27	VCCAUX	-		VCCAUX	-	
AH29	VCCAUX	-		VCCAUX	-	
AJ14	VCCAUX	-		VCCAUX	-	
AJ15	VCCAUX	-		VCCAUX	-	
AJ28	VCCAUX	-		VCCAUX	-	
AJ29	VCCAUX	-		VCCAUX	-	
P14	VCCAUX	-		VCCAUX	-	
P15	VCCAUX	-		VCCAUX	-	
P28	VCCAUX	-		VCCAUX	-	
P29	VCCAUX	-		VCCAUX	-	
R14	VCCAUX	-		VCCAUX	-	
R16	VCCAUX	-		VCCAUX	-	
R17	VCCAUX	-		VCCAUX	-	
R18	VCCAUX	-		VCCAUX	-	
R19	VCCAUX	-		VCCAUX	-	
R20	VCCAUX	-		VCCAUX	-	
R23	VCCAUX	-		VCCAUX	-	
R24	VCCAUX	-		VCCAUX	-	
R25	VCCAUX	-		VCCAUX	-	
R26	VCCAUX	-		VCCAUX	-	
R27	VCCAUX	-		VCCAUX	-	
R29	VCCAUX	-		VCCAUX	-	
T15	VCCAUX	-		VCCAUX	-	
T28	VCCAUX	-		VCCAUX	-	
U15	VCCAUX	-		VCCAUX	-	
U28	VCCAUX	-		VCCAUX	-	
V15	VCCAUX	-		VCCAUX	-	
V28	VCCAUX	-		VCCAUX	-	
W15	VCCAUX	-		VCCAUX	-	
W28	VCCAUX	-		VCCAUX	-	
Y15	VCCAUX	-		VCCAUX	-	
Y28	VCCAUX	-		VCCAUX	-	
F3	VCCIO1	-		VCCIO1	-	
F39	VCCIO1	-		VCCIO1	-	
G35	VCCIO1	-		VCCIO1	-	
G8	VCCIO1	-		VCCIO1	-	
L19	VCCIO1	-		VCCIO1	-	
L24	VCCIO1	-		VCCIO1	-	
M16	VCCIO1	-		VCCIO1	-	
M27	VCCIO1	-		VCCIO1	-	
N11	VCCIO1	-		VCCIO1	-	
N32	VCCIO1	-		VCCIO1	-	
AA4	VCCIO2	-		VCCIO2	-	
H7	VCCIO2	-		VCCIO2	-	
J4	VCCIO2	-		VCCIO2	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH22	VTT_5	5		VTT_5	5	
AJ22	VTT_5	5		VTT_5	5	
AJ23	VTT_5	5		VTT_5	5	
AJ24	VTT_5	5		VTT_5	5	
AJ25	VTT_5	5		VTT_5	5	
AB28	VTT_6	6		VTT_6	6	
AB29	VTT_6	6		VTT_6	6	
AE29	VTT_6	6		VTT_6	6	
AJ30	VTT_6	6		VTT_6	6	
AA28	VTT_7	7		VTT_7	7	
AA29	VTT_7	7		VTT_7	7	
R31	VTT_7	7		VTT_7	7	
V29	VTT_7	7		VTT_7	7	
Y24	GND	-		GND	-	
Y26	GND	-		GND	-	
Y8	GND	-		GND	-	
Y35	GND	-		GND	-	
AA16	VCC12	-		VCC12	-	
AA27	VCC12	-		VCC12	-	
AB16	VCC12	-		VCC12	-	
AB27	VCC12	-		VCC12	-	
AF16	VCC12	-		VCC12	-	
AF27	VCC12	-		VCC12	-	
AG17	VCC12	-		VCC12	-	
AG21	VCC12	-		VCC12	-	
G33	NC	-		NC	-	
G10	NC	-		NC	-	
M15	NC	-		NC	-	
L15	NC	-		NC	-	
K16	NC	-		NC	-	
J16	NC	-		NC	-	
M18	NC	-		NC	-	
L18	NC	-		NC	-	
M25	NC	-		NC	-	
L25	NC	-		NC	-	
J27	NC	-		NC	-	
K27	NC	-		NC	-	
L28	NC	-		NC	-	
M28	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M80 and LatticeSC/M115 in a 1704-pin package supports a 32-bit MPI interface.

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C[1]	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C[1]	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C[1]	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C[1]	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.