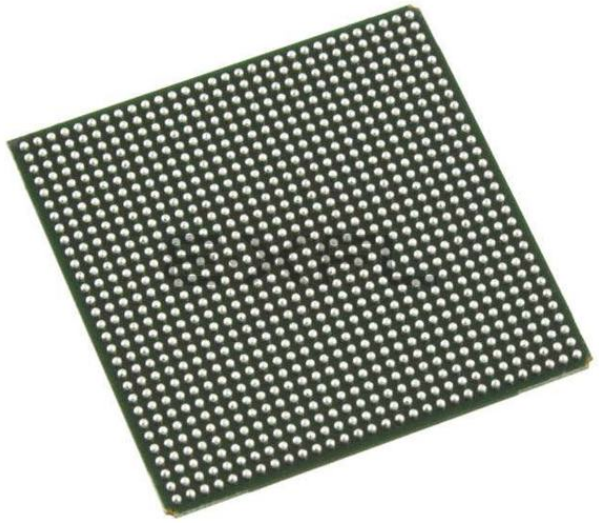
Lattice Semiconductor Corporation - LFSC3GA25E-5FN900C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	378
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga25e-5fn900c

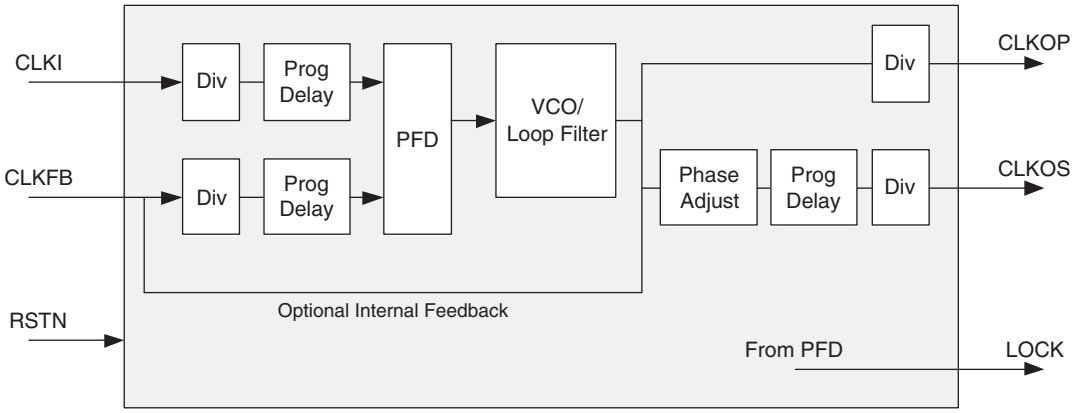
The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically.

The Phase Select block can modify the phase of the clock signal if desired. The Spread Spectrum block supports the modulation of the PLL output frequency. This reduces the peak energy in the fundamental and its harmonics providing for lower EMI (Electro Magnetic Interference).

The sysCLOCK PLL can be configured at power-up and then, if desired, reconfigured dynamically through the serial memory interface bus which connects with the on-chip system bus. For example, the user can select inputs, loop filters, divider setting, delay settings and phase shift settings. The user can also directly access the SMI bus through the routing.

The PLL clock input, from pin or routing, feeds into an input divider. There are four sources of feedback signal to the feedback divider: from the clock net, directly from the voltage controlled oscillator (VCO) output, from the routing or from an external pin. The signal from the input clock divider and the feedback divider are passed through the programmable delay before entering the phase frequency detector (PFD) unit. The output of this PFD is used to control the voltage controlled oscillator. There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

Figure 2-11. PLL Diagram



For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

Spread Spectrum Clocking (SSC)

The PLL supports spread spectrum clocking to reduce peak EMI by using “down-spread” modulation. The spread spectrum operation will vary the output frequency (at 30KHz to 500KHz) in a range that is between its nominal value, down to a frequency that is a programmable 1%, 2%, or 3% lower than normal.

Digital Locked Loop (DLLs)

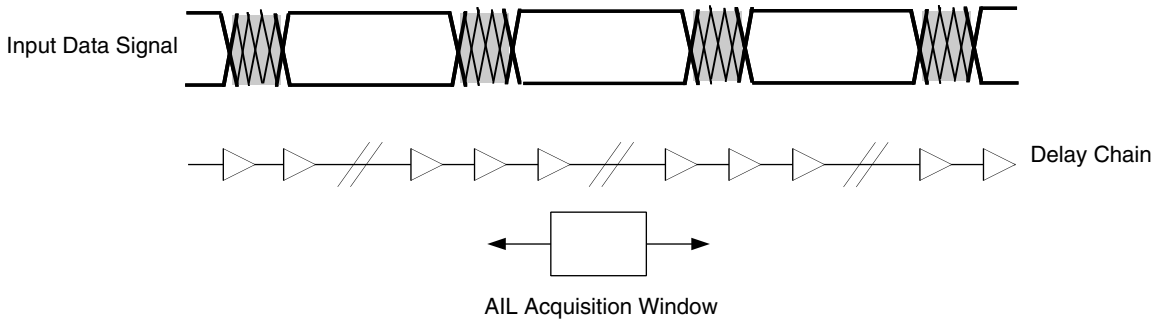
In addition to PLLs, the LatticeSC devices have up to 12 DLLs per device. DLLs assist in the management of clocks and strobes. DLLs are well suited to applications where the clock may be stopped or transferring jitter from input to output is important, for example forward clocked interfaces. PLLs are good for applications requiring the lowest output jitter or jitter filtering. All DLL outputs are routed as primary/edge clock sources.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. LOCK output signal is asserted when the DLL is locked. The ALU HOLD signal setting allows users to freeze the DLL at its current delay setting.

Adaptive Input Logic (AIL) Overview

The Adaptive Input Logic (AIL) provides the ability of the input logic to dynamically find a solution by monitoring multiple samples of the input data. The input data signal from the input buffer is run through a delay chain. Data, transitions, jitter, noise are all contained inside of the delay chain. The AIL will then search the delay chain for a clean sampling point for data. Once found the AIL will monitor and walk with the data dynamically. This novel approach of using a delay chain to create multiple copies of the data provides a lower power solution than oversampling data with a higher speed clock. Figure 2-19 provides a high level view of the AIL methodology.

Figure 2-19. LatticeSC AIL Delay of Input Data Waveform



The AIL slides the acquisition window through the delay chain searching for stable data based solely on data transitions. A specific training pattern is not required to perform this bit alignment, simply data transitions. The size of the acquisition window is user-selectable allowing the AIL to operate over the full range of the PURESPEED I/O range. Based on dynamic user control the AIL can either continuously adjust the window location based on data edge detection or it can be locked to a specific delay.

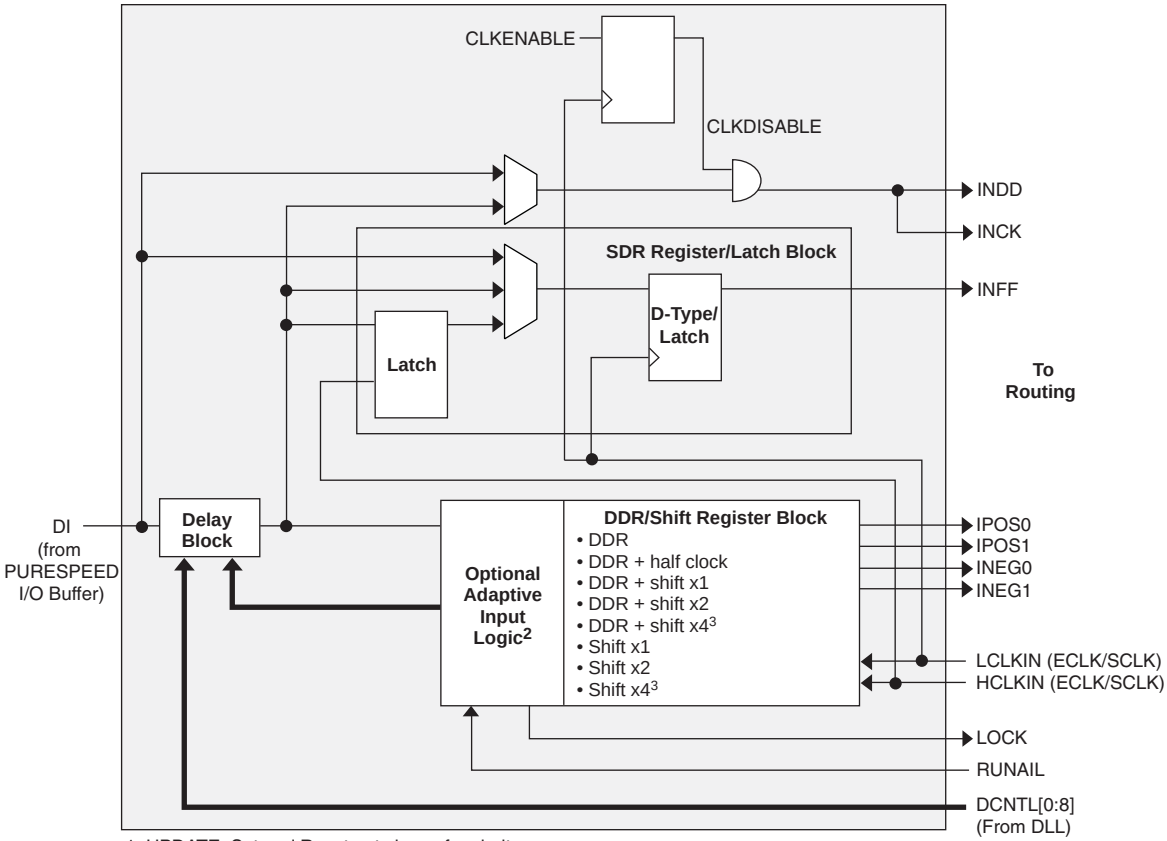
The AIL operates on single data and double data rate interfaces and is available on most FPGA input pins on the LatticeSC device and all buffer types. The AIL block is low power using only 0.003 mW/MHz typical (6 mW @ 2 Gbps) for PRBS 2^7 data. Multiple AIL inputs can be used to create a bus with a FPGA circuit to realign the bus to a common clock cycle. The FPGA circuit to realign the bus is required and is provided by Lattice as a reference design.

For more information on the LatticeSC AIL please refer to TN1158 LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide.

Input DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer to the low-speed clock domain. It functions as a gearbox allowing high-speed incoming data to be passed into the FPGA fabric. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. The PIOs A and C on the left, right and bottom of the device also contain an optional Adaptive Input Logic (AIL) element. This logic automatically aligns incoming data with the clock allowing for easy design of high-speed interfaces. Figure 2-21 shows a simplified block diagram of the shift register block. The shift block in conjunction with the update and clock divider blocks automatically handles the hand off between the low-speed and high-speed clock domains.

Figure 2-20. Input Register Block[1]



1. UPDATE, Set and Reset not shown for clarity
2. Adaptive input logic is only available in selected PIO
3. By four shift modes utilize DDR/shift register block from paired PIO.
4. CLKDISABLE is used to block the transitions on the DQS pin during post-amble. Its main use is to disable DQS (typically found in DDR memory interfaces) or other clock signals. It can also be used to disable any/all input signals to save power.

PURESPEED I/O Buffer Banks

LatticeSC devices have seven PURESPEED I/O buffer banks; each is capable of supporting multiple I/O standards. Each PURESPEED I/O bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-26 shows the seven banks and their associated supplies. Table 2-7 lists the maximum number of I/Os per bank for the whole LatticeSC family.

In the LatticeSC devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI33 and PCIX33) are powered using V_{CCIO}. In addition to the bank V_{CCIO} supplies, the LatticeSC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers. VCCAUX also powers a predriver of single-ended output buffers to enhance buffer performance.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeSC devices any I/O pin in a bank can be configured to be a dedicated reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Differential drivers have user selectable internal or external bias. External bias is brought in by the VREF1 pin in the bank. External bias for differential buffers is needed for applications that requires tighter than standard output common mode range.

Since a bank can have only one external bias circuit for differential drivers, LVDS and RSDS differential outputs can be mixed in a bank.

If a differential driver is configured in a bank, one pin in that bank becomes a DIFFR pin. This DIFFR pin must be connected to ground via an external 1K +/-1% ohm resistor. Note that differential drivers are not supported in banks 1, 4 and 5.

In addition, there are dedicated Terminating Supply (V_{TT}) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These V_{TT} pins are available in banks 2-7, these pins are not available in some packages. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.

There are further restrictions on the use of V_{TT} pins, for additional details refer to technical information at the end of this data sheet.

Initialization and Standby Supply Current

The table below indicates initialization and standby supply current while operating at 85°C junction temperature (T_J), which is the high end of the commercial temperature range, and 105°C, which is the high end of the industrial temperature range. This data assumes all outputs are tri-stated and all inputs are configured as LVCMOS and held at V_{CCIO} or GND. The remaining SERDES supply current for V_{DDIB} and V_{DDOB} is detailed in the SERDES section of this data sheet. For power at your design temperature, it is recommended to use the Power Calculator tool which is accessible in ispLEVER or can be used as a standalone tool. For more information on supply current, see the reference to additional technical documentation available at the end of this data sheet.

Over Recommended Operating Conditions

Symbol	Condition	Parameter	Device	25°C Typ.[1]	85°C Max.[2]		105°C Max.[2]	Units
				All	-5, -6	-7	-5, -6	
I_{CC}	(VCC = 1.2V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	65	449	678	755	mA
			LFSC/M25	113	798	1255	1343	mA
			LFSC/M40	159	1178	2006	1981	mA
			LFSC/M80	276	2122	3827	3569	mA
			LFSC/M115	454	3376	—	5679	mA
	(VCC = 1.0V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	45	312	471	524	mA
			LFSC/M25	79	554	872	933	mA
			LFSC/M40	110	818	1393	1375	mA
			LFSC/M80	191	1473	2658	2478	mA
			LFSC/M115	315	2344	—	3943	mA
I_{CC12}		1.2V Power Supply Current for Configuration Logic, FPGA PLL, SERDES PLL and SERDES Analog Supplies	LFSC/M15	23	39	59	35	mA
			LFSC/M25	25	50	78	56	mA
			LFSC/M40	31	78	133	89	mA
			LFSC/M80	50	108	195	123	mA
			LFSC/M115	65	131	—	154	mA
I_{CCAUX}		Auxiliary Operating Power Supply Current	LFSC/M15	7	12	19	14	mA
			LFSC/M25	9	16	25	18	mA
			LFSC/M40	12	23	39	25	mA
			LFSC/M80	13	25	45	23	mA
			LFSC/M115	16	27	—	26	mA
I_{CCIO} and I_{CCJ}		Bank Power Supply Current (per bank)	LFSC/M15	0.1	0.2	0.3	0.2	mA
			LFSC/M25	0.3	0.6	1.0	0.7	mA
			LFSC/M40	0.4	0.9	1.5	1.0	mA
			LFSC/M80	0.5	1.1	2.1	1.3	mA
			LFSC/M115	0.7	1.5	—	1.8	mA

1. I_{CC} is specified at T_J = 25°C and typical V_{CC}.
2. I_{CC} is specified at the respective commercial and industrial maximum T_J and V_{CC} limits.

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
GTLPLUS15	GTLPLUS15	-0.013	-0.017	0.012	0.004	0.037	0.024	ns
GTL12	GTL12	-0.063	-0.071	-0.007	-0.048	0.056	-0.032	ns
Output Adjusters								
LVDS	LVDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
RSDS	RSDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
BLVDS25	BLVDS	-0.129	0.05	-0.136	0.069	-0.136	0.083	ns
MLVDS25	MLVDS	-0.059	0.059	-0.057	0.096	-0.054	0.133	ns
LVPECL33	LVPECL	-0.334	-0.181	-0.325	-1.389	-0.315	-2.598	ns
HSTL18_I	HSTL_18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18_II	HSTL_18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL18D_I	Differential HSTL 18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18D_II	Differential HSTL 18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL15_I	HSTL_15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15_II	HSTL_15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
HSTL15D_I	Differential HSTL 15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15D_II	Differential HSTL 15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
SSTL33_I	SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33_II	SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL33D_I	Differential SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33D_II	Differential SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL25_I	SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25_II	SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL25D_I	Differential SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25D_II	Differential SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL18_I	SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18_II	SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
SSTL18D_I	Differential SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18D_II	Differential SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
LVTTL33_8mA	LVTTL 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVTTL33_16mA	LVTTL 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVTTL33_24mA	LVTTL 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVCMOS33_24mA	LVCMOS 3.3 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	-0.174	0.004	-0.195	0.002	-0.215	0	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	0	0	0	0	0	0	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.094	-0.025	0.107	0.096	0.12	0.216	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive	0.145	-0.054	0.162	0.063	0.181	0.179	ns
LVCMOS25_OD	LVCMOS 2.5 open drain	0.073	-0.125	0.081	-0.081	0.091	-0.09	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	-0.278	-0.099	-0.312	-0.115	-0.345	-0.131	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	-0.073	-0.078	-0.078	-0.084	-0.083	-0.089	ns

LatticeSC/M Internal Timing Parameters[1]

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Symbol	Description	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
PFU Logic Mode Timing									
t_{LUT4_PFU}	CTOF_DEL	LUT4 delay (A to D inputs to F output)	—	0.045	—	0.050	—	0.054	ns
t_{LUT5_PFU}	MTOOFX_DEL	LUT5 delay (inputs to output)	—	0.152	—	0.172	—	0.192	ns
t_{LSR_PFU}	LSR_DEL	Set/Reset to output (asynchronous)	—	0.378	—	0.426	—	0.474	ns
t_{SUM_PFU}	M_SET	Clock to Mux (M0,M1) input setup time	0.113	—	0.131	—	0.148	—	ns
t_{HM_PFU}	M_HLD	Clock to Mux (M0,M1) input hold time	-0.041	—	-0.046	—	-0.052	—	ns
t_{SUD_PFU}	DIN_SET	Clock to D input setup time	0.072	—	0.083	—	0.094	—	ns
t_{HD_PFU}	DIN_HLD	Clock to D input hold time	-0.028	—	-0.032	—	-0.035	—	ns
t_{CK2Q_PFU}	REG_DEL	Clock to Q delay, D-type register configuration	—	0.224	—	0.252	—	0.279	ns
t_{LE2Q_PFU}	LTCH_DEL	Clock to Q delay latch configuration	—	0.294	—	0.331	—	0.367	ns
t_{LD2Q_PFU}	TLTCH_DEL	D to Q throughput delay when latch is enabled	—	0.300	—	0.338	—	0.376	ns
PFU Memory Mode Timing									
t_{CORAM_PFU}	CLKTOF_DEL	Clock to Output	—	0.575	—	0.649	—	0.724	ns
t_{SUDATA_PFU}	DIN_SET	Data Setup Time	-0.024	—	-0.026	—	-0.027	—	ns
t_{HDATA_PFU}	DIN_HLD	Data Hold Time	0.075	—	0.084	—	0.094	—	ns
t_{SUADDR_PFU}	WAD_SET	Address Setup Time	-0.176	—	-0.196	—	-0.215	—	ns
t_{HADDR_PFU}	WAD_HLD	Address Hold Time	0.110	—	0.124	—	0.138	—	ns
t_{SUWREN_PFU}	WE_SET	Write/Read Enable Setup Time	0.014	—	0.019	—	0.024	—	ns
t_{HWREN_PFU}	WE_HLD	Write/Read Enable Hold Time	0.078	—	0.086	—	0.094	—	ns
PIC Timing									
PIO Input/Output Buffer Timing									
t_{IN_PIO}	IN_DEL	Input Buffer Delay(LVCMOS25)	—	0.578	—	0.661	—	0.744	ns
t_{OUT_PIO}	DOPADI_DEL	Output Buffer Delay(LVCMOS25)	—	2.712	—	3.027	—	3.395	ns
t_{SUI_PIO}	DIN_SET	Input Register Setup Time (Data Before Clock)	0.277	—	0.312	—	0.348	—	ns
t_{HI_PIO}	DIN_HLD	Input Register Hold Time (Data after Clock)	-0.267	—	-0.306	—	-0.345	—	ns
t_{COO_PIO}	CK_DEL	Output Register Clock to Output Delay	—	0.513	—	0.571	—	0.639	ns
t_{SUCE_PIO}	CE_SET	Input Register Clock Enable Setup Time	—	0.000	—	0.000	—	0.000	ns
t_{HCE_PIO}	CE_HLD	Input Register Clock Enable Hold Time	—	0.129	—	0.145	—	0.161	ns
t_{SULSR_PIO}	LSR_SET	Set/Reset Setup Time	0.057	—	0.060	—	0.063	—	ns
t_{HLSR_PIO}	LSR_HLD	Set/Reset Hold Time	-0.151	—	-0.159	—	-0.169	—	ns
t_{LE2Q_PIO}	CK_DEL	Input Register Clock to Q delay latch configuration	—	0.335	—	0.372	—	0.410	ns
t_{LD2Q_PIO}	DIN_DEL	Input Register D to Q throughput delay when latch is enabled	—	0.578	—	0.647	—	0.717	ns

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		2	—	1000	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		1.5625	—	1000	MHz
f_{VCO}	PLL VCO Frequency		100	—	1000	MHz
f_{PFD}	Phase Detector Input Frequency		2	—	700	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected (at 50% levels)	45	—	55	%
t_{OPJIT}[1]	Output Clock Period Jitter	2 MHz ≤ f_{PFD} ≤ 10 MHz	—	—	200	ps
		f_{PFD} > 10 MHz	—	—	100	ps
t_{CPJIT}[1]	Output Clock Cycle-to-Cycle Jitter		—	—	100	ps
t_{SKEW}	Output Clock-to-Clock Skew (Between Two Outputs with the Same Phase Setting)		—	—	20	ps
t_{LOCK}	PLL Lock-in Time		—	—	1	ms
t_{IPJIT}	Input Clock Period Jitter		—	—	±250	ps
t_{HI}	Input Clock High Time	At 80% level	350	—	—	ps
t_{LO}	Input Clock Low Time	At 20% level	350	—	—	ps
t_{RSWA}	Analog Reset Signal Pulse Width		100	—	—	ns
t_{RSWD}	Digital Reset Signal Pulse Width		3	—	—	ns
t_{DEL}	Timeshift Delay Step Size		40	80	120	ps
t_{RANGE}	Timeshift Delay Range		—	+/- 560	—	ps
f_{SS}	Spread Spectrum Modulation Frequency		30	—	500	KHz
% Spread	Percentage Downspread for SS Mode		0.5	—	1.5	%
	VCO Clock Phase Adjustment Accuracy		-5	—	5	°

1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps

Pin Information Summary (Cont.)

Pin Type		1152 fcBGA			1704 fcBGA	
		LFSC/M40	LFSC/M80	LFSC/M115	LFSC/M80	LFSC/M115
Single Ended User I/O		604	660	660	904	942
Differential Pair User I/O		302	330	330	452	470
LVDS Output Pairs		78	102	102	114	132
Configuration	Dedicated	11	11	11	11	11
	Muxes/MPI sysBus	72	72	72	72	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		4	4	4	4	4
VCC		44	44	44	76	76
VCC12		52	52	52	88	88
VCCAUX		38	38	38	52	52
VCCIO	Bank 1	10	10	10	10	10
	Bank 2	9	9	9	12	12
	Bank 3	12	12	12	14	14
	Bank 4	12	12	12	14	14
	Bank 5	12	12	12	14	14
	Bank 6	12	12	12	14	14
	Bank 7	9	9	9	12	12
VTT	Bank 2	3	3	3	4	4
	Bank 3	3	3	3	4	4
	Bank 4	3	3	3	5	5
	Bank 5	3	3	3	5	5
	Bank 6	3	3	3	4	4
	Bank 7	3	3	3	4	4
GND		130	130	130	184	184
NC		62	6	6	52	14
Single Ended User / Differential I/O per Bank	Bank 1	80/40	80/40	80/40	80/40	80/40
	Bank 2	60/30	76/38	76/38	96/48	103/51
	Bank 3	96/48	108/54	108/54	132/66	144/72
	Bank 4	106/53	106/53	106/53	184/92	184/92
	Bank 5	106/53	106/53	106/53	184/92	184/92
	Bank 6	96/48	108/54	108/54	132/66	144/72
	Bank 7	60/30	76/38	76/38	96/48	103/51
LVDS Output Pairs Per Bank	Bank 2	15	21	21	24	27
	Bank 3	24	30	30	33	39
	Bank 6	24	30	30	33	39
	Bank 7	15	21	21	24	27
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		108	108	108	212	212
Total		1152	1152	1152	1704	1704

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2]

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
E4	A_VDDAX25_L	-	
B1	A_REFCLKP_L	-	
C1	A_REFCLKN_L	-	
D2	RESP_ULC	-	
F5	RESETN	1	
D1	DONE	1	
E1	INITN	1	
E2	M0	1	
E3	M1	1	
E5	M2	1	
E6	M3	1	
F2	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
F1	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
F3	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G1	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
G4	PL18D	7	VREF2_7
H3	PL22A	7	
H2	PL22B	7	
H5	PL22C	7	VREF1_7
G5	PL22D	7	DIFFR_7
H1	PL23A	7	PCLKT7_1
J1	PL23B	7	PCLKC7_1
J2	PL24A	7	PCLKT7_0
J3	PL24B	7	PCLKC7_0
H4	PL24C	7	PCLKT7_2
H6	PL24D	7	PCLKC7_2
J4	PL26A	6	PCLKT6_0
K5	PL26B	6	PCLKC6_0
J5	PL26C	6	PCLKT6_1
J6	PL26D	6	PCLKC6_1
K1	PL28A	6	
L1	PL28B	6	
L4	PL28C	6	PCLKT6_2
K4	PL28D	6	PCLKC6_2
L2	PL31C	6	VREF1_6
L3	PL35A	6	
M3	PL35B	6	
M2	PL35D	6	DIFFR_6
M1	PL37A	6	
N1	PL37B	6	
P2	PL41D	6	VREF2_6
M5	PL43A	6	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB57D	4		PB79D	4	
AN13	PB58A	4	PCLKT4_3	PB80A	4	PCLKT4_3
AN12	PB58B	4	PCLKC4_3	PB80B	4	PCLKC4_3
AD14	PB58C	4	PCLKT4_4	PB80C	4	PCLKT4_4
AD15	PB58D	4	PCLKC4_4	PB80D	4	PCLKC4_4
AP13	PB61A	4		PB73A	4	
AP12	PB61B	4		PB73B	4	
AK13	PB61C	4		PB73C	4	
AK12	PB61D	4		PB73D	4	
AP11	PB62A	4		PB83A	4	
AP10	PB62B	4		PB83B	4	
AN11	PB63A	4		PB99A	4	
AN10	PB63B	4		PB99B	4	
AF14	PB63C	4		PB99C	4	
AF13	PB63D	4		PB99D	4	
AM10	PB67A	4		PB101A	4	
AM9	PB67B	4		PB101B	4	
AE14	PB67C	4		PB101C	4	
AE13	PB67D	4		PB101D	4	
AP9	PB69A	4		PB104A	4	
AP8	PB69B	4		PB104B	4	
AK11	PB69C	4		PB104C	4	
AK10	PB69D	4		PB104D	4	
AL10	PB70A	4		PB107A	4	
AL9	PB70B	4		PB107B	4	
AF12	PB70C	4		PB107C	4	
AF11	PB70D	4		PB107D	4	
AN9	PB73A	4		PB109A	4	
AN8	PB73B	4		PB109B	4	
AG11	PB73C	4		PB109C	4	
AG10	PB73D	4		PB109D	4	
AP7	PB74A	4		PB111A	4	
AP6	PB74B	4		PB111B	4	
AG13	PB74C	4		PB111C	4	
AG12	PB74D	4		PB111D	4	
AN7	PB75A	4		PB113A	4	
AN6	PB75B	4		PB113B	4	
AK9	PB75C	4		PB113C	4	
AK8	PB75D	4		PB113D	4	
AP5	PB77A	4		PB115A	4	
AP4	PB77B	4		PB115B	4	
AD11	PB77C	4		PB115C	4	
AE11	PB77D	4		PB115D	4	
AM7	PB78A	4		PB117A	4	
AM6	PB78B	4		PB117B	4	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W13	VCCAUX	-		VCCAUX	-	
W22	VCCAUX	-		VCCAUX	-	
Y21	GND	-		GND	-	
Y25	GND	-		GND	-	
C18	VCCIO1	-		VCCIO1	-	
D17	VCCIO1	-		VCCIO1	-	
F16	VCCIO1	-		VCCIO1	-	
G19	VCCIO1	-		VCCIO1	-	
J20	VCCIO1	-		VCCIO1	-	
K12	VCCIO1	-		VCCIO1	-	
K15	VCCIO1	-		VCCIO1	-	
L23	VCCIO1	-		VCCIO1	-	
Y9	GND	-		GND	-	
J9	VCCIO1	-		VCCIO1	-	
E3	VCCIO2	-		VCCIO2	-	
G6	VCCIO2	-		VCCIO2	-	
H4	VCCIO2	-		VCCIO2	-	
K7	VCCIO2	-		VCCIO2	-	
L3	VCCIO2	-		VCCIO2	-	
M11	VCCIO2	-		VCCIO2	-	
N6	VCCIO2	-		VCCIO2	-	
P4	VCCIO2	-		VCCIO2	-	
R9	VCCIO2	-		VCCIO2	-	
AA3	VCCIO3	-		VCCIO3	-	
AB7	VCCIO3	-		VCCIO3	-	
AC10	VCCIO3	-		VCCIO3	-	
AD4	VCCIO3	-		VCCIO3	-	
AE6	VCCIO3	-		VCCIO3	-	
AG3	VCCIO3	-		VCCIO3	-	
AK4	VCCIO3	-		VCCIO3	-	
T7	VCCIO3	-		VCCIO3	-	
U3	VCCIO3	-		VCCIO3	-	
V4	VCCIO3	-		VCCIO3	-	
W6	VCCIO3	-		VCCIO3	-	
Y10	VCCIO3	-		VCCIO3	-	
AD12	VCCIO4	-		VCCIO4	-	
AF15	VCCIO4	-		VCCIO4	-	
AF9	VCCIO4	-		VCCIO4	-	
AH10	VCCIO4	-		VCCIO4	-	
AH16	VCCIO4	-		VCCIO4	-	
AJ13	VCCIO4	-		VCCIO4	-	
AJ7	VCCIO4	-		VCCIO4	-	
AL14	VCCIO4	-		VCCIO4	-	
AL8	VCCIO4	-		VCCIO4	-	
AM11	VCCIO4	-		VCCIO4	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
N27	PL47C	7	
P27	PL47D	7	
K33	PL49A	7	
L33	PL49B	7	
M30	PL49C	7	
N30	PL49D	7	
M31	PL51A	7	
N31	PL51B	7	
P24	PL51C	7	
R24	PL51D	7	
M33	PL56A	7	
N33	PL56B	7	
U25	PL56C	7	
T25	PL56D	7	
L34	PL57A	7	
M34	PL57B	7	
P29	PL57C	7	
R29	PL57D	7	
N34	PL60A	7	
P34	PL60B	7	
R27	PL60C	7	
T27	PL60D	7	
R32	PL61A	7	PCLKT7_1
R31	PL61B	7	PCLKC7_1
U24	PL61C	7	PCLKT7_3
T24	PL61D	7	PCLKC7_3
P33	PL62A	7	PCLKT7_0
R33	PL62B	7	PCLKC7_0
T26	PL62C	7	PCLKT7_2
U26	PL62D	7	PCLKC7_2
T32	PL64A	6	PCLKT6_0
T31	PL64B	6	PCLKC6_0
U29	PL64C	6	PCLKT6_1
V29	PL64D	6	PCLKC6_1
T30	PL65A	6	
U30	PL65B	6	
U27	PL65C	6	PCLKT6_3
V27	PL65D	6	PCLKC6_3
R34	PL66A	6	
T34	PL66B	6	
U28	PL66C	6	PCLKT6_2
V28	PL66D	6	PCLKC6_2
V30	PL69A	6	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J3	PR45A	2	
M8	PR43D	2	DIFFR_2
L8	PR43C	2	VREF1_2
K4	PR43B	2	
J4	PR43A	2	
M7	PR26D	2	
L7	PR26C	2	
J5	PR26B	2	
H5	PR26A	2	
N9	PR19D	2	
P9	PR19C	2	
G3	PR19B	2	
F3	PR19A	2	
J6	PR18D	2	VREF2_2
H6	PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
D2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
G4	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
F4	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
J7	PR15D	2	
H7	PR15C	2	
G5	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
F5	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
C2	VCCJ	-	
M9	TDO	-	TDO
L9	TMS	-	
D1	TCK	-	
C1	TDI	-	
J8	PROGRAMN	1	
K8	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
B2	CCLK	1	
H9	RESP_URC	-	
H10	VCC12	-	
H8	A_REFCLKN_R	-	
G8	A_REFCLKP_R	-	
C3	VCC12	-	
D3	A_VDDIB0_R	-	
A3	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B3	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E5	VCC12	-	
A4	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J17	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT81B	1	MCA_CLK_P1_OUT
E16	PT81A	1	MCA_CLK_P1_IN
H15	PT78D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT78C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT78B	1	MCA_CLK_P2_OUT
C16	PT78A	1	MCA_CLK_P2_IN
L17	PT75D	1	MCA_DONE_OUT
K17	PT75C	1	BUSYN/RCLK/SCK
E17	PT75B	1	DP0/MPI_PAR0
F17	PT75A	1	MPI_TA
G17	PT73D	1	D23/MPI_DATA23
H17	PT73C	1	DP2/MPI_PAR2
A17	PT73B	1	PCLKC1_0
B17	PT73A	1	PCLKT1_0/MPI_CLK
G18	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT71C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT71B	1	MPI_RETRY
F18	PT71A	1	A0/MPI_ADDR14
J18	PT69D	1	A1/MPI_ADDR15
J19	PT69C	1	A2/MPI_ADDR16
C20	PT69B	1	A3/MPI_ADDR17
C19	PT69A	1	A4/MPI_ADDR18
K18	PT66D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT66C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT66B	1	A5/MPI_ADDR19
E19	PT66A	1	A6/MPI_ADDR20
H19	PT63D	1	D27/MPI_DATA27
H20	PT63C	1	VREF1_1
A18	PT63B	1	A7/MPI_ADDR21
B18	PT63A	1	A8/MPI_ADDR22
H21	PT61D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT61C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT61B	1	A9/MPI_ADDR23
B19	PT61A	1	A10/MPI_ADDR24
H22	PT58D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT58C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT58B	1	A11/MPI_ADDR25
G20	PT58A	1	A12/MPI_ADDR26
K21	PT57D	1	D11/MPI_DATA11
K22	PT57C	1	D12/MPI_DATA12
A20	PT57B	1	A13/MPI_ADDR27
B20	PT57A	1	A14/MPI_ADDR28

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
A26	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N
C34	D_VDDOB2_L	-		D_VDDOB2_L	-	
B26	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P
C32	VCC12	-		VCC12	-	
E27	D_HDINN2_L	-	PCS 363 CH 2 IN N	D_HDINN2_L	-	PCS 363 CH 2 IN N
D27	D_HDINP2_L	-	PCS 363 CH 2 IN P	D_HDINP2_L	-	PCS 363 CH 2 IN P
G25	D_VDDIB2_L	-		D_VDDIB2_L	-	
F29	VCC12	-		VCC12	-	
H26	D_VDDIB1_L	-		D_VDDIB1_L	-	
F30	VCC12	-		VCC12	-	
D28	D_HDINP1_L	-	PCS 363 CH 1 IN P	D_HDINP1_L	-	PCS 363 CH 1 IN P
E28	D_HDINN1_L	-	PCS 363 CH 1 IN N	D_HDINN1_L	-	PCS 363 CH 1 IN N
B27	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P
F36	VCC12	-		VCC12	-	
A27	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N
F35	D_VDDOB1_L	-		D_VDDOB1_L	-	
A28	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N
M30	D_VDDOB0_L	-		D_VDDOB0_L	-	
B28	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P
F37	VCC12	-		VCC12	-	
E29	D_HDINN0_L	-	PCS 363 CH 0 IN N	D_HDINN0_L	-	PCS 363 CH 0 IN N
D29	D_HDINP0_L	-	PCS 363 CH 0 IN P	D_HDINP0_L	-	PCS 363 CH 0 IN P
H27	D_VDDIB0_L	-		D_VDDIB0_L	-	
G28	VCC12	-		VCC12	-	
J28	C_REFCLKP_L	-		C_REFCLKP_L	-	
K28	C_REFCLKN_L	-		C_REFCLKN_L	-	
F32	VCC12	-		VCC12	-	
G29	C_VDDIB3_L	-		C_VDDIB3_L	-	
C31	VCC12	-		VCC12	-	
D30	C_HDINP3_L	-	PCS 362 CH 3 IN P	C_HDINP3_L	-	PCS 362 CH 3 IN P
E30	C_HDINN3_L	-	PCS 362 CH 3 IN N	C_HDINN3_L	-	PCS 362 CH 3 IN N
B29	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P
F38	VCC12	-		VCC12	-	
A29	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N
J33	C_VDDOB3_L	-		C_VDDOB3_L	-	
A30	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N
K33	C_VDDOB2_L	-		C_VDDOB2_L	-	
B30	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P
J34	VCC12	-		VCC12	-	
F31	C_HDINN2_L	-	PCS 362 CH 2 IN N	C_HDINN2_L	-	PCS 362 CH 2 IN N
E31	C_HDINP2_L	-	PCS 362 CH 2 IN P	C_HDINP2_L	-	PCS 362 CH 2 IN P
G30	C_VDDIB2_L	-		C_VDDIB2_L	-	
H28	VCC12	-		VCC12	-	
C37	C_VDDIB1_L	-		C_VDDIB1_L	-	
H30	VCC12	-		VCC12	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D32	C_HDINP1_L	-	PCS 362 CH 1 IN P	C_HDINP1_L	-	PCS 362 CH 1 IN P
E32	C_HDINN1_L	-	PCS 362 CH 1 IN N	C_HDINN1_L	-	PCS 362 CH 1 IN N
B31	C_HDOUTP1_L	-	PCS 362 CH 1 OUT P	C_HDOUTP1_L	-	PCS 362 CH 1 OUT P
K32	VCC12	-		VCC12	-	
A31	C_HDOUTN1_L	-	PCS 362 CH 1 OUT N	C_HDOUTN1_L	-	PCS 362 CH 1 OUT N
L32	C_VDDOB1_L	-		C_VDDOB1_L	-	
A32	C_HDOUTN0_L	-	PCS 362 CH 0 OUT N	C_HDOUTN0_L	-	PCS 362 CH 0 OUT N
M31	C_VDDOB0_L	-		C_VDDOB0_L	-	
B32	C_HDOUTP0_L	-	PCS 362 CH 0 OUT P	C_HDOUTP0_L	-	PCS 362 CH 0 OUT P
H37	VCC12	-		VCC12	-	
E33	C_HDINN0_L	-	PCS 362 CH 0 IN N	C_HDINN0_L	-	PCS 362 CH 0 IN N
D33	C_HDINP0_L	-	PCS 362 CH 0 IN P	C_HDINP0_L	-	PCS 362 CH 0 IN P
G31	C_VDDIB0_L	-		C_VDDIB0_L	-	
J29	VCC12	-		VCC12	-	
L29	B_REFCLKP_L	-		B_REFCLKP_L	-	
M29	B_REFCLKN_L	-		B_REFCLKN_L	-	
J31	VCC12	-		VCC12	-	
H31	B_VDDIB3_L	-		B_VDDIB3_L	-	
J30	VCC12	-		VCC12	-	
D34	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
E34	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
B33	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
H38	VCC12	-		VCC12	-	
A33	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
C38	B_VDDOB3_L	-		B_VDDOB3_L	-	
A34	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
L31	B_VDDOB2_L	-		B_VDDOB2_L	-	
B34	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G38	VCC12	-		VCC12	-	
E35	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
D35	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H32	B_VDDIB2_L	-		B_VDDIB2_L	-	
K29	VCC12	-		VCC12	-	
K30	B_VDDIB1_L	-		B_VDDIB1_L	-	
F33	VCC12	-		VCC12	-	
D36	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
E36	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
B35	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L34	VCC12	-		VCC12	-	
A35	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
K35	B_VDDOB1_L	-		B_VDDOB1_L	-	
A36	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
G39	B_VDDOB0_L	-		B_VDDOB0_L	-	
B36	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
J35	VCC12	-		VCC12	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH27	VCCAUX	-		VCCAUX	-	
AH29	VCCAUX	-		VCCAUX	-	
AJ14	VCCAUX	-		VCCAUX	-	
AJ15	VCCAUX	-		VCCAUX	-	
AJ28	VCCAUX	-		VCCAUX	-	
AJ29	VCCAUX	-		VCCAUX	-	
P14	VCCAUX	-		VCCAUX	-	
P15	VCCAUX	-		VCCAUX	-	
P28	VCCAUX	-		VCCAUX	-	
P29	VCCAUX	-		VCCAUX	-	
R14	VCCAUX	-		VCCAUX	-	
R16	VCCAUX	-		VCCAUX	-	
R17	VCCAUX	-		VCCAUX	-	
R18	VCCAUX	-		VCCAUX	-	
R19	VCCAUX	-		VCCAUX	-	
R20	VCCAUX	-		VCCAUX	-	
R23	VCCAUX	-		VCCAUX	-	
R24	VCCAUX	-		VCCAUX	-	
R25	VCCAUX	-		VCCAUX	-	
R26	VCCAUX	-		VCCAUX	-	
R27	VCCAUX	-		VCCAUX	-	
R29	VCCAUX	-		VCCAUX	-	
T15	VCCAUX	-		VCCAUX	-	
T28	VCCAUX	-		VCCAUX	-	
U15	VCCAUX	-		VCCAUX	-	
U28	VCCAUX	-		VCCAUX	-	
V15	VCCAUX	-		VCCAUX	-	
V28	VCCAUX	-		VCCAUX	-	
W15	VCCAUX	-		VCCAUX	-	
W28	VCCAUX	-		VCCAUX	-	
Y15	VCCAUX	-		VCCAUX	-	
Y28	VCCAUX	-		VCCAUX	-	
F3	VCCIO1	-		VCCIO1	-	
F39	VCCIO1	-		VCCIO1	-	
G35	VCCIO1	-		VCCIO1	-	
G8	VCCIO1	-		VCCIO1	-	
L19	VCCIO1	-		VCCIO1	-	
L24	VCCIO1	-		VCCIO1	-	
M16	VCCIO1	-		VCCIO1	-	
M27	VCCIO1	-		VCCIO1	-	
N11	VCCIO1	-		VCCIO1	-	
N32	VCCIO1	-		VCCIO1	-	
AA4	VCCIO2	-		VCCIO2	-	
H7	VCCIO2	-		VCCIO2	-	
J4	VCCIO2	-		VCCIO2	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C[1]	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C[1]	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C[1]	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C[1]	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.