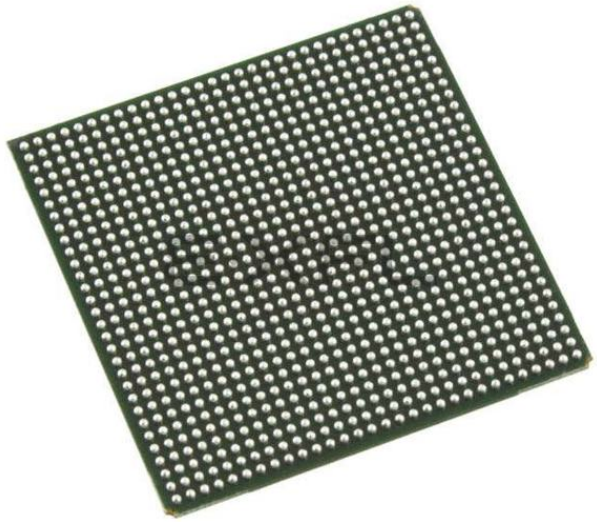
Lattice Semiconductor Corporation - LFSC3GA25E-6F900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	378
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga25e-6f900c

DLLs and dynamic glitch free clock MUXs which are required in today's high end system designs. High-speed, high-bandwidth I/O make this family ideal for high-throughput systems.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeSC family of FPGA devices. Synthesis library support for LatticeSC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeSC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeSC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

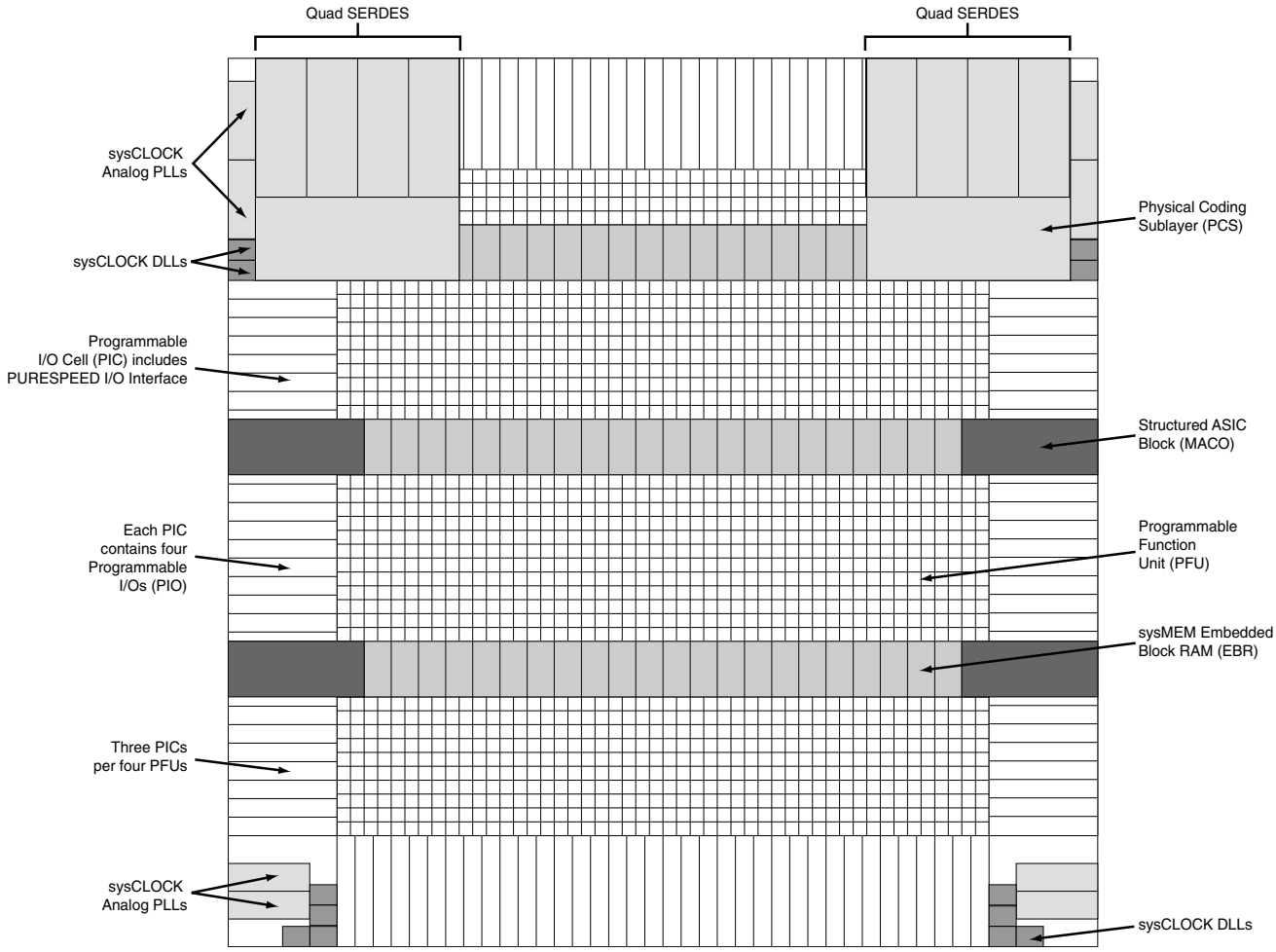
Innovative high-performance FPGA architecture, high-speed SERDES with PCS support, sysMEM embedded memory and high performance I/O are combined in the LatticeSC to provide excellent performance for today's leading edge systems designs. Table 1-3 details the performance of several common functions implemented within the LatticeSC.

Table1-3. Speed Performance for Typical Functions[1]

Functions	Performance (MHz)[2]
32-bit Address Decoder	539
64-bit Address Decoder	517
32:1 Multiplexer	779
64-bit Adder (ripple)	353
32x8 Distributed Single Port (SP) RAM	768
64-bit Counter (up or down counter, non-loadable)	369
True Dual-Port 1024x18 bits	372
FIFO Port A: x36 bits, B: x9 bits	375

1. For additional information, see Typical Building BLock Function Performance table in this data sheet.
2. Advance information (-7 speed grade).

Figure 2-1. Simplified Block Diagram (Top Level)



PURESPEED I/O Buffer Banks

LatticeSC devices have seven PURESPEED I/O buffer banks; each is capable of supporting multiple I/O standards. Each PURESPEED I/O bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-26 shows the seven banks and their associated supplies. Table 2-7 lists the maximum number of I/Os per bank for the whole LatticeSC family.

In the LatticeSC devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI33 and PCIX33) are powered using V_{CCIO}. In addition to the bank V_{CCIO} supplies, the LatticeSC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers. VCCAUX also powers a predriver of single-ended output buffers to enhance buffer performance.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeSC devices any I/O pin in a bank can be configured to be a dedicated reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Differential drivers have user selectable internal or external bias. External bias is brought in by the VREF1 pin in the bank. External bias for differential buffers is needed for applications that requires tighter than standard output common mode range.

Since a bank can have only one external bias circuit for differential drivers, LVDS and RSDS differential outputs can be mixed in a bank.

If a differential driver is configured in a bank, one pin in that bank becomes a DIFFR pin. This DIFFR pin must be connected to ground via an external 1K +/-1% ohm resistor. Note that differential drivers are not supported in banks 1, 4 and 5.

In addition, there are dedicated Terminating Supply (V_{TT}) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These V_{TT} pins are available in banks 2-7, these pins are not available in some packages. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.

There are further restrictions on the use of V_{TT} pins, for additional details refer to technical information at the end of this data sheet.

this allows for easy integration with the rest of the system. These capabilities make the LatticeSC ideal for many multiple power supply and hot-swap applications. The maximum current during hot socketing is 4mA. See Hot Socketing Specifications in Chapter 3 of this data sheet.

Power-Up Requirements

To prevent high power supply and input pin currents, each VCC, VCC12, VCCAUX, VCCIO and VCCJ power supplies must have a monotonic ramp up time of 75 ms or less to reach its minimum operating voltage. Apart from VCC and VCC12, which have an additional requirement, and VCCIO and VCCAUX, which also have an additional requirement, the VCC, VCC12, VCCAUX, VCCIO and VCCJ power supplies can ramp up in any order, with no restriction on the time between them. However, the ramp time for each must be 75 ms or less. Configuration of the device will not proceed until the last power supply has reached its minimum operating voltage.

Additional Requirement for VCC and VCC12:
VCC12 must always be higher than VCC. This condition must be maintained at ALL times, including during power-up and power-down. Note that for 1.2V only operation, it is advisable to source both of these supplies from the same power supply.

Additional Requirement for VCCIO and VCCAUX:
If any VCCIOs are 1.2/1.5/1.8V, then VCCAUX MUST be applied before them. If any VCCIO is 1.2/1.5/1.8V and is powered up before VCCAUX, then when VCCAUX is powered up, it may drag VCCIO up with it as it crosses through the VCCIO value. (Note: If the VCCIO supply is capable of sinking current, as well as the more usual sourcing capability, this behavior is eliminated. However, the amount of current that the supply needs to sink is unknown and is likely to be in the hundreds of milliamps range).

Power-Down Requirements

To prevent high power supply and input pin currents, power must be removed monotonically from either VCC or VCCAUX (and must reach the power-down trip point of 0.5V for VCC, 0.95V for VCCAUX) before power is removed monotonically from VCC12, any of the VCCIOs, or VCCJ. Note that VCC12 can be removed at the same time as VCC, but it cannot be removed earlier. In many applications, VCC and VCC12 will be sourced from the same power supply and so will be removed together. For systems where disturbance of the user pins is a don't care condition, the power supplies can be removed in any order as long as they power down monotonically within 200ms of each other.

Additionally, if any banks have VCCIO=3.3V nominal (potentially banks 1, 4, 5) then VCCIO for those banks must not be lower than VCCAUX during power-down. The normal variation in ramp-up times of power supplies and voltage regulators is not a concern here.

Note: The SERDES power supplies are NOT included in these requirements and have no specific sequencing requirements. However, when using the SERDES with VDDIB or VDDOB that is greater than 1.2V (1.5V nominal for example), the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in the ramp-up times of power supplies and voltage regulators is not a concern here.

SERDES Power Supply Sequencing Requirements

When using the SERDES with 1.5V VDDIB or VDDOB supplies, the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and the 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in ramp-up times of power supples and voltage regulators is not a concern.

Additional Requirement for SERDES Power Supply
All VCC12 pins need to be connected on all devices independent of functionality used on the device. This analog supply is used by both the RX and TX portions of the SERDES and is used to control the core SERDES logic regardless of the SERDES being used in the design. VDDIB and VDDOB are used as supplies for the terminations on the CML input and output buffers. If a particular channel is not used, these can be UNCONNECTED (floating).

- 8-bit SERDES Only
- 10-bit SERDES Only
- SONET (STS-12/STS-48)
- Gigabit Ethernet
- Fibre Channel
- XAUI
- Serial RapidIO
- PCI-Express
- Generic 8b10b

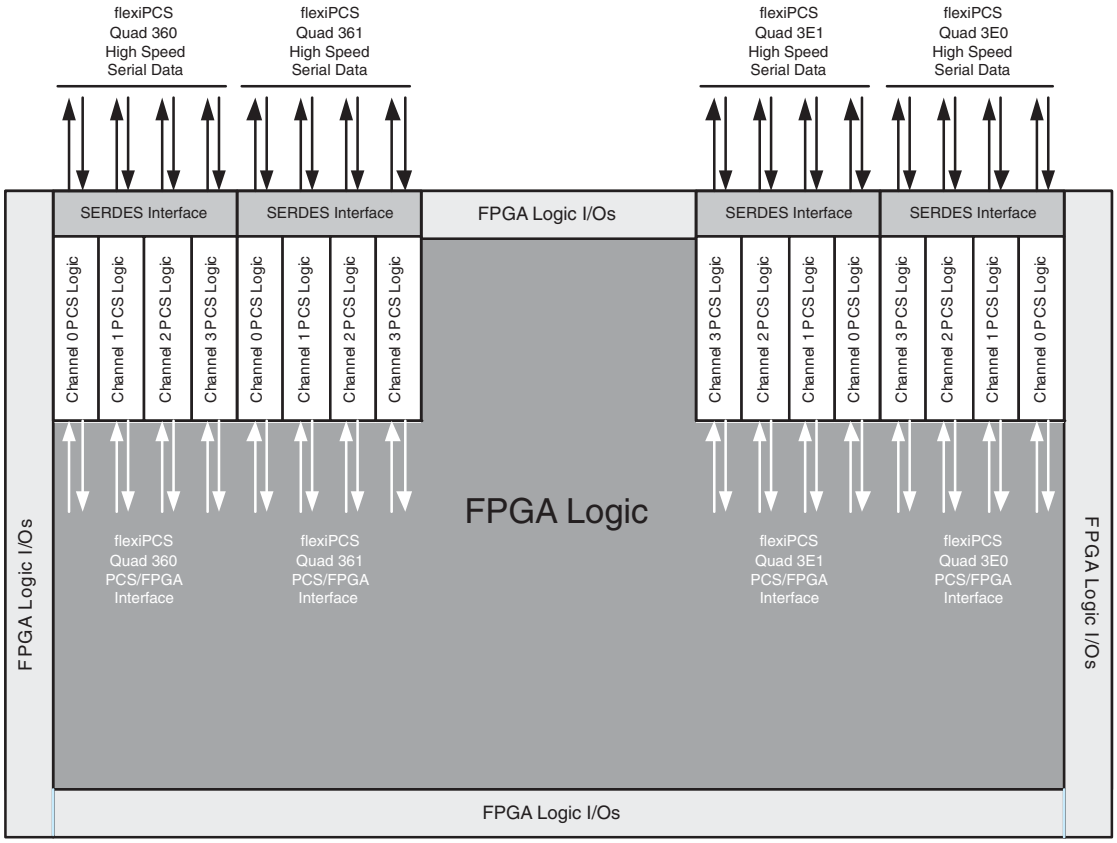
flexiPCS Quad

The flexiPCS logic is arranged in quads containing logic for four independent full-duplex data channels. Each device in the LatticeSC family has up to eight quads of flexiPCS logic. The LatticeSC Family Selection Guide table on the first page of this data sheet contains the number of flexiPCS channels present on the chip. Note that in some packages (particularly lower pin count packages), not all channels from all quads on a given device may be bonded to package pins.

Each quad supports up to four channels of full-duplex data and can be programmed into any one of several protocol based modes. Each quad requires its own reference clock which can be sourced externally or from the FPGA logic. The user can utilize between one and four channels in a quad, depending on the application.

Figure 2-30 shows an example of four flexiPCS quads in a LatticeSC device. Quads are labeled according to the address of their software controlled registers.

Figure 2-30. LatticeSC flexiPCS



Since each quad has its own reference clock, different quads can support different standards on the same chip. This feature makes the LatticeSC family of devices ideal for bridging between different standards.

Initialization and Standby Supply Current

The table below indicates initialization and standby supply current while operating at 85°C junction temperature (T_J), which is the high end of the commercial temperature range, and 105°C, which is the high end of the industrial temperature range. This data assumes all outputs are tri-stated and all inputs are configured as LVCMOS and held at V_{CCIO} or GND. The remaining SERDES supply current for V_{DDIB} and V_{DDOB} is detailed in the SERDES section of this data sheet. For power at your design temperature, it is recommended to use the Power Calculator tool which is accessible in ispLEVER or can be used as a standalone tool. For more information on supply current, see the reference to additional technical documentation available at the end of this data sheet.

Over Recommended Operating Conditions

Symbol	Condition	Parameter	Device	25°C Typ.[1]	85°C Max.[2]		105°C Max.[2]	Units
				All	-5, -6	-7	-5, -6	
I_{CC}	(VCC = 1.2V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	65	449	678	755	mA
			LFSC/M25	113	798	1255	1343	mA
			LFSC/M40	159	1178	2006	1981	mA
			LFSC/M80	276	2122	3827	3569	mA
			LFSC/M115	454	3376	—	5679	mA
	(VCC = 1.0V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	45	312	471	524	mA
			LFSC/M25	79	554	872	933	mA
			LFSC/M40	110	818	1393	1375	mA
			LFSC/M80	191	1473	2658	2478	mA
			LFSC/M115	315	2344	—	3943	mA
I_{CC12}		1.2V Power Supply Current for Configuration Logic, FPGA PLL, SERDES PLL and SERDES Analog Supplies	LFSC/M15	23	39	59	35	mA
			LFSC/M25	25	50	78	56	mA
			LFSC/M40	31	78	133	89	mA
			LFSC/M80	50	108	195	123	mA
			LFSC/M115	65	131	—	154	mA
I_{CCAUX}		Auxiliary Operating Power Supply Current	LFSC/M15	7	12	19	14	mA
			LFSC/M25	9	16	25	18	mA
			LFSC/M40	12	23	39	25	mA
			LFSC/M80	13	25	45	23	mA
			LFSC/M115	16	27	—	26	mA
I_{CCIO} and I_{CCJ}		Bank Power Supply Current (per bank)	LFSC/M15	0.1	0.2	0.3	0.2	mA
			LFSC/M25	0.3	0.6	1.0	0.7	mA
			LFSC/M40	0.4	0.9	1.5	1.0	mA
			LFSC/M80	0.5	1.1	2.1	1.3	mA
			LFSC/M115	0.7	1.5	—	1.8	mA

1. I_{CC} is specified at T_J = 25°C and typical V_{CC}.
2. I_{CC} is specified at the respective commercial and industrial maximum T_J and V_{CC} limits.

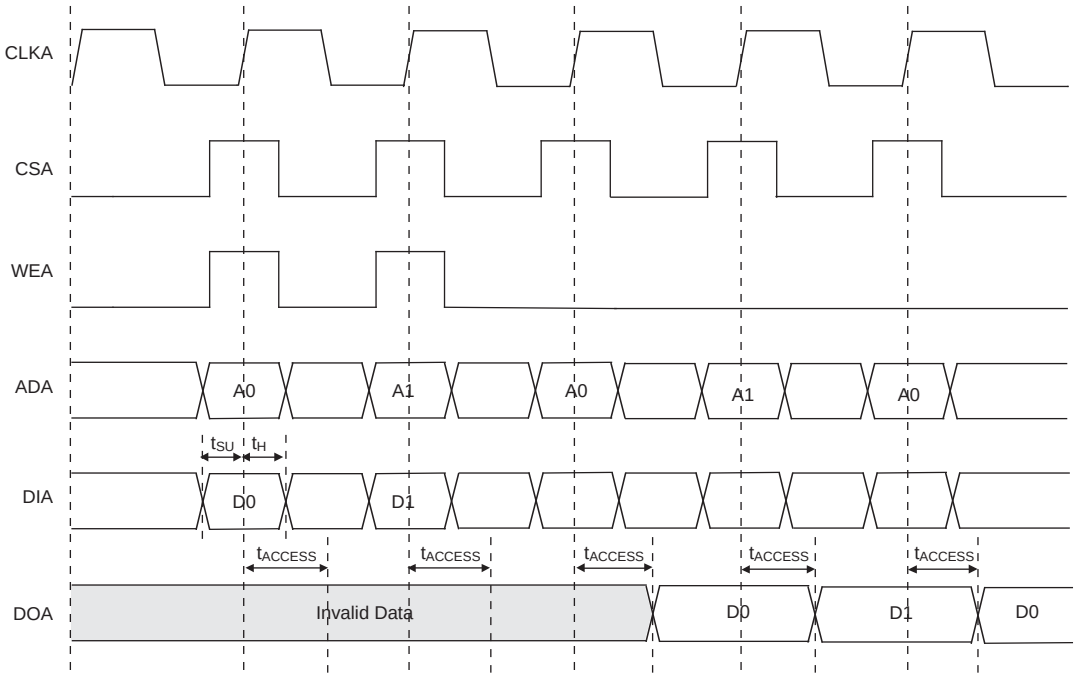
LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	0.024	-0.106	0.019	-0.004	0.016	0.099	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive	0.074	-0.134	0.08	-0.022	0.088	0.089	ns
LVCMOS18_OD	LVCMOS 1.8 open drain	0.002	-0.206	0	-0.196	-0.002	-0.221	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	-0.344	-0.164	-0.379	-0.186	-0.412	-0.209	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	-0.125	-0.137	-0.145	-0.157	-0.164	-0.176	ns
LVCMOS15_12mA	LVCMOS 1.5 12mA drive	-0.027	-0.166	-0.043	-0.07	-0.059	0.026	ns
LVCMOS15_16mA	LVCMOS 1.5 16mA drive	0.025	-0.195	0.013	-0.089	0.003	0.017	ns
LVCMOS15_OD	LVCMOS 1.5 open drain	-0.047	-0.267	-0.067	-0.267	-0.087	-0.299	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	-0.473	-0.293	-0.505	-0.317	-0.537	-0.34	ns
LVCMOS12_4mA	LVCMOS 1.2 4mA drive	-0.218	-0.239	-0.25	-0.271	-0.28	-0.303	ns
LVCMOS12_8mA	LVCMOS 1.2 8mA drive	-0.109	-0.269	-0.143	-0.181	-0.176	-0.093	ns
LVCMOS12_12mA	LVCMOS 1.2 12mA drive	-0.054	-0.3	-0.085	-0.203	-0.114	-0.106	ns
LVCMOS12_OD	LVCMOS 1.2 open drain	-0.126	-0.371	-0.166	-0.398	-0.204	-0.43	ns
PCI33	PCI	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX33	PCI-X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX15	PCI-X 1.5	0.208	0.227	0.233	0.312	0.259	0.398	ns
AGP1X33	AGP-1X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
AGP2X33	AGP-2X	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns

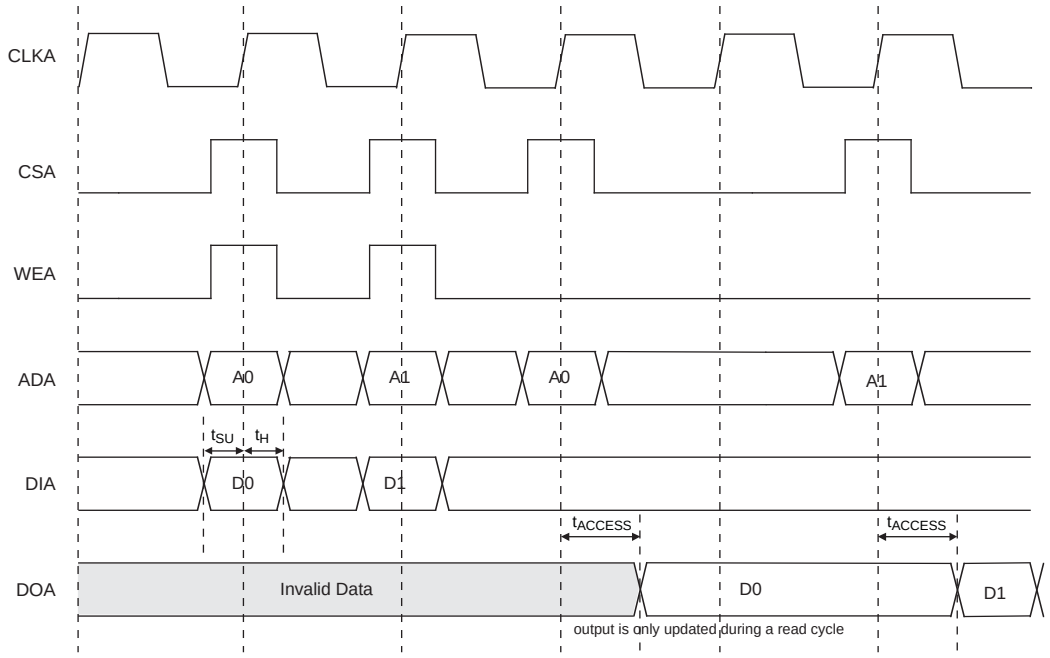
EBR Memory Timing Diagrams

Figure 3-6. Read Mode



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-7. Read Mode with Input Registers Only



LatticeSC/M sysCONFIG Port Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
General Configuration Timing				
t_{SMODE}	M[3:0] Setup Time to INITN High	0	—	ns
t_{HMODE}	M[3:0] Hold Time from INITN High	600	—	ns
t_{RW}	RESETN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
t_{PGW}	PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
$f_{ESB\_CLK\_FRQ}$	System Bus ESB_CLK Frequency (No Wait States)	—	133	MHz
sysCONFIG Master Parallel Configuration Mode				
t_{SMB}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMB}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMB}	RCLK Low Time (Non-compressed Bitstreams)	0.5	0.5	CCLK periods
	RCLK Low Time (Compressed Bitstreams)	0.5	7.5	CCLK periods
t_{CHMB}	RCLK High Time	0.5	0.5	CCLK periods
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CSCK Low	—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low	0	2	µs
t_{SCK}	CSCK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CSCK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN Low to CSCK high Setup Time	—	15	ns
f_{MAXSPI}	Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0)	—	50	MHz
t_{SUSPI}	SOSPI/D0 Data Setup Time Before CSCK	7	—	ns
t_{HSPI}	SOSPI/D0 Data Hold Time After CSCK	2	—	ns
	Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
	Duty Cycle	40	60	%
sysCONFIG Master Serial Configuration Mode				
t_{SMS}	DIN Setup Time	4.4	—	ns
t_{HMS}	DIN Hold Time	0	—	ns
f_{CMS}	CCLK Frequency (No Divider)	90	190	MHz
f_{C_DIV}	CCLK Frequency (Div 128)	0.70	1.48	MHz
t_{D}	CCLK to DOUT Delay	—	7.5	ns
sysCONFIG Master Parallel Configuration Mode				
t_{AVMP}	RCLK to Address Valid	—	10	ns
t_{SMP}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMP}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMP}	RCLK Low Time (Non-compressed Bitstream)	7.5	7.5	CCLK periods
	RCLK Low Time (Compressed Bitstream)	0.5	63.5	
t_{CHMP}	RCLK High Time	0.5	0.5	CCLK periods
t_{DMP}	CCLK to DOUT	—	7.5	ns

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB10	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
J10	VCC	-		VCC	-	
J21	VCC	-		VCC	-	
K10	VCC	-		VCC	-	
K11	VCC	-		VCC	-	
K12	VCC	-		VCC	-	
K13	VCC	-		VCC	-	
K14	VCC	-		VCC	-	
K17	VCC	-		VCC	-	
K18	VCC	-		VCC	-	
K19	VCC	-		VCC	-	
K20	VCC	-		VCC	-	
K21	VCC	-		VCC	-	
K22	VCC	-		VCC	-	
K9	VCC	-		VCC	-	
L10	VCC	-		VCC	-	
L21	VCC	-		VCC	-	
M10	VCC	-		VCC	-	
M21	VCC	-		VCC	-	
N10	VCC	-		VCC	-	
N21	VCC	-		VCC	-	
P10	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
U10	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V10	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W10	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y10	VCC	-		VCC	-	
Y21	VCC	-		VCC	-	
H11	VCCAUX	-		VCCAUX	-	
H12	VCCAUX	-		VCCAUX	-	
H19	VCCAUX	-		VCCAUX	-	
H20	VCCAUX	-		VCCAUX	-	
M23	VCCAUX	-		VCCAUX	-	
M24	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
N24	VCCAUX	-		VCCAUX	-	
U23	VCCAUX	-		VCCAUX	-	
U24	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	
V24	VCCAUX	-		VCCAUX	-	
W23	VCCAUX	-		VCCAUX	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ31	PB9A	5		PB9A	5	
AH30	PB9B	5		PB9B	5	
AM30	PB11A	5		PB11A	5	
AM29	PB11B	5		PB11B	5	
AH29	PB11C	5		PB11C	5	
AH28	PB11D	5		PB11D	5	
AJ27	PB12A	5		PB13A	5	
AK27	PB12B	5		PB13B	5	
AE22	PB12C	5		PB13C	5	
AF23	PB12D	5		PB13D	5	
AL28	PB13A	5		PB15A	5	
AL27	PB13B	5		PB15B	5	
AC21	PB13C	5		PB15C	5	
AD21	PB13D	5		PB15D	5	
AM28	PB15A	5		PB17A	5	
AM27	PB15B	5		PB17B	5	
AG23	PB15C	5		PB17C	5	
AF22	PB15D	5		PB17D	5	
AG26	PB16A	5		PB19A	5	
AG25	PB16B	5		PB19B	5	
AL26	PB17A	5		PB22A	5	
AM26	PB17B	5		PB22B	5	
AJ24	PB19A	5		PB25A	5	
AK24	PB19B	5		PB25B	5	
AE21	PB19C	5		PB25C	5	
AE20	PB19D	5		PB25D	5	
AJ22	PB20A	5	PCLKT5_3	PB30A	5	PCLKT5_3
AK22	PB20B	5	PCLKC5_3	PB30B	5	PCLKC5_3
AG22	PB20C	5	PCLKT5_4	PB30C	5	PCLKT5_4
AH22	PB20D	5	PCLKC5_4	PB30D	5	PCLKC5_4
AL23	PB21A	5	PCLKT5_5	PB31A	5	PCLKT5_5
AL22	PB21B	5	PCLKC5_5	PB31B	5	PCLKC5_5
AH23	PB21C	5		PB31C	5	
AH24	PB21D	5		PB31D	5	
AJ21	PB23A	5	PCLKT5_0	PB33A	5	PCLKT5_0
AK21	PB23B	5	PCLKC5_0	PB33B	5	PCLKC5_0
AE19	PB23C	5		PB33C	5	
AF19	PB23D	5	VREF2_5	PB33D	5	VREF2_5
AM23	PB24A	5	PCLKT5_1	PB34A	5	PCLKT5_1
AM22	PB24B	5	PCLKC5_1	PB34B	5	PCLKC5_1
AH25	PB24C	5	PCLKT5_6	PB34C	5	PCLKT5_6
AH26	PB24D	5	PCLKC5_6	PB34D	5	PCLKC5_6
AL21	PB25A	5	PCLKT5_2	PB35A	5	PCLKT5_2
AL20	PB25B	5	PCLKC5_2	PB35B	5	PCLKC5_2
AG20	PB25C	5	PCLKT5_7	PB35C	5	PCLKT5_7
AG19	PB25D	5	PCLKC5_7	PB35D	5	PCLKC5_7
AJ19	PB28A	5		PB37A	5	
AK19	PB28B	5		PB37B	5	
AD18	PB28C	5		PB37C	5	
AE18	PB28D	5		PB37D	5	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB47C	4	PCLKT4_6	PB54C	4	PCLKT4_6
AH10	PB47D	4	PCLKC4_6	PB54D	4	PCLKC4_6
AK12	PB49A	4	PCLKT4_0	PB55A	4	PCLKT4_0
AJ12	PB49B	4	PCLKC4_0	PB55B	4	PCLKC4_0
AF14	PB49C	4	VREF2_4	PB55C	4	VREF2_4
AE14	PB49D	4		PB55D	4	
AL11	PB51A	4	PCLKT4_5	PB57A	4	PCLKT4_5
AL10	PB51B	4	PCLKC4_5	PB57B	4	PCLKC4_5
AH9	PB51C	4		PB57C	4	
AH8	PB51D	4		PB57D	4	
AK11	PB52A	4	PCLKT4_3	PB58A	4	PCLKT4_3
AJ11	PB52B	4	PCLKC4_3	PB58B	4	PCLKC4_3
AH7	PB52C	4	PCLKT4_4	PB58C	4	PCLKT4_4
AH6	PB52D	4	PCLKC4_4	PB58D	4	PCLKC4_4
AK8	PB53A	4		PB67A	4	
AJ8	PB53B	4		PB67B	4	
AF11	PB53C	4		PB67C	4	
AD12	PB55A	4		PB69A	4	
AE12	PB55B	4		PB69B	4	
AM6	PB56A	4		PB70A	4	
AM5	PB56B	4		PB70B	4	
AC12	PB56C	4		PB70C	4	
AL6	PB57A	4		PB73A	4	
AL5	PB57B	4		PB73B	4	
AG7	PB59A	4		PB74A	4	
AG8	PB59B	4		PB74B	4	
AK6	PB60A	4		PB75A	4	
AJ6	PB60B	4		PB75B	4	
AF10	PB60C	4		PB75C	4	
AE11	PB60D	4		PB75D	4	
AM4	PB61A	4		PB77A	4	
AM3	PB61B	4		PB77B	4	
AH5	PB63A	4		PB78A	4	
AH4	PB63B	4		PB78B	4	
AK5	PB64A	4		PB79A	4	
AJ5	PB64B	4		PB79B	4	
AF8	PB64C	4		PB79C	4	
AF7	PB64D	4		PB79D	4	
AL4	PB65A	4		PB81A	4	
AL3	PB65B	4		PB81B	4	
AG5	PB65C	4		PB81C	4	
AF6	PB65D	4		PB81D	4	
AK3	PB67A	4		PB82A	4	
AJ3	PB67B	4		PB82B	4	
AE10	PB67C	4	VREF1_4	PB82C	4	VREF1_4
AD10	PB67D	4		PB82D	4	
AL2	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AK2	PB68B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AE9	PB68C	4		PB83C	4	
AE8	PB68D	4		PB83D	4	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF21	PB26D	5		PB29D	5	
AN23	PB27A	5		PB45A	5	
AN22	PB27B	5		PB45B	5	
AP23	PB29A	5		PB55A	5	
AP22	PB29B	5		PB55B	5	
AG21	PB29C	5		PB55C	5	
AG20	PB29D	5		PB55D	5	
AP25	PB30A	5	PCLKT5_3	PB48A	5	PCLKT5_3
AP24	PB30B	5	PCLKC5_3	PB48B	5	PCLKC5_3
AD21	PB30C	5	PCLKT5_4	PB48C	5	PCLKT5_4
AD20	PB30D	5	PCLKC5_4	PB48D	5	PCLKC5_4
AL23	PB31A	5	PCLKT5_5	PB49A	5	PCLKT5_5
AL22	PB31B	5	PCLKC5_5	PB49B	5	PCLKC5_5
AH24	PB31C	5		PB49C	5	
AH23	PB31D	5		PB49D	5	
AM23	PB33A	5	PCLKT5_0	PB51A	5	PCLKT5_0
AM22	PB33B	5	PCLKC5_0	PB51B	5	PCLKC5_0
AJ24	PB33C	5		PB51C	5	
AJ23	PB33D	5	VREF2_5	PB51D	5	VREF2_5
AN21	PB34A	5	PCLKT5_1	PB52A	5	PCLKT5_1
AN20	PB34B	5	PCLKC5_1	PB52B	5	PCLKC5_1
AE19	PB34C	5	PCLKT5_6	PB52C	5	PCLKT5_6
AD19	PB34D	5	PCLKC5_6	PB52D	5	PCLKC5_6
AK21	PB35A	5	PCLKT5_2	PB53A	5	PCLKT5_2
AK20	PB35B	5	PCLKC5_2	PB53B	5	PCLKC5_2
AK23	PB35C	5	PCLKT5_7	PB53C	5	PCLKT5_7
AK22	PB35D	5	PCLKC5_7	PB53D	5	PCLKC5_7
AL20	PB37A	5		PB56A	5	
AL19	PB37B	5		PB56B	5	
AG19	PB37C	5		PB56C	5	
AF19	PB37D	5		PB56D	5	
AP21	PB38A	5		PB57A	5	
AP20	PB38B	5		PB57B	5	
AH21	PB38C	5		PB57C	5	
AH20	PB38D	5		PB57D	5	
AM20	PB39A	5		PB59A	5	
AM19	PB39B	5		PB59B	5	
AJ21	PB39C	5		PB59C	5	
AJ20	PB39D	5		PB59D	5	
AK19	PB41A	5		PB60A	5	
AK18	PB41B	5		PB60B	5	
AE18	PB41C	5		PB60C	5	
AD18	PB41D	5		PB60D	5	
AN19	PB42A	5		PB61A	5	
AN18	PB42B	5		PB61B	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
R7	NC	-		PR39D	2	
P7	NC	-		PR39C	2	
N3	NC	-		PR39B	2	
M3	NC	-		PR39A	2	
H1	NC	-		PR26B	2	
G1	NC	-		PR26A	2	
L5	NC	-		PR25B	2	
K5	NC	-		PR25A	2	
G2	NC	-		PR24B	2	
F2	NC	-		PR24A	2	
F1	NC	-		PR22B	2	
E1	NC	-		PR22A	2	
A2	GND	-		GND	-	
A33	GND	-		GND	-	
AA15	GND	-		GND	-	
AA20	GND	-		GND	-	
AA32	GND	-		GND	-	
AA4	GND	-		GND	-	
AB28	GND	-		GND	-	
AB6	GND	-		GND	-	
AC11	GND	-		GND	-	
AC18	GND	-		GND	-	
AC25	GND	-		GND	-	
AD23	GND	-		GND	-	
AD3	GND	-		GND	-	
AD31	GND	-		GND	-	
AE12	GND	-		GND	-	
AE15	GND	-		GND	-	
AE29	GND	-		GND	-	
AE7	GND	-		GND	-	
AE9	GND	-		GND	-	
AF20	GND	-		GND	-	
AF26	GND	-		GND	-	
AG32	GND	-		GND	-	
AG4	GND	-		GND	-	
AH13	GND	-		GND	-	
AH19	GND	-		GND	-	
AH25	GND	-		GND	-	
AH7	GND	-		GND	-	
AJ10	GND	-		GND	-	
AJ16	GND	-		GND	-	
AJ22	GND	-		GND	-	
AJ28	GND	-		GND	-	
AK3	GND	-		GND	-	
AK31	GND	-		GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
G27	A_REFCLKP_L	-	
H27	A_REFCLKN_L	-	
H25	VCC12	-	
H26	RESP_ULC	-	
B33	RESETN	1	
C34	TSALLN	1	
D34	DONE	1	
C33	INITN	1	
J27	M0	1	
K27	M1	1	
M26	M2	1	
L26	M3	1	
F30	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
G30	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
H28	PL15C	7	
J28	PL15D	7	
F31	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N25	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P25	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
D33	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E33	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
H29	PL18C	7	
J29	PL18D	7	VREF2_7
F32	PL19A	7	
G32	PL19B	7	
P26	PL19C	7	
N26	PL19D	7	
H30	PL26A	7	
J30	PL26B	7	
L28	PL26C	7	
M28	PL26D	7	
J31	PL43A	7	
K31	PL43B	7	
L27	PL43C	7	VREF1_7
M27	PL43D	7	DIFFR_7
J32	PL45A	7	
K32	PL45B	7	
L29	PL45C	7	
M29	PL45D	7	
H33	PL47A	7	
J33	PL47B	7	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J17	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT81B	1	MCA_CLK_P1_OUT
E16	PT81A	1	MCA_CLK_P1_IN
H15	PT78D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT78C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT78B	1	MCA_CLK_P2_OUT
C16	PT78A	1	MCA_CLK_P2_IN
L17	PT75D	1	MCA_DONE_OUT
K17	PT75C	1	BUSYN/RCLK/SCK
E17	PT75B	1	DP0/MPI_PAR0
F17	PT75A	1	MPI_TA
G17	PT73D	1	D23/MPI_DATA23
H17	PT73C	1	DP2/MPI_PAR2
A17	PT73B	1	PCLKC1_0
B17	PT73A	1	PCLKT1_0/MPI_CLK
G18	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT71C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT71B	1	MPI_RETRY
F18	PT71A	1	A0/MPI_ADDR14
J18	PT69D	1	A1/MPI_ADDR15
J19	PT69C	1	A2/MPI_ADDR16
C20	PT69B	1	A3/MPI_ADDR17
C19	PT69A	1	A4/MPI_ADDR18
K18	PT66D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT66C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT66B	1	A5/MPI_ADDR19
E19	PT66A	1	A6/MPI_ADDR20
H19	PT63D	1	D27/MPI_DATA27
H20	PT63C	1	VREF1_1
A18	PT63B	1	A7/MPI_ADDR21
B18	PT63A	1	A8/MPI_ADDR22
H21	PT61D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT61C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT61B	1	A9/MPI_ADDR23
B19	PT61A	1	A10/MPI_ADDR24
H22	PT58D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT58C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT58B	1	A11/MPI_ADDR25
G20	PT58A	1	A12/MPI_ADDR26
K21	PT57D	1	D11/MPI_DATA11
K22	PT57C	1	D12/MPI_DATA12
A20	PT57B	1	A13/MPI_ADDR27
B20	PT57A	1	A14/MPI_ADDR28

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
F25	B_HDINN0_L	-	PCS 361 CH 0 IN N
E25	B_HDINP0_L	-	PCS 361 CH 0 IN P
D28	B_VDDIB0_L	-	
G25	VCC12	-	
D29	A_VDDIB3_L	-	
C25	VCC12	-	
A25	A_HDINP3_L	-	PCS 360 CH 3 IN P
B25	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
E27	VCC12	-	
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
F26	A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
F27	A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E28	VCC12	-	
B28	A_HDINN2_L	-	PCS 360 CH 2 IN N
A28	A_HDINP2_L	-	PCS 360 CH 2 IN P
D30	A_VDDIB2_L	-	
C28	VCC12	-	
D31	A_VDDIB1_L	-	
C29	VCC12	-	
A29	A_HDINP1_L	-	PCS 360 CH 1 IN P
B29	A_HDINN1_L	-	PCS 360 CH 1 IN N
A30	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
E29	VCC12	-	
B30	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
F28	A_VDDOB1_L	-	
B31	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
F29	A_VDDOB0_L	-	
A31	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E30	VCC12	-	
B32	A_HDINN0_L	-	PCS 360 CH 0 IN N
A32	A_HDINP0_L	-	PCS 360 CH 0 IN P
D32	A_VDDIB0_L	-	
C32	VCC12	-	
E34	PL30A	7	
F34	PL30B	7	
F33	PL34A	7	
G33	PL34B	7	
K30	PL38A	7	
L30	PL38B	7	
G34	PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF40	PL76A	6		PL90A	6	
AG40	PL76B	6		PL90B	6	
AG36	PL76C	6		PL90C	6	
AH36	PL76D	6	DIFFR_6	PL90D	6	DIFFR_6
AF39	PL77A	6		PL91A	6	
AG39	PL77B	6		PL91B	6	
AF29	PL77C	6		PL91C	6	
AG29	PL77D	6		PL91D	6	
AH42	PL78A	6		PL92A	6	
AG42	PL78B	6		PL92B	6	
AG35	PL78C	6		PL92C	6	
AH35	PL78D	6		PL92D	6	
AG41	PL80A	6		PL94A	6	
AH41	PL80B	6		PL94B	6	
AG34	PL80C	6		PL94C	6	
AH34	PL80D	6		PL94D	6	
AJ42	PL81A	6		PL96A	6	
AK42	PL81B	6		PL96B	6	
AG33	PL81C	6		PL96C	6	
AH33	PL81D	6		PL96D	6	
AJ41	PL82A	6		PL98A	6	
AK41	PL82B	6		PL98B	6	
AJ37	PL82C	6		PL98C	6	
AK37	PL82D	6		PL98D	6	
AJ40	PL84A	6		PL99A	6	
AK40	PL84B	6		PL99B	6	
AJ34	PL84C	6		PL99C	6	
AK34	PL84D	6		PL99D	6	
AJ38	PL85A	6		PL103A	6	
AK38	PL85B	6		PL103B	6	
AH32	PL85C	6		PL103C	6	
AJ32	PL85D	6		PL103D	6	
AL42	PL86A	6		PL104A	6	
AM42	PL86B	6		PL104B	6	
AK36	PL86C	6		PL104C	6	
AL36	PL86D	6		PL104D	6	
AL38	PL89A	6		PL107A	6	
AM38	PL89B	6		PL107B	6	
AJ33	PL89C	6		PL107C	6	
AK33	PL89D	6	VREF2_6	PL107D	6	VREF2_6
AN42	PL90A	6		PL109A	6	
AP42	PL90B	6		PL109B	6	
AH31	PL90C	6		PL109C	6	
AJ31	PL90D	6		PL109D	6	
AN41	PL91A	6		PL112A	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BA19	PB73A	4		PB87A	4	
BA18	PB73B	4		PB87B	4	
AU19	PB73C	4		PB87C	4	
AU18	PB73D	4		PB87D	4	
AV19	PB74A	4	PCLKT4_2	PB89A	4	PCLKT4_2
AV18	PB74B	4	PCLKC4_2	PB89B	4	PCLKC4_2
AN19	PB74C	4	PCLKT4_7	PB89C	4	PCLKT4_7
AP19	PB74D	4	PCLKC4_7	PB89D	4	PCLKC4_7
BB17	PB75A	4	PCLKT4_1	PB90A	4	PCLKT4_1
BB16	PB75B	4	PCLKC4_1	PB90B	4	PCLKC4_1
AT19	PB75C	4	PCLKT4_6	PB90C	4	PCLKT4_6
AT18	PB75D	4	PCLKC4_6	PB90D	4	PCLKC4_6
BA17	PB77A	4	PCLKT4_0	PB91A	4	PCLKT4_0
BA16	PB77B	4	PCLKC4_0	PB91B	4	PCLKC4_0
AR19	PB77C	4	VREF2_4	PB91C	4	VREF2_4
AR18	PB77D	4		PB91D	4	
AY17	PB79A	4	PCLKT4_5	PB93A	4	PCLKT4_5
AY16	PB79B	4	PCLKC4_5	PB93B	4	PCLKC4_5
AN18	PB79C	4		PB93C	4	
AP18	PB79D	4		PB93D	4	
AW17	PB80A	4	PCLKT4_3	PB94A	4	PCLKT4_3
AW16	PB80B	4	PCLKC4_3	PB94B	4	PCLKC4_3
AU17	PB80C	4	PCLKT4_4	PB94C	4	PCLKT4_4
AU16	PB80D	4	PCLKC4_4	PB94D	4	PCLKC4_4
AV17	PB81A	4		PB95A	4	
AV16	PB81B	4		PB95B	4	
AL18	PB81C	4		PB95C	4	
AM18	PB81D	4		PB95D	4	
BB15	PB83A	4		PB97A	4	
BB14	PB83B	4		PB97B	4	
AP17	PB83C	4		PB97C	4	
AN17	PB83D	4		PB97D	4	
BA15	PB84A	4		PB98A	4	
BA14	PB84B	4		PB98B	4	
AT16	PB84C	4		PB98C	4	
AT15	PB84D	4		PB98D	4	
AV15	PB85A	4		PB99A	4	
AV14	PB85B	4		PB99B	4	
AR16	PB85C	4		PB99C	4	
AR15	PB85D	4		PB99D	4	
AY14	PB87A	4		PB101A	4	
AY13	PB87B	4		PB101B	4	
AU15	PB87C	4		PB101C	4	
AU14	PB87D	4		PB101D	4	
BB13	PB88A	4		PB102A	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG38	NC	-		PL95A	6	
AH38	NC	-		PL95B	6	
AJ39	NC	-		PL100A	6	
AK39	NC	-		PL100B	6	
AL41	NC	-		PL105A	6	
AM41	NC	-		PL105B	6	
AN40	NC	-		PL108A	6	
AM40	NC	-		PL108B	6	
AM39	NC	-		PL111A	6	
AN39	NC	-		PL111B	6	
AR42	NC	-		PL113A	6	
AT42	NC	-		PL113B	6	
AT1	NC	-		PR113B	3	
AR1	NC	-		PR113A	3	
AN4	NC	-		PR111B	3	
AM4	NC	-		PR111A	3	
AM3	NC	-		PR108B	3	
AN3	NC	-		PR108A	3	
AM2	NC	-		PR105B	3	
AL2	NC	-		PR105A	3	
AK4	NC	-		PR100B	3	
AJ4	NC	-		PR100A	3	
AH5	NC	-		PR95B	3	
AG5	NC	-		PR95A	3	
P6	NC	-		PR39B	2	
N6	NC	-		PR39A	2	
L3	NC	-		PR36B	2	
K3	NC	-		PR36A	2	
M5	NC	-		PR35A	2	
L4	NC	-		PR32B	2	
K4	NC	-		PR32A	2	
A2	GND	-		GND	-	
A41	GND	-		GND	-	
AA20	GND	-		GND	-	
AA23	GND	-		GND	-	
AA3	GND	-		GND	-	
AA39	GND	-		GND	-	
AB20	GND	-		GND	-	
AB23	GND	-		GND	-	
AB4	GND	-		GND	-	
AB40	GND	-		GND	-	
AC17	GND	-		GND	-	
AC19	GND	-		GND	-	
AC21	GND	-		GND	-	
AC22	GND	-		GND	-	