Lattice Semiconductor Corporation - LFSC3GA25E-6FFA1020I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

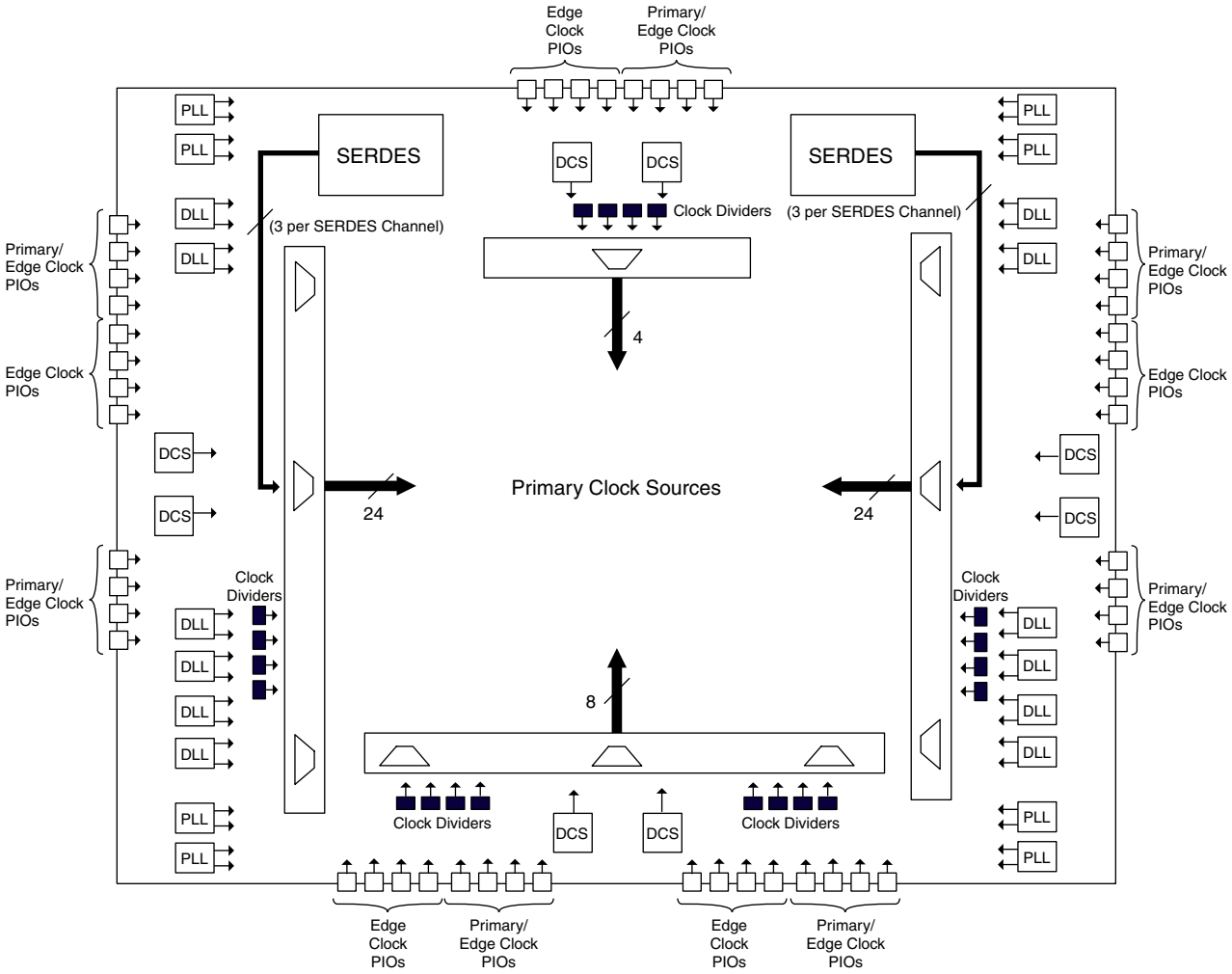
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	476
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFcBGA Rev 2 (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga25e-6ffa1020i

- Two outputs per PLL
- Clock divider outputs
- Digital Clock Select (DCS) block outputs
- Three outputs per SERDES quad

Figure 2-5 shows the arrangement of the primary clock sources.

Figure 2-5. Clock Sources

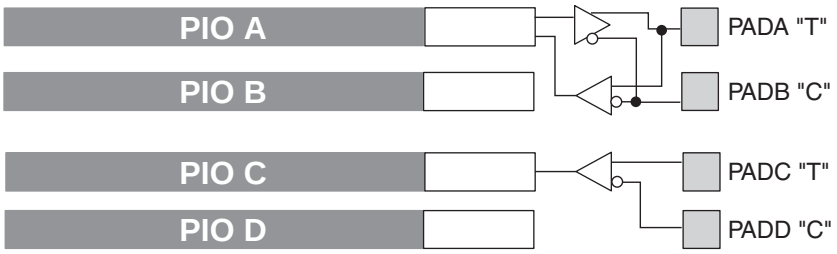


Primary Clock Routing

The clock routing structure in LatticeSC devices consists of 12 Primary Clock lines per quadrant. The primary clocks are generated from 64:1 MUXs located in each quadrant. Three of the inputs to each 64:1 MUX comes from local routing, one is connected to GND and rest of the 60 inputs are from the primary clock sources. Figure 2-6 shows this clock routing.

high-speed interfaces in the LatticeSC devices. Figure 2-18 shows how differential receivers and drivers are arranged between PIOs.

Figure 2-18. Differential Drivers and Receivers



*Differential Driver only available on right and left of the device.

PIO

The PIO contains five blocks: an input register block, output register block, tristate register block, update block, and a control logic block. These blocks contain registers for both single data rate (SDR), double data rate (DDR), and shift register operation along with the necessary clock and selection logic.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 show the diagram of the input register block. The signal from the PURESPEED I/O buffer (DI) enters the input register block and can be used for three purposes, as a source for the combinatorial (INDD) and clock outputs (INCK), the input into the SDR register/latch block and the input to the delay block. The output of the delay block can be used as combinatorial (INDD) and clock (INCK) outputs, an input to the DDR/Shift Register Block or an input into the SDR register block.

Input SDR Register/Latch Block

The SDR register/latch block has a latch and a register/latch that can be used in a variety of combinations to provide a registered or latched output (INFF). The latch operates off high-speed input clocks and latches data on the positive going edge. The register/latch operates off the low-speed input clock and registers/latches data on the positive going edge. Both the latch and the register/latch have a clock enable input that is driven by the input clock enable. In addition both have a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register and latch LSR inputs are driven from LSRI, which is generated from the PIO control MUX. The GSR inputs are driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Input Delay Block

The delay block uses 144 tapped delay lines to obtain coarse and fine delay resolution. These delays can be adjusted during configuration or automatically via DLL or AIL blocks. The Adaptive Input Logic (AIL) uses this delay block to adjust automatically the delay in the data path to ensure that it has sufficient setup and hold time.

The delay line in this block matches the delay line that is used in the 12 on-chip DLLs. The delay line can be set via configuration bits or driven from a calibration bus that allows the setting to be controlled either from one of the on-chip DLLs or user logic. Controlling the delay from one of the on-chip DLLs allow the delay to be calibrated to the DLL clock and hence compensated for the variations in process, voltage and temperature.

Table 2-9. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)	On-chip Termination
Single Ended Interfaces			
LVTTL33[3]	—	3.3	None
LVCMOS 33, 25, 18, 15, 12[3]	—	3.3/2.5/1.8/1.5/1.2	None
PCI33, PCIX33, AGP1X33[3]	—	3.3	None
PCIX15	0.75	1.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
AGP2X33	1.32	—	None
HSTL18_I, II	0.9	1.8[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL18_III, IV	1.08	1.8[2]	None / V_{CCIO}: 50
HSTL15_I, II	0.75	1.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL15_III, IV	0.9	1.5[2]	None / V_{CCIO}: 50
SSTL33_I, II	1.5	3.3	None
SSTL25_I, II	1.25	2.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL18_I, II	0.9	1.8[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
GTL+, GTL	1.0 / 0.8	1.5 / 1.2[2]	None / V_{CCIO}: 50
Differential Interfaces			
SSTL18D_I, II	—	1.8[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL25D_I, II	—	2.5[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL33D_I, II	—	3.3	None
HSTL15D_I, II	—	1.5[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL18D_I, II	—	1.8[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
LVDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240
Mini-LVDS	—	—	None / Diff: 120, 150 / Diff to V_{CMT}: 120, 150
BLVDS25	—	—	None
MLVDS25	—	—	None
RSDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240
LVPECL33	—	≤2.5	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240

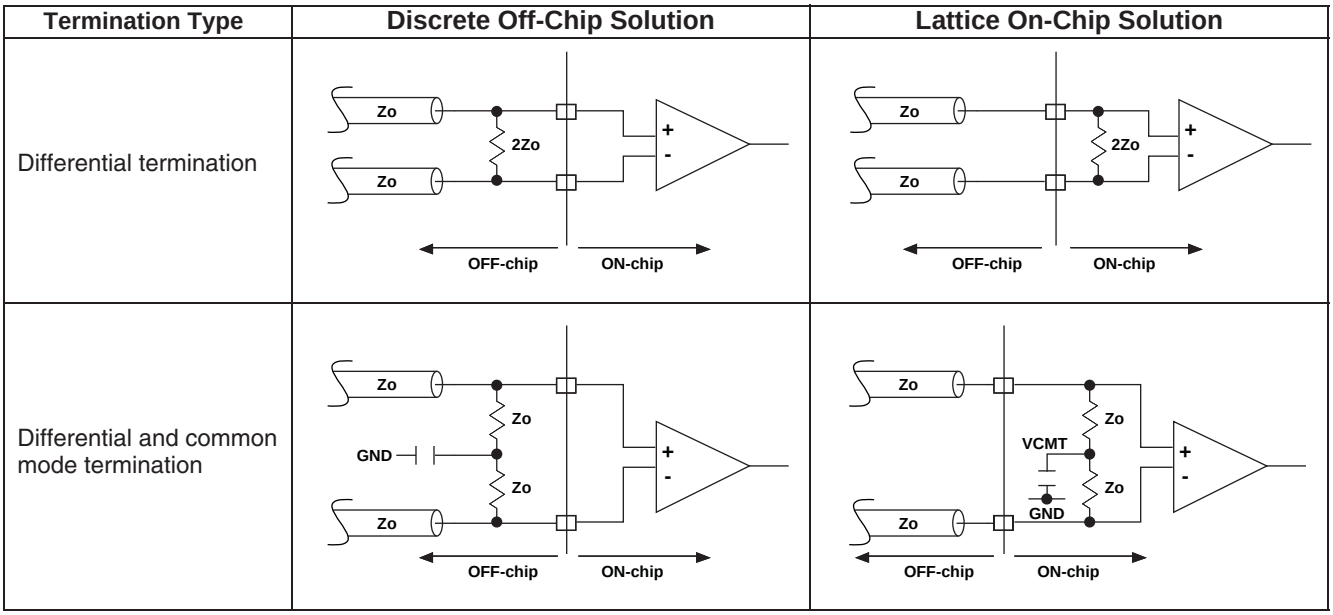
1. When not specified V_{CCIO} can be set anywhere in the valid operating range.
2. V_{CCIO} needed for on-chip termination to $V_{CCIO}/2$ or V_{CCIO} only. V_{CCIO} is not specified for off-chip termination or V_{TT} termination.
3. All ratioed input buffers and dedicated pin input buffers include hysteresis with a typical value of 50mV.

Differential Input Termination

The LatticeSC device allows two types of differential termination. The first is a single resistor across the differential inputs. The second is a center-tapped system where each input is terminated to the on-chip termination bus V_{CMT}. The V_{CMT} bus is DC-coupled through an internal capacitor to ground.

Figure 2-29 shows the differential termination schemes and Table 2-9 shows the nominal values of the termination resistors.

Figure 2-29. Differential Termination Scheme



Calibration

There are two calibration sources that are associated with the termination scheme used in the LatticeSC devices:

- DIFFR – This pin occurs in each bank that supports differential drivers and must be connected through a 1K+/-1% resistor to ground if differential outputs are used. Note that differential drivers are not supported in banks 1, 4 and 5.
- XRES – There is one of these pins per device. It is used for several functions including calibrating on-chip termination. This pin should always be connected through a 1K+/-1% resistor to ground.

The LatticeSC devices support two modes of calibration:

- Continuous – In this mode the SC devices continually calibrate the termination resistances. Calibration happens several times a second. Using this mode ensures that termination resistances remain calibrated as the silicon junction temperature changes.
- User Request – In this mode the calibration circuit operates continuously. However, the termination resistor values are only updated on the assertion of the calibration_update signal available to the core logic.

For more information on calibration, refer to the details of additional technical documentation at the end of this data sheet.

Hot Socketing

The LatticeSC devices have been carefully designed to ensure predictable behavior during power-up and power-down. To ensure proper power sequencing, care must be taken during power-up and power-down as described below. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits,

Power Supply Ramp Rates

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
t_{RAMP}	Power supply ramp rates for all power supplies	Over process, voltage, temperature	3.45	—	—	mV/µs
			—	—	75	ms

1. See the Power-up and Power-Down requirements section for more details on power sequencing.
2. From 0.5V to minimum operating voltage.

Hot Socketing Specifications[1]

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Programmable and dedicated Input or I/O leakage current[2, 3, 4, 5, 6]	0 <= V_{IN} <= V_{IH} (MAX)	—	—	±1500	µA
I_{HDIN}	SERDES average input current when device powered down and inputs driven[7]		—	—	4	mA

1. See Hot Socket power up/down information in Chapter 2 of this document.
2. Assumes monotonic rise/fall rates for all power supplies.
3. Sensitive to power supply sequencing as described in hot socketing section.
4. Assumes power supplies are between 0 and maximum recommended operations conditions.
5. IDK is additive to I_{PU}, I_{PD} or I_{BH}.
6. Represents DC conditions. For the first 20ns after hot insertion, current specification is 8 mA.
7. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed VDDOB of 1.575V, 8b/10b data and internal AC coupling.

DC Electrical Characteristics[5]

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.[3]	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low leakage	0 ≤ V_{IN} ≤ V_{IH} (MAX)	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	0 ≤ V_{IN} ≤ 0.7 V_{CCIO}	-30	—	-210	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) ≤ V_{IN} ≤ V_{IH} (MAX)	30	—	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7V_{CCIO}	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ≤ V_{IN} ≤ V_{IH} (MAX)	—	—	210	µA
I_{BHLH}	Bus Hold High Overdrive Current	0 ≤ V_{IN} ≤ V_{IH} (MAX)	—	—	-210	µA
I_{CL}	PCI Low Clamp Current	-3 < V_{IN} ≤ -1	-25 + (V_{IN} + 1)/0.015	—	—	mA
I_{CH}	PCI High Clamp Current	V_{CC} + 4 > V_{IN} ≥ V_{CC} + 1	25 + (V_{IN} - V_{CC} -1)/ 0.015	—	—	mA
V_{BHT}	Bus Hold trip Points	0 ≤ V_{IN} ≤ V_{IH} (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{CCIP2} = 1.2V, V_{CCAUX} = 2.5, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C3[2]	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{CCIP2} = 1.2V, V_{CCAUX} = 2.5, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. I_{PU}, I_{PD}, I_{BHLS} and I_{BHHS} have minimum values of 15 or -15µA if V_{CCIO} is set to 1.2V nominal.
4. This table does not apply to SERDES pins.
5. For programmable I/Os.

RSDS

Over Recommended Operating Conditions

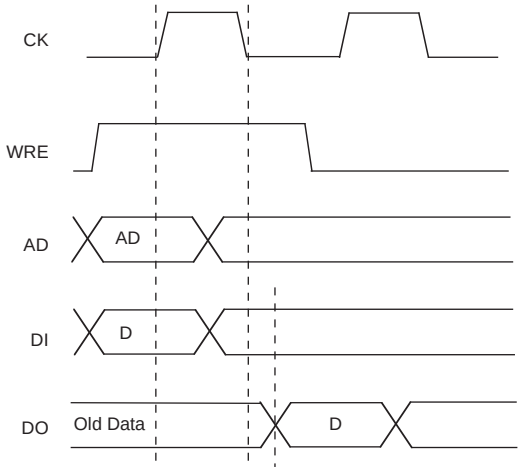
Parameter Symbol	Description	Min.	Typ.	Max.	Units
V_{OD}	Output voltage, differential, R_T = 100 ohms	100	200	600	mV
V_{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I_{RSDS}	Differential driver output current	1	2	6	mA
V_{THD}	Input voltage differential	100	—	—	mV
V_{CM}	Input common mode voltage	0.3	—	1.5	V
T_R, T_F	Output rise and fall times, 20% to 80%	—	500	—	ps
T_{ODUTY}	Output clock duty cycle	45	50	55	%

Note: Data is for 2mA drive. Other differential driver current options are available.

Timing Diagrams

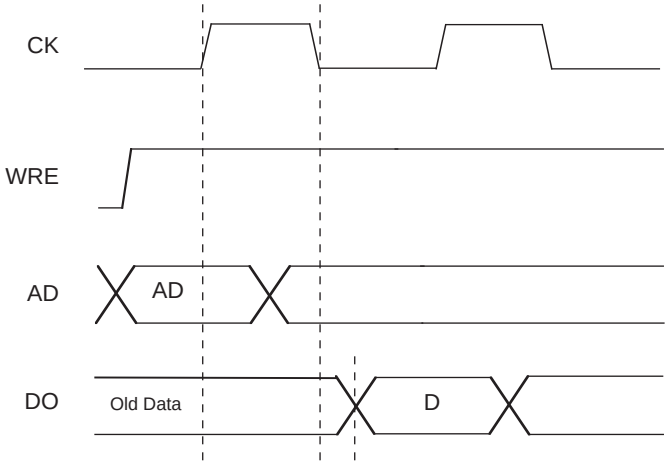
PFU Timing Diagrams

Figure 3-4. Slice Single/Dual Port Write Cycle Timing



Notes:
- Rising Edge for latching WREN, WAD and DATAIN.
- WREN must continue past falling edge clock.
- Data output occurs on negative edge.

Figure 3-5. Slice Single/Dual Port Read Cycle Timing

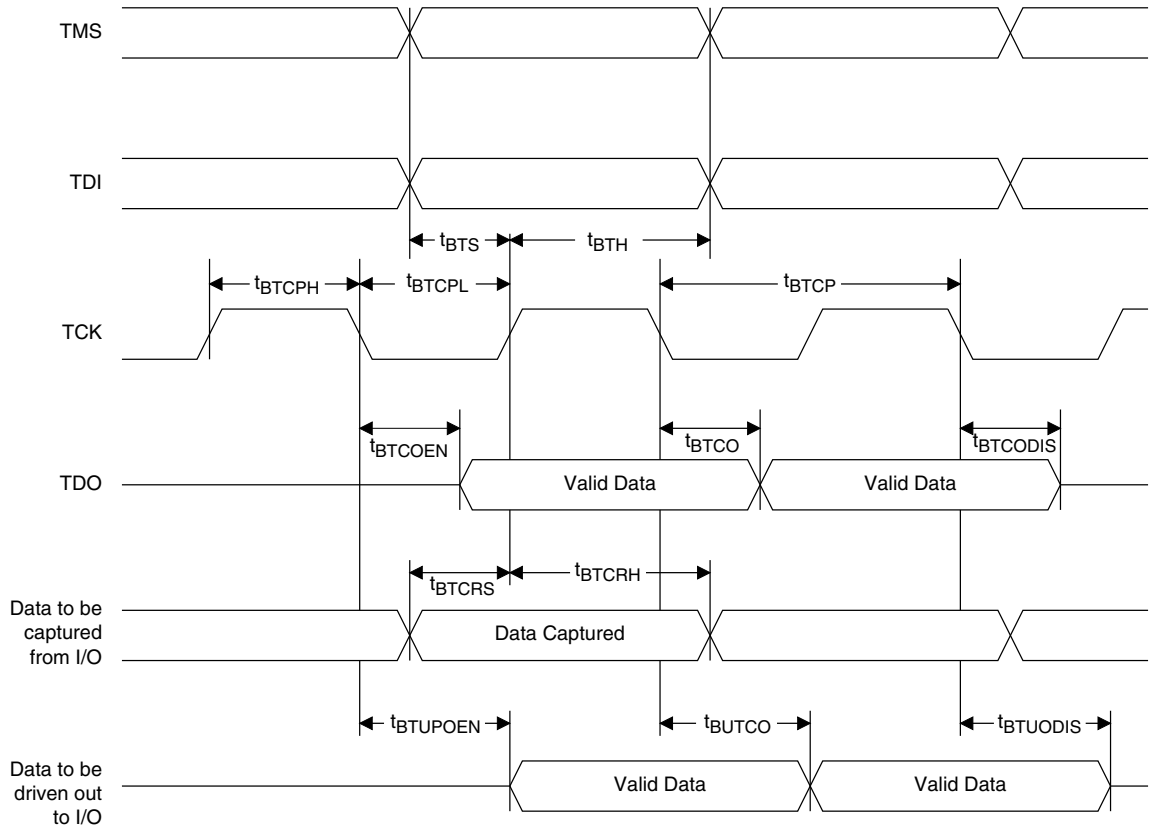


JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	10	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	10	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	25	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	25	ns

Figure 3-14. JTAG Port Timing Waveforms



Signal Descriptions (Cont.)

Signal Name	I/O	Description
RESETN		Reset. (Also sent to general routing). During configuration it resets the configuration state machine. After configuration this pin can perform the global set/reset (GSR) functions or can be used as a general input pin.
CFGIRQN	O	MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins.
TSALLN	I	Tristates all I/O.
Configuration Pads (User I/O if not used. Used during sysCONFIG.)		
HDC/SI	O	High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete. For SPI modes, this pin is used to download the read command and initial read address into the Flash memory device on the falling edge of SCK. This pin will be connected to SI of the memory. If the SPI mode is used, the 8-bit instruction code 0x03 will be downloaded followed by a 24-bit starting address of 0x000000 or a non-zero stat address for partial reconfiguration. If the SPIX mode has been selected, the 8-bit instruction captured on D[7:0] at power-up will be shifted in and followed by a 32-bit starting address of 0x000000.
LDCN/SCS	O	Low During Configuration is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete. For SPI modes, this is an active low chip select for Flash memories. It will go active after INITN goes high but before SCK begins. During power up LDCN will be low. Once INITN goes high, LDCN will go high for 100ns-200ns after which time it will go back low and configuration can begin. During the 100ns-200ns period, the read instruction will be latched for SPIX mode.
DOUT	O	Serial data output that can drive the D0/DIN of daisy-chained slave devices. The data-stream from this output will propagate preamble bits of the bitstream to daisy-chained devices. Data out on DOUT changes on the rising edge of CCLK.
QOUT/CEON	O	During daisy-chaining configuration, QOUT is the serial data output that can drive the D0/DIN of daisy-chained slave devices that do not propagate preamble bits. Data out on QOUT changes on the rising edge of CCLK. During parallel-chaining configuration, active low CEON enables the cascaded slave device to receive bitstream data.
RDN	I	Used in the asynchronous peripheral configuration mode. A low on RDN changes D[7:3] into status outputs. WRN and RDN should not be used simultaneously. If they are, the write strobe overrides.
WRN	I	When the FPGA is selected, a low on the write strobe, WRN, loads the data on D[7:0] inputs into an internal data buffer.
CS0N CS1	I	Used in the asynchronous peripheral, slave parallel and MPI modes. The FPGA is selected when CS0N is low and CS1 is high. During configuration, a pull-up is enabled on both except with MPI DMA access control.
A[21:0]	I/O	In master parallel mode, A[21:0] is an output and will address the configuration EPROMs up to 4 MB space. For MPI configuration mode, A[17:0] will be the MPI address MPI_ADDR[31:14], A[19:18] will be the transfer size and A[21:20] will be the burst mode and burst in process.

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L33	PL27B	7		PL35B	7	
M30	PL27C	7		PL35C	7	
N30	PL27D	7		PL35D	7	
M31	PL29A	7		PL37A	7	
N31	PL29B	7		PL37B	7	
P24	PL29C	7		PL37C	7	
R24	PL29D	7		PL37D	7	
M33	PL30A	7		PL42A	7	
N33	PL30B	7		PL42B	7	
U25	PL30C	7		PL42C	7	
T25	PL30D	7		PL42D	7	
L34	PL31A	7		PL43A	7	
M34	PL31B	7		PL43B	7	
P29	PL31C	7		PL43C	7	
R29	PL31D	7		PL43D	7	
N34	PL34A	7		PL46A	7	
P34	PL34B	7		PL46B	7	
R27	PL34C	7		PL46C	7	
T27	PL34D	7		PL46D	7	
R32	PL35A	7	PCLKT7_1	PL47A	7	PCLKT7_1
R31	PL35B	7	PCLKC7_1	PL47B	7	PCLKC7_1
U24	PL35C	7	PCLKT7_3	PL47C	7	PCLKT7_3
T24	PL35D	7	PCLKC7_3	PL47D	7	PCLKC7_3
P33	PL36A	7	PCLKT7_0	PL48A	7	PCLKT7_0
R33	PL36B	7	PCLKC7_0	PL48B	7	PCLKC7_0
T26	PL36C	7	PCLKT7_2	PL48C	7	PCLKT7_2
U26	PL36D	7	PCLKC7_2	PL48D	7	PCLKC7_2
T32	PL38A	6	PCLKT6_0	PL50A	6	PCLKT6_0
T31	PL38B	6	PCLKC6_0	PL50B	6	PCLKC6_0
U29	PL38C	6	PCLKT6_1	PL50C	6	PCLKT6_1
V29	PL38D	6	PCLKC6_1	PL50D	6	PCLKC6_1
T30	PL39A	6		PL51A	6	
U30	PL39B	6		PL51B	6	
U27	PL39C	6	PCLKT6_3	PL51C	6	PCLKT6_3
V27	PL39D	6	PCLKC6_3	PL51D	6	PCLKC6_3
R34	PL40A	6		PL52A	6	
T34	PL40B	6		PL52B	6	
U28	PL40C	6	PCLKT6_2	PL52C	6	PCLKT6_2
V28	PL40D	6	PCLKC6_2	PL52D	6	PCLKC6_2
V30	PL43A	6		PL55A	6	
W30	PL43B	6		PL55B	6	
W27	PL43C	6	VREF1_6	PL55C	6	VREF1_6
Y27	PL43D	6		PL55D	6	
T33	PL44A	6		PL56A	6	
U33	PL44B	6		PL56B	6	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG18	PB42C	5		PB61C	5	
AF18	PB42D	5		PB61D	5	
AP19	PB43A	5		PB63A	5	
AP18	PB43B	5		PB63B	5	
AJ18	PB43C	5		PB63C	5	
AH18	PB43D	5		PB63D	5	
AP17	PB45A	4		PB65A	4	
AP16	PB45B	4		PB65B	4	
AJ17	PB45C	4		PB65C	4	
AH17	PB45D	4		PB65D	4	
AN17	PB46A	4		PB66A	4	
AN16	PB46B	4		PB66B	4	
AE17	PB46C	4		PB66C	4	
AD17	PB46D	4		PB66D	4	
AK17	PB47A	4		PB67A	4	
AK16	PB47B	4		PB67B	4	
AG17	PB47C	4		PB67C	4	
AF17	PB47D	4		PB67D	4	
AM16	PB49A	4		PB69A	4	
AM15	PB49B	4		PB69B	4	
AJ15	PB49C	4		PB69C	4	
AJ14	PB49D	4		PB69D	4	
AL16	PB50A	4		PB70A	4	
AL15	PB50B	4		PB70B	4	
AG16	PB50C	4		PB70C	4	
AF16	PB50D	4		PB70D	4	
AP15	PB51A	4		PB71A	4	
AP14	PB51B	4		PB71B	4	
AH15	PB51C	4		PB71C	4	
AH14	PB51D	4		PB71D	4	
AN15	PB53A	4	PCLKT4_2	PB74A	4	PCLKT4_2
AN14	PB53B	4	PCLKC4_2	PB74B	4	PCLKC4_2
AE16	PB53C	4	PCLKT4_7	PB74C	4	PCLKT4_7
AD16	PB53D	4	PCLKC4_7	PB74D	4	PCLKC4_7
AK15	PB54A	4	PCLKT4_1	PB75A	4	PCLKT4_1
AK14	PB54B	4	PCLKC4_1	PB75B	4	PCLKC4_1
AG15	PB54C	4	PCLKT4_6	PB75C	4	PCLKT4_6
AG14	PB54D	4	PCLKC4_6	PB75D	4	PCLKC4_6
AM13	PB55A	4	PCLKT4_0	PB77A	4	PCLKT4_0
AM12	PB55B	4	PCLKC4_0	PB77B	4	PCLKC4_0
AJ12	PB55C	4	VREF2_4	PB77C	4	VREF2_4
AJ11	PB55D	4		PB77D	4	
AL13	PB57A	4	PCLKT4_5	PB79A	4	PCLKT4_5
AL12	PB57B	4	PCLKC4_5	PB79B	4	PCLKC4_5
AH12	PB57C	4		PB79C	4	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB57D	4		PB79D	4	
AN13	PB58A	4	PCLKT4_3	PB80A	4	PCLKT4_3
AN12	PB58B	4	PCLKC4_3	PB80B	4	PCLKC4_3
AD14	PB58C	4	PCLKT4_4	PB80C	4	PCLKT4_4
AD15	PB58D	4	PCLKC4_4	PB80D	4	PCLKC4_4
AP13	PB61A	4		PB73A	4	
AP12	PB61B	4		PB73B	4	
AK13	PB61C	4		PB73C	4	
AK12	PB61D	4		PB73D	4	
AP11	PB62A	4		PB83A	4	
AP10	PB62B	4		PB83B	4	
AN11	PB63A	4		PB99A	4	
AN10	PB63B	4		PB99B	4	
AF14	PB63C	4		PB99C	4	
AF13	PB63D	4		PB99D	4	
AM10	PB67A	4		PB101A	4	
AM9	PB67B	4		PB101B	4	
AE14	PB67C	4		PB101C	4	
AE13	PB67D	4		PB101D	4	
AP9	PB69A	4		PB104A	4	
AP8	PB69B	4		PB104B	4	
AK11	PB69C	4		PB104C	4	
AK10	PB69D	4		PB104D	4	
AL10	PB70A	4		PB107A	4	
AL9	PB70B	4		PB107B	4	
AF12	PB70C	4		PB107C	4	
AF11	PB70D	4		PB107D	4	
AN9	PB73A	4		PB109A	4	
AN8	PB73B	4		PB109B	4	
AG11	PB73C	4		PB109C	4	
AG10	PB73D	4		PB109D	4	
AP7	PB74A	4		PB111A	4	
AP6	PB74B	4		PB111B	4	
AG13	PB74C	4		PB111C	4	
AG12	PB74D	4		PB111D	4	
AN7	PB75A	4		PB113A	4	
AN6	PB75B	4		PB113B	4	
AK9	PB75C	4		PB113C	4	
AK8	PB75D	4		PB113D	4	
AP5	PB77A	4		PB115A	4	
AP4	PB77B	4		PB115B	4	
AD11	PB77C	4		PB115C	4	
AE11	PB77D	4		PB115D	4	
AM7	PB78A	4		PB117A	4	
AM6	PB78B	4		PB117B	4	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C32	VCC12	-		VCC12	-	
E34	NC	-		PL22A	7	
F34	NC	-		PL22B	7	
F33	NC	-		PL24A	7	
G33	NC	-		PL24B	7	
K30	NC	-		PL25A	7	
L30	NC	-		PL25B	7	
G34	NC	-		PL26A	7	
H34	NC	-		PL26B	7	
M32	NC	-		PL39A	7	
N32	NC	-		PL39B	7	
P28	NC	-		PL39C	7	
R28	NC	-		PL39D	7	
J34	NC	-		PL41A	7	
K34	NC	-		PL41B	7	
P30	NC	-		PL41C	7	
R30	NC	-		PL41D	7	
W34	NC	-		PL59A	6	
Y34	NC	-		PL59B	6	
W32	NC	-		PL61A	6	
Y32	NC	-		PL61B	6	
AA34	NC	-		PL64A	6	
AB34	NC	-		PL64B	6	
AC34	NC	-		PL67A	6	
AD34	NC	-		PL67B	6	
Y30	NC	-		PL68A	6	
AA30	NC	-		PL68B	6	
AB33	NC	-		PL69A	6	
AC33	NC	-		PL69B	6	
AC2	NC	-		PR69B	3	
AB2	NC	-		PR69A	3	
AA5	NC	-		PR68B	3	
Y5	NC	-		PR68A	3	
AD1	NC	-		PR67B	3	
AC1	NC	-		PR67A	3	
AB1	NC	-		PR64B	3	
AA1	NC	-		PR64A	3	
Y3	NC	-		PR61B	3	
W3	NC	-		PR61A	3	
Y1	NC	-		PR59B	3	
W1	NC	-		PR59A	3	
R5	NC	-		PR41D	2	
P5	NC	-		PR41C	2	
K1	NC	-		PR41B	2	
J1	NC	-		PR41A	2	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
R7	NC	-		PR39D	2	
P7	NC	-		PR39C	2	
N3	NC	-		PR39B	2	
M3	NC	-		PR39A	2	
H1	NC	-		PR26B	2	
G1	NC	-		PR26A	2	
L5	NC	-		PR25B	2	
K5	NC	-		PR25A	2	
G2	NC	-		PR24B	2	
F2	NC	-		PR24A	2	
F1	NC	-		PR22B	2	
E1	NC	-		PR22A	2	
A2	GND	-		GND	-	
A33	GND	-		GND	-	
AA15	GND	-		GND	-	
AA20	GND	-		GND	-	
AA32	GND	-		GND	-	
AA4	GND	-		GND	-	
AB28	GND	-		GND	-	
AB6	GND	-		GND	-	
AC11	GND	-		GND	-	
AC18	GND	-		GND	-	
AC25	GND	-		GND	-	
AD23	GND	-		GND	-	
AD3	GND	-		GND	-	
AD31	GND	-		GND	-	
AE12	GND	-		GND	-	
AE15	GND	-		GND	-	
AE29	GND	-		GND	-	
AE7	GND	-		GND	-	
AE9	GND	-		GND	-	
AF20	GND	-		GND	-	
AF26	GND	-		GND	-	
AG32	GND	-		GND	-	
AG4	GND	-		GND	-	
AH13	GND	-		GND	-	
AH19	GND	-		GND	-	
AH25	GND	-		GND	-	
AH7	GND	-		GND	-	
AJ10	GND	-		GND	-	
AJ16	GND	-		GND	-	
AJ22	GND	-		GND	-	
AJ28	GND	-		GND	-	
AK3	GND	-		GND	-	
AK31	GND	-		GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AD5	PR94C	3	
AE2	PR94B	3	
AD2	PR94A	3	
AC5	PR92D	3	
AB5	PR92C	3	
AF1	PR92B	3	
AE1	PR92A	3	
AA11	PR91D	3	
Y11	PR91C	3	
AC4	PR91B	3	
AB4	PR91A	3	
AA8	PR90D	3	DIFFR_3
AA9	PR90C	3	
AC3	PR90B	3	
AB3	PR90A	3	
AA7	PR79D	3	
Y7	PR79C	3	
AA2	PR79B	3	
Y2	PR79A	3	
AA6	PR77D	3	
Y6	PR77C	3	
Y4	PR77B	3	
W4	PR77A	3	
W11	PR74D	3	
V11	PR74C	3	
W2	PR74B	3	
V2	PR74A	3	
W9	PR71D	3	
V9	PR71C	3	
V1	PR71B	3	
U1	PR71A	3	
W10	PR70D	3	
V10	PR70C	3	
U2	PR70B	3	
T2	PR70A	3	
Y8	PR69D	3	
W8	PR69C	3	VREF1_3
W5	PR69B	3	
V5	PR69A	3	
V7	PR66D	3	PCLKC3_2
U7	PR66C	3	PCLKT3_2
T1	PR66B	3	
R1	PR66A	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J17	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT81B	1	MCA_CLK_P1_OUT
E16	PT81A	1	MCA_CLK_P1_IN
H15	PT78D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT78C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT78B	1	MCA_CLK_P2_OUT
C16	PT78A	1	MCA_CLK_P2_IN
L17	PT75D	1	MCA_DONE_OUT
K17	PT75C	1	BUSYN/RCLK/SCK
E17	PT75B	1	DP0/MPI_PAR0
F17	PT75A	1	MPI_TA
G17	PT73D	1	D23/MPI_DATA23
H17	PT73C	1	DP2/MPI_PAR2
A17	PT73B	1	PCLKC1_0
B17	PT73A	1	PCLKT1_0/MPI_CLK
G18	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT71C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT71B	1	MPI_RETRY
F18	PT71A	1	A0/MPI_ADDR14
J18	PT69D	1	A1/MPI_ADDR15
J19	PT69C	1	A2/MPI_ADDR16
C20	PT69B	1	A3/MPI_ADDR17
C19	PT69A	1	A4/MPI_ADDR18
K18	PT66D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT66C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT66B	1	A5/MPI_ADDR19
E19	PT66A	1	A6/MPI_ADDR20
H19	PT63D	1	D27/MPI_DATA27
H20	PT63C	1	VREF1_1
A18	PT63B	1	A7/MPI_ADDR21
B18	PT63A	1	A8/MPI_ADDR22
H21	PT61D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT61C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT61B	1	A9/MPI_ADDR23
B19	PT61A	1	A10/MPI_ADDR24
H22	PT58D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT58C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT58B	1	A11/MPI_ADDR25
G20	PT58A	1	A12/MPI_ADDR26
K21	PT57D	1	D11/MPI_DATA11
K22	PT57C	1	D12/MPI_DATA12
A20	PT57B	1	A13/MPI_ADDR27
B20	PT57A	1	A14/MPI_ADDR28

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
K26	GND	-	
K28	GND	-	
K6	GND	-	
K9	GND	-	
L12	GND	-	
L32	GND	-	
L4	GND	-	
M10	GND	-	
M17	GND	-	
M24	GND	-	
N29	GND	-	
N7	GND	-	
P15	GND	-	
P20	GND	-	
P3	GND	-	
P31	GND	-	
R10	GND	-	
R14	GND	-	
R16	GND	-	
R19	GND	-	
R21	GND	-	
R26	GND	-	
T15	GND	-	
T17	GND	-	
T18	GND	-	
T20	GND	-	
T28	GND	-	
T6	GND	-	
U16	GND	-	
U19	GND	-	
U23	GND	-	
U32	GND	-	
U4	GND	-	
V12	GND	-	
V16	GND	-	
V19	GND	-	
V3	GND	-	
V31	GND	-	
W15	GND	-	
W17	GND	-	
W18	GND	-	
W20	GND	-	
W29	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AU9	PB103C	4		PB117C	4	
AU8	PB103D	4		PB117D	4	
AY8	PB104A	4		PB118A	4	
AY7	PB104B	4		PB118B	4	
AU7	PB104C	4		PB118C	4	
AU6	PB104D	4		PB118D	4	
BA7	PB105A	4		PB119A	4	
BA6	PB105B	4		PB119B	4	
AN13	PB105C	4		PB119C	4	
AN12	PB105D	4		PB119D	4	
AV9	PB107A	4		PB121A	4	
AV8	PB107B	4		PB121B	4	
AT10	PB107C	4		PB121C	4	
AT9	PB107D	4		PB121D	4	
AW8	PB108A	4		PB122A	4	
AW7	PB108B	4		PB122B	4	
AP11	PB108C	4		PB122C	4	
AP10	PB108D	4		PB122D	4	
BB5	PB109A	4		PB123A	4	
BB4	PB109B	4		PB123B	4	
AR10	PB109C	4		PB123C	4	
AR9	PB109D	4		PB123D	4	
BA5	PB111A	4		PB125A	4	
BA4	PB111B	4		PB125B	4	
AT7	PB111C	4		PB125C	4	
AT6	PB111D	4		PB125D	4	
BB3	PB112A	4		PB126A	4	
BA3	PB112B	4		PB126B	4	
AM14	PB112C	4		PB126C	4	
AL14	PB112D	4		PB126D	4	
AY5	PB113A	4		PB127A	4	
AY4	PB113B	4		PB127B	4	
AN11	PB113C	4		PB127C	4	
AN10	PB113D	4		PB127D	4	
AV7	PB115A	4		PB129A	4	
AV6	PB115B	4		PB129B	4	
AM12	PB115C	4		PB129C	4	
AM11	PB115D	4		PB129D	4	
AW5	PB116A	4		PB130A	4	
AW4	PB116B	4		PB130B	4	
AT5	PB116C	4		PB130C	4	
AT4	PB116D	4		PB130D	4	
AY2	PB117A	4		PB131A	4	
BA2	PB117B	4		PB131B	4	
AP9	PB117C	4		PB131C	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM27	GND	-		GND	-	
AM36	GND	-		GND	-	
AM7	GND	-		GND	-	
AP4	GND	-		GND	-	
AP40	GND	-		GND	-	
AR14	GND	-		GND	-	
AR20	GND	-		GND	-	
AR23	GND	-		GND	-	
AR29	GND	-		GND	-	
AR35	GND	-		GND	-	
AR8	GND	-		GND	-	
AT11	GND	-		GND	-	
AT17	GND	-		GND	-	
AT26	GND	-		GND	-	
AT32	GND	-		GND	-	
AU3	GND	-		GND	-	
AU39	GND	-		GND	-	
AW12	GND	-		GND	-	
AW18	GND	-		GND	-	
AW22	GND	-		GND	-	
AW28	GND	-		GND	-	
AW34	GND	-		GND	-	
AW6	GND	-		GND	-	
AY15	GND	-		GND	-	
AY21	GND	-		GND	-	
AY25	GND	-		GND	-	
AY31	GND	-		GND	-	
AY37	GND	-		GND	-	
AY9	GND	-		GND	-	
B1	GND	-		GND	-	
B42	GND	-		GND	-	
BA1	GND	-		GND	-	
BA42	GND	-		GND	-	
BB2	GND	-		GND	-	
BB41	GND	-		GND	-	
C10	GND	-		GND	-	
C12	GND	-		GND	-	
C13	GND	-		GND	-	
C16	GND	-		GND	-	
C18	GND	-		GND	-	
C19	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C27	GND	-		GND	-	
C28	GND	-		GND	-	

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-6FCN1152I[2]	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FCN1152I[2]	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-6FCN1152I[1]	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-5FCN1152I[1]	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-6FCN1704I[1]	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-5FCN1704I[1]	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSC3GA80E-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-6FCN1152I[1]	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FCN1152I[1]	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FCN1704I[1]	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FCN1704I[1]	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.