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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	476
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFcBGA Rev 2 (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga25e-6ffan1020c

DLLs and dynamic glitch free clock MUXs which are required in today's high end system designs. High-speed, high-bandwidth I/O make this family ideal for high-throughput systems.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeSC family of FPGA devices. Synthesis library support for LatticeSC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeSC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeSC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Innovative high-performance FPGA architecture, high-speed SERDES with PCS support, sysMEM embedded memory and high performance I/O are combined in the LatticeSC to provide excellent performance for today's leading edge systems designs. Table 1-3 details the performance of several common functions implemented within the LatticeSC.

Table1-3. Speed Performance for Typical Functions¹

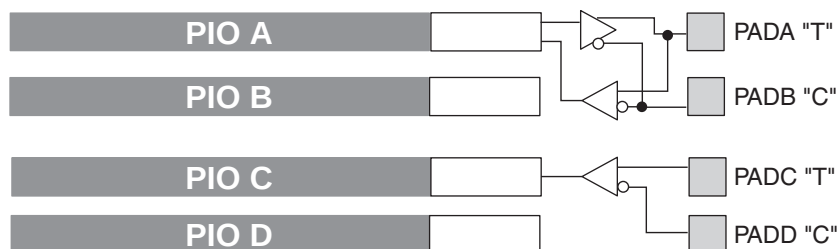
Functions	Performance (MHz) ²
32-bit Address Decoder	539
64-bit Address Decoder	517
32:1 Multiplexer	779
64-bit Adder (ripple)	353
32x8 Distributed Single Port (SP) RAM	768
64-bit Counter (up or down counter, non-loadable)	369
True Dual-Port 1024x18 bits	372
FIFO Port A: x36 bits, B: x9 bits	375

1. For additional information, see Typical Building BLock Function Performance table in this data sheet.

2. Advance information (-7 speed grade).

high-speed interfaces in the LatticeSC devices. Figure 2-18 shows how differential receivers and drivers are arranged between PIOs.

Figure 2-18. Differential Drivers and Receivers



*Differential Driver only available on right and left of the device.

PIO

The PIO contains five blocks: an input register block, output register block, tristate register block, update block, and a control logic block. These blocks contain registers for both single data rate (SDR), double data rate (DDR), and shift register operation along with the necessary clock and selection logic.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 show the diagram of the input register block. The signal from the PURE-SPEED I/O buffer (DI) enters the input register block and can be used for three purposes, as a source for the combinatorial (INDD) and clock outputs (INCK), the input into the SDR register/latch block and the input to the delay block. The output of the delay block can be used as combinatorial (INDD) and clock (INCK) outputs, an input to the DDR/Shift Register Block or an input into the SDR register block.

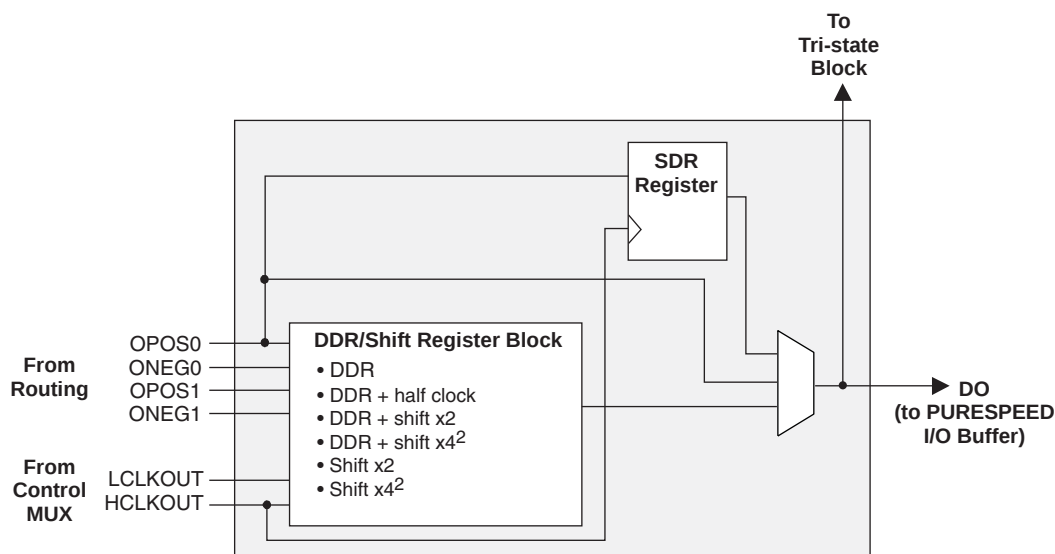
Input SDR Register/Latch Block

The SDR register/latch block has a latch and a register/latch that can be used in a variety of combinations to provide a registered or latched output (INFF). The latch operates off high-speed input clocks and latches data on the positive going edge. The register/latch operates off the low-speed input clock and registers/latches data on the positive going edge. Both the latch and the register/latch have a clock enable input that is driven by the input clock enable. In addition both have a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register and latch LSR inputs are driven from LSRI, which is generated from the PIO control MUX. The GSR inputs are driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

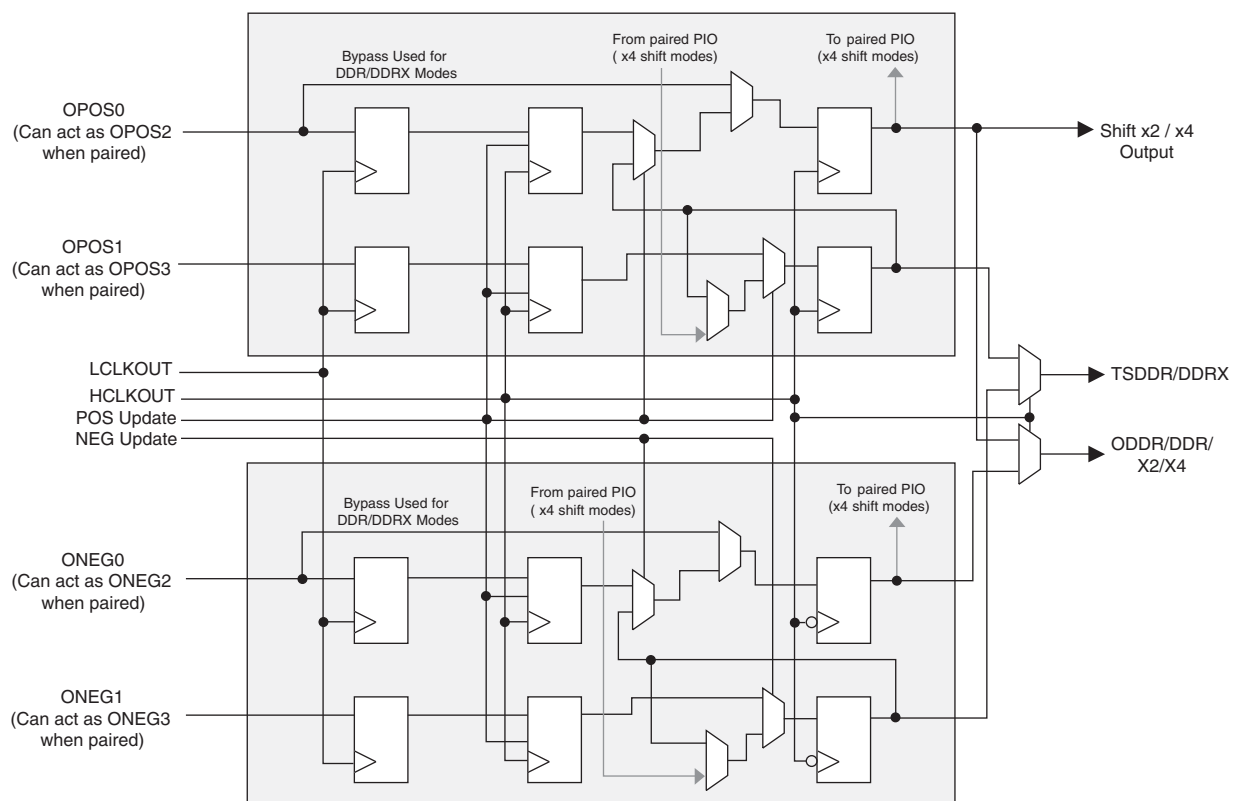
Input Delay Block

The delay block uses 144 tapped delay lines to obtain coarse and fine delay resolution. These delays can be adjusted during configuration or automatically via DLL or AIL blocks. The Adaptive Input Logic (AIL) uses this delay block to adjust automatically the delay in the data path to ensure that it has sufficient setup and hold time.

The delay line in this block matches the delay line that is used in the 12 on-chip DLLs. The delay line can be set via configuration bits or driven from a calibration bus that allows the setting to be controlled either from one of the on-chip DLLs or user logic. Controlling the delay from one of the on-chip DLLs allow the delay to be calibrated to the DLL clock and hence compensated for the variations in process, voltage and temperature.

Figure 2-22. Output Register Block¹**Notes:**

1. CE, Update, Set and Reset not shown for clarity.
2. By four shift modes utilizes DDR/Shift register block from paired PIO.
3. DDR/Shift register block shared with tristate block.

Figure 2-23. Output/Tristate DDR/Shift Register Block

flexiPCS quads are not dedicated solely to industry standard protocols. Each quad (and each channel within a quad) can be programmed for many user defined data manipulation modes. For example, modes governing user-defined word alignment and multi-channel alignment can be programmed for non-standard protocol applications.

For more information on the functions and use of the flexiPCS, refer to the [LatticeSC/M Family flexiPCS Data Sheet](#).

System Bus

Each LatticeSC device connects the FPGA elements with a standardized bus framework referred to as a System Bus. Multiple bus masters optimize system performance by sharing resources between different bus masters such as the MPI and configuration logic. The wide data bus configuration of 32 bits with 4-bit parity supports high-bandwidth, data intensive applications.

There are two types of interfaces on the System Bus, master and slave. A master interface has the ability to perform actions on the bus, such as writes and reads to and from a specific address. A slave interface responds to the actions of a master by accepting data and address on a write and providing data on a read. The System Bus has a memory map which describes each of the slave peripherals that is connected on the bus. Using the addresses listed in the memory map, a master interface can access each of the slave peripherals on the System Bus. Any and all peripherals on the System Bus can be used at the same time. Table 2-12 list all of the available user peripherals on the System Bus after device power-up.

Table 2-12. System Bus User Peripherals

Peripheral	Name	Interface Type
Micro Processor Interface	MPI	Master
User Master Interface	UMI	Master
User Slave Interface	USI	Slave
Serial Management Interface (PLL, DLL, User Logic)	SMI	Slave
Physical Coding Sublayer	PCS	Slave
Direct FPGA Access	DFA	Slave

The peripherals listed in Table 2-12 can be added when the System Bus module is created using Module IP/Manager (ispLEVER Module/IP Manager).

Figure 2-31 also lists the existing peripherals on the System Bus. The gray boxes are available only during configuration. Refer to Lattice technical note TN1080, [LatticeSC sysCONFIG Usage Guide](#), for configuration options. The Status and Config box refers to internal System Bus registers. This document presents all the interfaces listed in Table 2-12 in detail to help the user utilize the desired functions of the System Bus.

Initialization and Standby Supply Current

The table below indicates initialization and standby supply current while operating at 85°C junction temperature (T_J), which is the high end of the commercial temperature range, and 105°C, which is the high end of the industrial temperature range. This data assumes all outputs are tri-stated and all inputs are configured as LVCMOS and held at V_{CCIO} or GND. The remaining SERDES supply current for V_{DDIB} and V_{DDOB} is detailed in the SERDES section of this data sheet. For power at your design temperature, it is recommended to use the Power Calculator tool which is accessible in ispLEVER or can be used as a standalone tool. For more information on supply current, see the reference to additional technical documentation available at the end of this data sheet.

Over Recommended Operating Conditions

Symbol	Condition	Parameter	Device	25°C Typ. ¹	85°C Max. ²		105°C Max. ²	Units
				All	-5, -6	-7	-5, -6	
I_{CC}	(VCC = 1.2V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	65	449	678	755	mA
			LFSC/M25	113	798	1255	1343	mA
			LFSC/M40	159	1178	2006	1981	mA
			LFSC/M80	276	2122	3827	3569	mA
			LFSC/M115	454	3376	—	5679	mA
	(VCC = 1.0V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	45	312	471	524	mA
			LFSC/M25	79	554	872	933	mA
			LFSC/M40	110	818	1393	1375	mA
			LFSC/M80	191	1473	2658	2478	mA
			LFSC/M115	315	2344	—	3943	mA
I_{CC12}		1.2V Power Supply Current for Configuration Logic, FPGA PLL, SERDES PLL and SERDES Analog Supplies	LFSC/M15	23	39	59	35	mA
			LFSC/M25	25	50	78	56	mA
			LFSC/M40	31	78	133	89	mA
			LFSC/M80	50	108	195	123	mA
			LFSC/M115	65	131	—	154	mA
I_{CCAUX}		Auxiliary Operating Power Supply Current	LFSC/M15	7	12	19	14	mA
			LFSC/M25	9	16	25	18	mA
			LFSC/M40	12	23	39	25	mA
			LFSC/M80	13	25	45	23	mA
			LFSC/M115	16	27	—	26	mA
I_{CCIO} and I_{CCJ}		Bank Power Supply Current (per bank)	LFSC/M15	0.1	0.2	0.3	0.2	mA
			LFSC/M25	0.3	0.6	1.0	0.7	mA
			LFSC/M40	0.4	0.9	1.5	1.0	mA
			LFSC/M80	0.5	1.1	2.1	1.3	mA
			LFSC/M115	0.7	1.5	—	1.8	mA

1. I_{CC} is specified at $T_J = 25^\circ\text{C}$ and typical V_{CC} .

2. I_{CC} is specified at the respective commercial and industrial maximum T_J and V_{CC} limits.

PURESPEED I/O Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V _{IL}		V _{IH}		V _{OL} Max. (V)	V _{OH} Min. (V)	I _{OL} (mA)	I _{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 33	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 25	-0.3	0.7	1.7	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 18	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 15	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 12	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.3	VCCIO - 0.3	12, 8, 4, 2	-12, -8, -4, -2
					0.2	VCCIO - 0.2	0.1	-0.1
PCIX15	-0.3	0.3VCCIO	0.5VCCIO	1.5	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCI33	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCIX33	-0.3	0.35VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
AGP-1X, AGP-2X	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
SSTL3_I	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.7	VCCIO - 1.1	8	-8
SSTS3_I OST ²	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 1.3	8	-8
SSTL3_II	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.5	VCCIO - 0.9	16	-16
SSTL3_II OST ²	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 0.13	16	-16
SSTL2_I	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.54	VCCIO - 0.62	7.6	-7.6
SSTL2_I OST ²	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	7.6	-7.6
SSTL2_II	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.35	VCCIO - 0.43	15.2	-15.2
SSTL2_II OST ²	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	15.2	-15.2
SSTL18_I	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
SSTL18_II	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
HSTL15_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	8	-8
HSTL15_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	16	-16
HSTL15_III ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL15_IV ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	9.6	-9.6
HSTL18_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	19.2	-19.2
HSTL18_III ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_IV ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
GTL12 ¹ , GTLPLUS15 ¹	-0.3	VREF - 0.2	VREF + 0.2	N/A	N/A	N/A	N/A	N/A

1. Input only.

2. Input with on-chip series termination.

Switching Characteristics

All devices are 100% functionally tested. Listed below are representative values of internal and external timing parameters. For more specific, more precise, and worst-case guaranteed data at a particular temperature and voltage, use the values reported by the static timing analyzer in the ispLEVER design tool from Lattice and back-annotate to the simulation net list.

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PIC row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
VREF1_x, VREF2_x	—	The reference supply pins for I/O bank x. Any I/O pin in a bank can be assigned as a reference supply pin, but software defaults use designated pin.
NC	—	No connect. NC pins should not be connected to any active signals, VCC or GND.
Non-SERDES Power Supplies		
VCCIOx	—	VCCIO - The power supply pins for I/O bank x. Dedicated pins.
VCC12 ¹	—	1.2V supply for configuration logic, PLLs and SERDES Rx, Tx and PLL. All VCC12 pins must be connected. As VCC12 supplies power for analog circuitry, VCC12 should be quiet and isolated from noisy digital board supplies.
VTT_x	—	Termination voltage for bank x. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.
GND	—	GND - Ground. Dedicated pins. All grounds must be electrically connected at the board level.
VCC	—	VCC - The power supply pins for core logic. Dedicated pins (1.2V/1.0V).
VCCAUX	—	VCCAUX - Auxiliary power supply pin - powers all differential and referenced input buffers. Dedicated pins (2.5V).
VCCJ	—	VCCJ - The power supply pin for JTAG Test Access Port.
PROBE_VCC	—	VCC signal - Connected to internal VCC node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D14	PT15B	1	A15/MPI_ADDR29	PT25B	1	A15/MPI_ADDR29
D13	PT15A	1	A17/MPI_ADDR31	PT25A	1	A17/MPI_ADDR31
F12	PT13D	1	A19/MPI_TSI21	PT24D	1	A19/MPI_TSI21
F13	PT13C	1	A20/MPI_BDIP	PT24C	1	A20/MPI_BDIP
B12	PT11B	1	A18/MPI_TSI20	PT24B	1	A18/MPI_TSI20
B11	PT11A	1	MPI_TEA	PT24A	1	MPI_TEA
E12	PT10D	1	D14/MPI_DATA14	PT23D	1	D14/MPI_DATA14
D12	PT10C	1	DP1/MPI_PAR1	PT23C	1	DP1/MPI_PAR1
G10	PT9B	1	A21/MPI_BURST	PT23B	1	A21/MPI_BURST
G9	PT9A	1	D15/MPI_DATA15	PT23A	1	D15/MPI_DATA15
C10	A_VDDIB3_L	-		A_VDDIB3_L	-	
E9	VCC12	-		VCC12	-	
B10	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
B9	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A10	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
D9	VCC12	-		VCC12	-	
A9	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
C9	A_VDDOB3_L	-		A_VDDOB3_L	-	
A8	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
C8	A_VDDOB2_L	-		A_VDDOB2_L	-	
A7	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E8	VCC12	-		VCC12	-	
B8	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
B7	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
C7	A_VDDIB2_L	-		A_VDDIB2_L	-	
D8	VCC12	-		VCC12	-	
C6	A_VDDIB1_L	-		A_VDDIB1_L	-	
E7	VCC12	-		VCC12	-	
B6	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
B5	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A6	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
D7	VCC12	-		VCC12	-	
A5	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
C5	A_VDDOB1_L	-		A_VDDOB1_L	-	
A4	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
C4	A_VDDOB0_L	-		A_VDDOB0_L	-	
A3	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E6	VCC12	-		VCC12	-	
B4	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
B3	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
C3	A_VDDIB0_L	-		A_VDDIB0_L	-	
D6	VCC12	-		VCC12	-	
L5	NC	-		PL21A	7	
M5	NC	-		PL21B	7	
G2	NC	-		PL20A	7	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ31	PB9A	5		PB9A	5	
AH30	PB9B	5		PB9B	5	
AM30	PB11A	5		PB11A	5	
AM29	PB11B	5		PB11B	5	
AH29	PB11C	5		PB11C	5	
AH28	PB11D	5		PB11D	5	
AJ27	PB12A	5		PB13A	5	
AK27	PB12B	5		PB13B	5	
AE22	PB12C	5		PB13C	5	
AF23	PB12D	5		PB13D	5	
AL28	PB13A	5		PB15A	5	
AL27	PB13B	5		PB15B	5	
AC21	PB13C	5		PB15C	5	
AD21	PB13D	5		PB15D	5	
AM28	PB15A	5		PB17A	5	
AM27	PB15B	5		PB17B	5	
AG23	PB15C	5		PB17C	5	
AF22	PB15D	5		PB17D	5	
AG26	PB16A	5		PB19A	5	
AG25	PB16B	5		PB19B	5	
AL26	PB17A	5		PB22A	5	
AM26	PB17B	5		PB22B	5	
AJ24	PB19A	5		PB25A	5	
AK24	PB19B	5		PB25B	5	
AE21	PB19C	5		PB25C	5	
AE20	PB19D	5		PB25D	5	
AJ22	PB20A	5	PCLKT5_3	PB30A	5	PCLKT5_3
AK22	PB20B	5	PCLKC5_3	PB30B	5	PCLKC5_3
AG22	PB20C	5	PCLKT5_4	PB30C	5	PCLKT5_4
AH22	PB20D	5	PCLKC5_4	PB30D	5	PCLKC5_4
AL23	PB21A	5	PCLKT5_5	PB31A	5	PCLKT5_5
AL22	PB21B	5	PCLKC5_5	PB31B	5	PCLKC5_5
AH23	PB21C	5		PB31C	5	
AH24	PB21D	5		PB31D	5	
AJ21	PB23A	5	PCLKT5_0	PB33A	5	PCLKT5_0
AK21	PB23B	5	PCLKC5_0	PB33B	5	PCLKC5_0
AE19	PB23C	5		PB33C	5	
AF19	PB23D	5	VREF2_5	PB33D	5	VREF2_5
AM23	PB24A	5	PCLKT5_1	PB34A	5	PCLKT5_1
AM22	PB24B	5	PCLKC5_1	PB34B	5	PCLKC5_1
AH25	PB24C	5	PCLKT5_6	PB34C	5	PCLKT5_6
AH26	PB24D	5	PCLKC5_6	PB34D	5	PCLKC5_6
AL21	PB25A	5	PCLKT5_2	PB35A	5	PCLKT5_2
AL20	PB25B	5	PCLKC5_2	PB35B	5	PCLKC5_2
AG20	PB25C	5	PCLKT5_7	PB35C	5	PCLKT5_7
AG19	PB25D	5	PCLKC5_7	PB35D	5	PCLKC5_7
AJ19	PB28A	5		PB37A	5	
AK19	PB28B	5		PB37B	5	
AD18	PB28C	5		PB37C	5	
AE18	PB28D	5		PB37D	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD8	PR65C	3		PR89C	3	
AJ3	PR65B	3		PR89B	3	
AH3	PR65A	3		PR89A	3	
AD7	PR62D	3		PR86D	3	
AC7	PR62C	3		PR86C	3	
AJ2	PR62B	3		PR86B	3	
AH2	PR62A	3		PR86A	3	
AF6	PR61D	3		PR85D	3	
AF5	PR61C	3		PR85C	3	
AF4	PR61B	3		PR85B	3	
AE4	PR61A	3		PR85A	3	
AD6	PR60D	3		PR84D	3	
AC6	PR60C	3		PR84C	3	
AG2	PR60B	3		PR84B	3	
AF2	PR60A	3		PR84A	3	
AC8	PR58D	3		PR82D	3	
AB8	PR58C	3		PR82C	3	
AK1	PR58B	3		PR82B	3	
AJ1	PR58A	3		PR82A	3	
AB10	PR57D	3		PR81D	3	
AA10	PR57C	3		PR81C	3	
AF3	PR57B	3		PR81B	3	
AE3	PR57A	3		PR81A	3	
AE5	PR56D	3		PR80D	3	
AD5	PR56C	3		PR80C	3	
AE2	PR56B	3		PR80B	3	
AD2	PR56A	3		PR80A	3	
AC5	PR53D	3		PR78D	3	
AB5	PR53C	3		PR78C	3	
AF1	PR53B	3		PR78B	3	
AE1	PR53A	3		PR78A	3	
AA11	PR52D	3		PR77D	3	
Y11	PR52C	3		PR77C	3	
AC4	PR52B	3		PR77B	3	
AB4	PR52A	3		PR77A	3	
AA8	PR51D	3	DIFFR_3	PR76D	3	DIFFR_3
AA9	PR51C	3		PR76C	3	
AC3	PR51B	3		PR76B	3	
AB3	PR51A	3		PR76A	3	
AA7	PR49D	3		PR65D	3	
Y7	PR49C	3		PR65C	3	
AA2	PR49B	3		PR65B	3	
Y2	PR49A	3		PR65A	3	
AA6	PR48D	3		PR63D	3	
Y6	PR48C	3		PR63C	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AJ34	PL98A	6	
AK34	PL98B	6	
AB27	PL98C	6	
AC27	PL98D	6	
AF33	PL99A	6	
AG33	PL99B	6	
AC29	PL99C	6	
AD29	PL99D	6	
AE31	PL103A	6	
AF31	PL103B	6	
AF30	PL103C	6	
AF29	PL103D	6	
AH33	PL104A	6	
AJ33	PL104B	6	
AC28	PL104C	6	
AD28	PL104D	6	
AH32	PL107A	6	
AJ32	PL107B	6	
AD27	PL107C	6	
AE27	PL107D	6	VREF2_6
AG34	PL109A	6	
AH34	PL109B	6	
AC26	PL109C	6	
AB26	PL109D	6	
AK33	PL112A	6	
AL33	PL112B	6	
AG30	PL112C	6	
AH30	PL112D	6	
AL34	PL115A	6	
AM34	PL115B	6	
AJ30	PL115C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL115D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL116A	6	
AH31	PL116B	6	
AD26	PL116C	6	
AD25	PL116D	6	
AL32	PL117A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL117B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL117C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL117D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-	
AF27	TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP20	PB61B	5	
AH21	PB61C	5	
AH20	PB61D	5	
AM20	PB63A	5	
AM19	PB63B	5	
AJ21	PB63C	5	
AJ20	PB63D	5	
AK19	PB66A	5	
AK18	PB66B	5	
AE18	PB66C	5	
AD18	PB66D	5	
AN19	PB69A	5	
AN18	PB69B	5	
AG18	PB69C	5	
AF18	PB69D	5	
AP19	PB71A	5	
AP18	PB71B	5	
AJ18	PB71C	5	
AH18	PB71D	5	
AP17	PB73A	4	
AP16	PB73B	4	
AJ17	PB73C	4	
AH17	PB73D	4	
AN17	PB75A	4	
AN16	PB75B	4	
AE17	PB75C	4	
AD17	PB75D	4	
AK17	PB78A	4	
AK16	PB78B	4	
AG17	PB78C	4	
AF17	PB78D	4	
AM16	PB81A	4	
AM15	PB81B	4	
AJ15	PB81C	4	
AJ14	PB81D	4	
AL16	PB83A	4	
AL15	PB83B	4	
AG16	PB83C	4	
AF16	PB83D	4	
AP15	PB86A	4	
AP14	PB86B	4	
AH15	PB86C	4	
AH14	PB86D	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL5	GND	-	
AM14	GND	-	
AM18	GND	-	
AM24	GND	-	
AM30	GND	-	
AM8	GND	-	
AN1	GND	-	
AN34	GND	-	
AP2	GND	-	
AP33	GND	-	
B1	GND	-	
B34	GND	-	
C11	GND	-	
C12	GND	-	
C13	GND	-	
C14	GND	-	
C17	GND	-	
C21	GND	-	
C22	GND	-	
C23	GND	-	
C24	GND	-	
C26	GND	-	
C27	GND	-	
C30	GND	-	
C31	GND	-	
C4	GND	-	
C5	GND	-	
C8	GND	-	
C9	GND	-	
D18	GND	-	
E32	GND	-	
E4	GND	-	
F19	GND	-	
G16	GND	-	
G29	GND	-	
G7	GND	-	
H3	GND	-	
H31	GND	-	
J10	GND	-	
J15	GND	-	
J26	GND	-	
K20	GND	-	
K23	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP26	PB41C	5		PB43C	5	
AN26	PB41D	5		PB43D	5	
AY30	PB43A	5		PB45A	5	
AY29	PB43B	5		PB45B	5	
AU30	PB43C	5		PB45C	5	
AU31	PB43D	5		PB45D	5	
AV27	PB44A	5		PB46A	5	
AV26	PB44B	5		PB46B	5	
AT28	PB44C	5		PB46C	5	
AT27	PB44D	5		PB46D	5	
BA29	PB45A	5		PB47A	5	
BA28	PB45B	5		PB47B	5	
AL25	PB45C	5		PB47C	5	
AM25	PB45D	5		PB47D	5	
BB29	PB47A	5		PB49A	5	
BB28	PB47B	5		PB49B	5	
AN25	PB47C	5		PB49C	5	
AP25	PB47D	5		PB49D	5	
AY27	PB48A	5	PCLKT5_3	PB50A	5	PCLKT5_3
AY26	PB48B	5	PCLKC5_3	PB50B	5	PCLKC5_3
AT25	PB48C	5	PCLKT5_4	PB50C	5	PCLKT5_4
AT24	PB48D	5	PCLKC5_4	PB50D	5	PCLKC5_4
AW27	PB49A	5	PCLKT5_5	PB51A	5	PCLKT5_5
AW26	PB49B	5	PCLKC5_5	PB51B	5	PCLKC5_5
AU29	PB49C	5		PB51C	5	
AU28	PB49D	5		PB51D	5	
BB27	PB51A	5	PCLKT5_0	PB53A	5	PCLKT5_0
BB26	PB51B	5	PCLKC5_0	PB53B	5	PCLKC5_0
AR25	PB51C	5		PB53C	5	
AR24	PB51D	5	VREF2_5	PB53D	5	VREF2_5
BA27	PB52A	5	PCLKT5_1	PB54A	5	PCLKT5_1
BA26	PB52B	5	PCLKC5_1	PB54B	5	PCLKC5_1
AP24	PB52C	5	PCLKT5_6	PB54C	5	PCLKT5_6
AN24	PB52D	5	PCLKC5_6	PB54D	5	PCLKC5_6
AV25	PB53A	5	PCLKT5_2	PB55A	5	PCLKT5_2
AV24	PB53B	5	PCLKC5_2	PB55B	5	PCLKC5_2
AU27	PB53C	5	PCLKT5_7	PB55C	5	PCLKT5_7
AU26	PB53D	5	PCLKC5_7	PB55D	5	PCLKC5_7
BA25	PB55A	5		PB57A	5	
BA24	PB55B	5		PB57B	5	
AU24	PB55C	5		PB57C	5	
AU25	PB55D	5		PB57D	5	
BB24	PB56A	5		PB58A	5	
BB25	PB56B	5		PB58B	5	
AM23	PB56C	5		PB58C	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL23	PB56D	5		PB58D	5	
AW24	PB57A	5		PB61A	5	
AW23	PB57B	5		PB61B	5	
AN23	PB57C	5		PB61C	5	
AP23	PB57D	5		PB61D	5	
AY23	PB59A	5		PB63A	5	
AY24	PB59B	5		PB63B	5	
AU23	PB59C	5		PB63C	5	
AU22	PB59D	5		PB63D	5	
AV23	PB60A	5		PB66A	5	
AV22	PB60B	5		PB66B	5	
AM22	PB60C	5		PB66C	5	
AL22	PB60D	5		PB66D	5	
BA23	PB61A	5		PB69A	5	
BA22	PB61B	5		PB69B	5	
AN22	PB61C	5		PB69C	5	
AP22	PB61D	5		PB69D	5	
BB23	PB63A	5		PB71A	5	
BB22	PB63B	5		PB71B	5	
AT22	PB63C	5		PB71C	5	
AR22	PB63D	5		PB71D	5	
BB21	PB65A	4		PB73A	4	
BB20	PB65B	4		PB73B	4	
AR21	PB65C	4		PB73C	4	
AT21	PB65D	4		PB73D	4	
BA21	PB66A	4		PB75A	4	
BA20	PB66B	4		PB75B	4	
AP21	PB66C	4		PB75C	4	
AN21	PB66D	4		PB75D	4	
AV21	PB67A	4		PB78A	4	
AV20	PB67B	4		PB78B	4	
AM21	PB67C	4		PB78C	4	
AL21	PB67D	4		PB78D	4	
AY20	PB69A	4		PB81A	4	
AY19	PB69B	4		PB81B	4	
AU21	PB69C	4		PB81C	4	
AU20	PB69D	4		PB81D	4	
AW20	PB70A	4		PB83A	4	
AW19	PB70B	4		PB83B	4	
AP20	PB70C	4		PB83C	4	
AN20	PB70D	4		PB83D	4	
BB19	PB71A	4		PB86A	4	
BB18	PB71B	4		PB86B	4	
AM20	PB71C	4		PB86C	4	
AL20	PB71D	4		PB86D	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BB12	PB88B	4		PB102B	4	
AM17	PB88C	4		PB102C	4	
AL17	PB88D	4		PB102D	4	
AW14	PB89A	4		PB103A	4	
AW13	PB89B	4		PB103B	4	
AP16	PB89C	4		PB103C	4	
AN16	PB89D	4		PB103D	4	
BA13	PB91A	4		PB105A	4	
BA12	PB91B	4		PB105B	4	
AU13	PB91C	4		PB105C	4	
AU12	PB91D	4		PB105D	4	
BB11	PB92A	4		PB106A	4	
BB10	PB92B	4		PB106B	4	
AP15	PB92C	4		PB106C	4	
AN15	PB92D	4		PB106D	4	
AV13	PB93A	4		PB107A	4	
AV12	PB93B	4		PB107B	4	
AT13	PB93C	4		PB107C	4	
AT12	PB93D	4		PB107D	4	
BA11	PB95A	4		PB109A	4	
BA10	PB95B	4		PB109B	4	
AR13	PB95C	4		PB109C	4	
AR12	PB95D	4		PB109D	4	
AY11	PB96A	4		PB110A	4	
AY10	PB96B	4		PB110B	4	
AP14	PB96C	4		PB110C	4	
AN14	PB96D	4		PB110D	4	
BB9	PB97A	4		PB111A	4	
BB8	PB97B	4		PB111B	4	
AU11	PB97C	4		PB111C	4	
AU10	PB97D	4		PB111D	4	
AW11	PB99A	4		PB113A	4	
AW10	PB99B	4		PB113B	4	
AJ16	PB99C	4		PB113C	4	
AJ17	PB99D	4		PB113D	4	
BA9	PB100A	4		PB114A	4	
BA8	PB100B	4		PB114B	4	
AM15	PB100C	4		PB114C	4	
AL15	PB100D	4		PB114D	4	
AV11	PB101A	4		PB115A	4	
AV10	PB101B	4		PB115B	4	
AP13	PB101C	4		PB115C	4	
AP12	PB101D	4		PB115D	4	
BB7	PB103A	4		PB117A	4	
BB6	PB103B	4		PB117B	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCI/O Bank	Dual Function	Ball Function	VCCI/O Bank	Dual Function
AE1	PR74A	3		PR88A	3	
AF12	PR73D	3		PR87D	3	
AE12	PR73C	3		PR87C	3	
AF2	PR73B	3		PR87B	3	
AE2	PR73A	3		PR87A	3	
AF11	PR72D	3		PR86D	3	
AE11	PR72C	3		PR86C	3	
AF5	PR72B	3		PR86B	3	
AE5	PR72A	3		PR86A	3	
AF10	PR69D	3		PR83D	3	
AE10	PR69C	3		PR83C	3	
AD1	PR69B	3		PR83B	3	
AC1	PR69A	3		PR83A	3	
AF9	PR68D	3		PR82D	3	
AE9	PR68C	3		PR82C	3	
AD2	PR68B	3		PR82B	3	
AC2	PR68A	3		PR82A	3	
AF6	PR67D	3		PR81D	3	
AE6	PR67C	3		PR81C	3	
AD3	PR67B	3		PR81B	3	
AC3	PR67A	3		PR81A	3	
AE8	PR65D	3		PR79D	3	
AD8	PR65C	3		PR79C	3	
AD4	PR65B	3		PR79B	3	
AC4	PR65A	3		PR79A	3	
AE7	PR64D	3		PR78D	3	
AD7	PR64C	3		PR78C	3	
AD5	PR64B	3		PR78B	3	
AC5	PR64A	3		PR78A	3	
AD6	PR63D	3		PR77D	3	
AC6	PR63C	3		PR77C	3	
AB1	PR63B	3		PR77B	3	
AA1	PR63A	3		PR77A	3	
AD9	PR61D	3		PR75D	3	
AC9	PR61C	3		PR75C	3	
AB2	PR61B	3		PR75B	3	
AA2	PR61A	3		PR75A	3	
AD14	PR60D	3		PR74D	3	
AC14	PR60C	3		PR74C	3	
AB5	PR60B	3		PR74B	3	
AA5	PR60A	3		PR74A	3	
AD10	PR59D	3		PR73D	3	
AC10	PR59C	3		PR73C	3	
Y1	PR59B	3		PR73B	3	
W1	PR59A	3		PR73A	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H18	PT77C	1	LDCN/SCS	PT93C	1	LDCN/SCS
F18	PT77B	1	D8/MPI_DATA8	PT93B	1	D8/MPI_DATA8
E18	PT77A	1	CS1/MPI_CS1	PT93A	1	CS1/MPI_CS1
H19	PT75D	1	D9/MPI_DATA9	PT90D	1	D9/MPI_DATA9
G19	PT75C	1	D10/MPI_DATA10	PT90C	1	D10/MPI_DATA10
D19	PT75B	1	CS0N/MPI_CS0N	PT90B	1	CS0N/MPI_CS0N
D18	PT75A	1	RDN/MPI_STRB_N	PT90A	1	RDN/MPI_STRB_N
J20	PT74D	1	WRN/MPI_WR_N	PT89D	1	WRN/MPI_WR_N
K20	PT74C	1	D7/MPI_DATA7	PT89C	1	D7/MPI_DATA7
E19	PT74B	1	D6/MPI_DATA6	PT89B	1	D6/MPI_DATA6
F19	PT74A	1	D5/MPI_DATA5	PT89A	1	D5/MPI_DATA5
K18	PT73D	1	D4/MPI_DATA4	PT87D	1	D4/MPI_DATA4
J18	PT73C	1	D3/MPI_DATA3	PT87C	1	D3/MPI_DATA3
A19	PT73B	1	D2/MPI_DATA2	PT87B	1	D2/MPI_DATA2
B19	PT73A	1	D1/MPI_DATA1	PT87A	1	D1/MPI_DATA1
H17	PT71D	1	D16/PCLKC1_3/MPI_DATA16	PT86D	1	D16/PCLKC1_3/MPI_DATA16
J17	PT71C	1	D17/PCLKT1_3/MPI_DATA17	PT86C	1	D17/PCLKT1_3/MPI_DATA17
B20	PT71B	1	D0/MPI_DATA0	PT86B	1	D0/MPI_DATA0
C20	PT71A	1	QOUT/CEON	PT86A	1	QOUT/CEON
M20	PT70D	1	VREF2_1	PT83D	1	VREF2_1
L20	PT70C	1	D18/MPI_DATA18	PT83C	1	D18/MPI_DATA18
F20	PT70B	1	DOUT	PT83B	1	DOUT
G20	PT70A	1	MCA_DONE_IN	PT83A	1	MCA_DONE_IN
K19	PT69D	1	D19/PCLKC1_2/MPI_DATA19	PT81D	1	D19/PCLKC1_2/MPI_DATA19
J19	PT69C	1	D20/PCLKT1_2/MPI_DATA20	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D20	PT69B	1	MCA_CLK_P1_OUT	PT81B	1	MCA_CLK_P1_OUT
E20	PT69A	1	MCA_CLK_P1_IN	PT81A	1	MCA_CLK_P1_IN
H21	PT67D	1	D21/PCLKC1_1/MPI_DATA21	PT78D	1	D21/PCLKC1_1/MPI_DATA21
G21	PT67C	1	D22/PCLKT1_1/MPI_DATA22	PT78C	1	D22/PCLKT1_1/MPI_DATA22
B21	PT67B	1	MCA_CLK_P2_OUT	PT78B	1	MCA_CLK_P2_OUT
C21	PT67A	1	MCA_CLK_P2_IN	PT78A	1	MCA_CLK_P2_IN
M21	PT66D	1	MCA_DONE_OUT	PT75D	1	MCA_DONE_OUT
L21	PT66C	1	BUSYN/RCLK/SCK	PT75C	1	BUSYN/RCLK/SCK
A21	PT66B	1	DP0/MPI_PAR0	PT75B	1	DP0/MPI_PAR0
A20	PT66A	1	MPI_TA	PT75A	1	MPI_TA
J21	PT65D	1	D23/MPI_DATA23	PT73D	1	D23/MPI_DATA23
K21	PT65C	1	DP2/MPI_PAR2	PT73C	1	DP2/MPI_PAR2
E21	PT65B	1	PCLKC1_0	PT73B	1	PCLKC1_0
F21	PT65A	1	PCLKT1_0/MPI_CLK	PT73A	1	PCLKT1_0/MPI_CLK
G22	PT63D	1	DP3/PCLKC1_4/MPI_PAR3	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H22	PT63C	1	D24/PCLKT1_4/MPI_DATA24	PT71C	1	D24/PCLKT1_4/MPI_DATA24
A23	PT63B	1	MPI_RETRY	PT71B	1	MPI_RETRY
A22	PT63A	1	A0/MPI_ADDR14	PT71A	1	A0/MPI_ADDR14
L22	PT61D	1	A1/MPI_ADDR15	PT69D	1	A1/MPI_ADDR15
M22	PT61C	1	A2/MPI_ADDR16	PT69C	1	A2/MPI_ADDR16

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AW25	VCCIO5	-		VCCIO5	-	
AW31	VCCIO5	-		VCCIO5	-	
AW37	VCCIO5	-		VCCIO5	-	
AY22	VCCIO5	-		VCCIO5	-	
AY28	VCCIO5	-		VCCIO5	-	
AY34	VCCIO5	-		VCCIO5	-	
AB39	VCCIO6	-		VCCIO6	-	
AC36	VCCIO6	-		VCCIO6	-	
AD32	VCCIO6	-		VCCIO6	-	
AE40	VCCIO6	-		VCCIO6	-	
AF35	VCCIO6	-		VCCIO6	-	
AG31	VCCIO6	-		VCCIO6	-	
AH39	VCCIO6	-		VCCIO6	-	
AJ36	VCCIO6	-		VCCIO6	-	
AK32	VCCIO6	-		VCCIO6	-	
AL40	VCCIO6	-		VCCIO6	-	
AM35	VCCIO6	-		VCCIO6	-	
AP39	VCCIO6	-		VCCIO6	-	
AR36	VCCIO6	-		VCCIO6	-	
AU40	VCCIO6	-		VCCIO6	-	
AA40	VCCIO7	-		VCCIO7	-	
H36	VCCIO7	-		VCCIO7	-	
J40	VCCIO7	-		VCCIO7	-	
L35	VCCIO7	-		VCCIO7	-	
M39	VCCIO7	-		VCCIO7	-	
P36	VCCIO7	-		VCCIO7	-	
R40	VCCIO7	-		VCCIO7	-	
T31	VCCIO7	-		VCCIO7	-	
U35	VCCIO7	-		VCCIO7	-	
V39	VCCIO7	-		VCCIO7	-	
W32	VCCIO7	-		VCCIO7	-	
Y36	VCCIO7	-		VCCIO7	-	
AA14	VTT_2	2		VTT_2	2	
AA15	VTT_2	2		VTT_2	2	
R12	VTT_2	2		VTT_2	2	
V14	VTT_2	2		VTT_2	2	
AB14	VTT_3	3		VTT_3	3	
AB15	VTT_3	3		VTT_3	3	
AE14	VTT_3	3		VTT_3	3	
AJ13	VTT_3	3		VTT_3	3	
AH21	VTT_4	4		VTT_4	4	
AJ18	VTT_4	4		VTT_4	4	
AJ19	VTT_4	4		VTT_4	4	
AJ20	VTT_4	4		VTT_4	4	
AJ21	VTT_4	4		VTT_4	4	