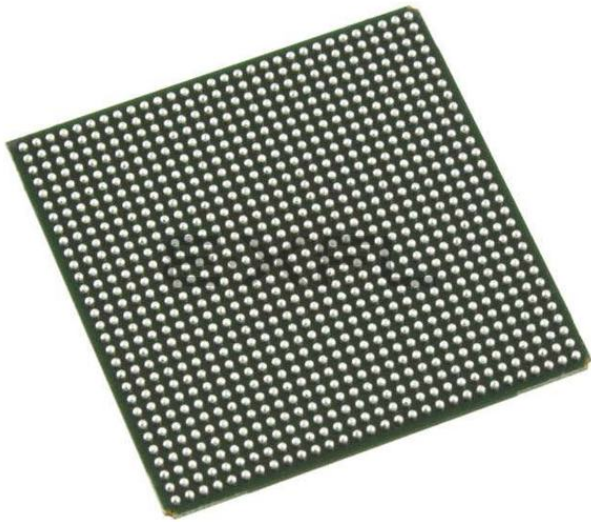




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	378
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga25e-6fn900c

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
FIFO	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output. A clock is required even in asynchronous read mode.

The EBR memory supports two forms of write behavior for dual port operation:

1. **Normal** — data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output.
2. **Write Through** — a copy of the input data appears at the output of the same port.

FIFO Configuration

The FIFO has a write port with Data-in, WCE, WE and WCLK signals. There is a separate read port with Data-out, RCE, RE and RCLK signals. The FIFO internally generates Almost Full, Full, Almost Empty, and Empty Flags. The Full and Almost Full flags are registered with WCLK. The Empty and Almost Empty flags are registered with RCLK.

- 8-bit SERDES Only
- 10-bit SERDES Only
- SONET (STS-12/STS-48)
- Gigabit Ethernet
- Fibre Channel
- XAUI
- Serial RapidIO
- PCI-Express
- Generic 8b10b

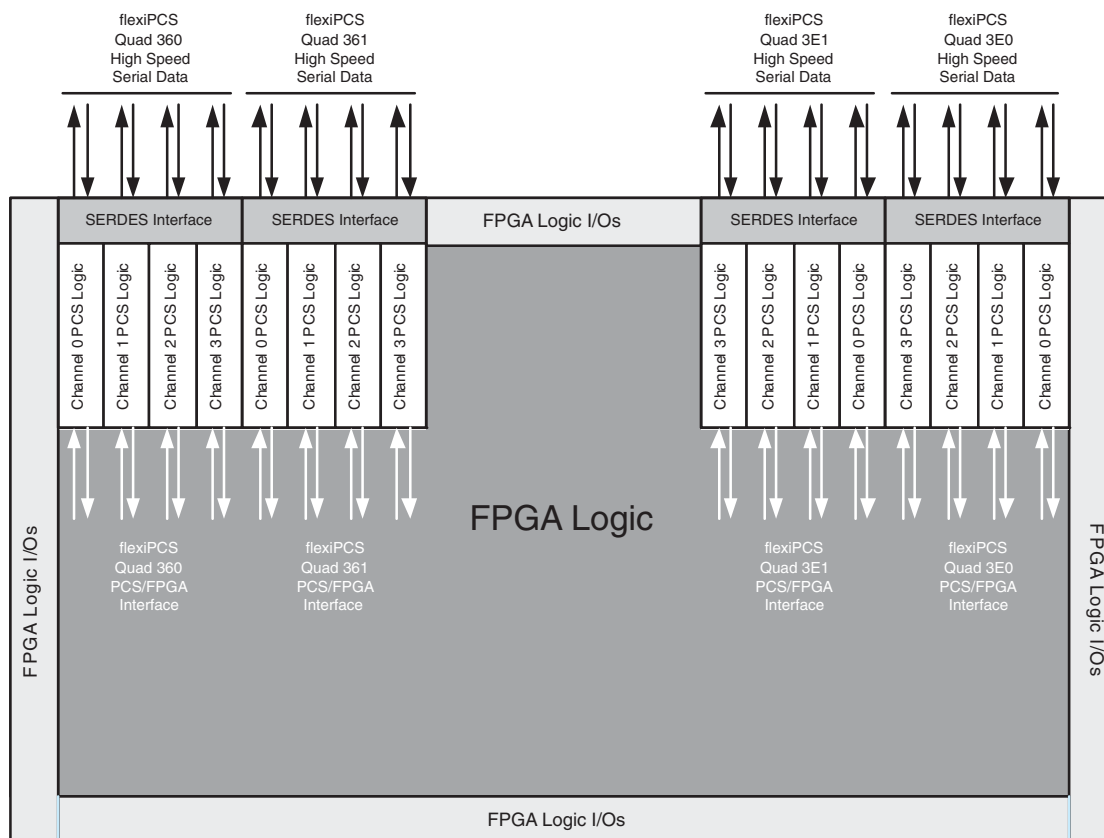
flexiPCS Quad

The flexiPCS logic is arranged in quads containing logic for four independent full-duplex data channels. Each device in the LatticeSC family has up to eight quads of flexiPCS logic. The LatticeSC Family Selection Guide table on the first page of this data sheet contains the number of flexiPCS channels present on the chip. Note that in some packages (particularly lower pin count packages), not all channels from all quads on a given device may be bonded to package pins.

Each quad supports up to four channels of full-duplex data and can be programmed into any one of several protocol based modes. Each quad requires its own reference clock which can be sourced externally or from the FPGA logic. The user can utilize between one and four channels in a quad, depending on the application.

Figure 2-30 shows an example of four flexiPCS quads in a LatticeSC device. Quads are labeled according to the address of their software controlled registers.

Figure 2-30. LatticeSC flexiPCS



Since each quad has its own reference clock, different quads can support different standards on the same chip. This feature makes the LatticeSC family of devices ideal for bridging between different standards.

Initialization and Standby Supply Current

The table below indicates initialization and standby supply current while operating at 85°C junction temperature (T_J), which is the high end of the commercial temperature range, and 105°C, which is the high end of the industrial temperature range. This data assumes all outputs are tri-stated and all inputs are configured as LVCMOS and held at V_{CCIO} or GND. The remaining SERDES supply current for V_{DDIB} and V_{DDOB} is detailed in the SERDES section of this data sheet. For power at your design temperature, it is recommended to use the Power Calculator tool which is accessible in ispLEVER or can be used as a standalone tool. For more information on supply current, see the reference to additional technical documentation available at the end of this data sheet.

Over Recommended Operating Conditions

Symbol	Condition	Parameter	Device	25°C Typ. ¹	85°C Max. ²		105°C Max. ²	Units
				All	-5, -6	-7	-5, -6	
I_{CC}	(VCC = 1.2V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	65	449	678	755	mA
			LFSC/M25	113	798	1255	1343	mA
			LFSC/M40	159	1178	2006	1981	mA
			LFSC/M80	276	2122	3827	3569	mA
			LFSC/M115	454	3376	—	5679	mA
	(VCC = 1.0V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	45	312	471	524	mA
			LFSC/M25	79	554	872	933	mA
			LFSC/M40	110	818	1393	1375	mA
			LFSC/M80	191	1473	2658	2478	mA
			LFSC/M115	315	2344	—	3943	mA
I_{CC12}		1.2V Power Supply Current for Configuration Logic, FPGA PLL, SERDES PLL and SERDES Analog Supplies	LFSC/M15	23	39	59	35	mA
			LFSC/M25	25	50	78	56	mA
			LFSC/M40	31	78	133	89	mA
			LFSC/M80	50	108	195	123	mA
			LFSC/M115	65	131	—	154	mA
I_{CCAUX}		Auxiliary Operating Power Supply Current	LFSC/M15	7	12	19	14	mA
			LFSC/M25	9	16	25	18	mA
			LFSC/M40	12	23	39	25	mA
			LFSC/M80	13	25	45	23	mA
			LFSC/M115	16	27	—	26	mA
I_{CCIO} and I_{CCJ}		Bank Power Supply Current (per bank)	LFSC/M15	0.1	0.2	0.3	0.2	mA
			LFSC/M25	0.3	0.6	1.0	0.7	mA
			LFSC/M40	0.4	0.9	1.5	1.0	mA
			LFSC/M80	0.5	1.1	2.1	1.3	mA
			LFSC/M115	0.7	1.5	—	1.8	mA

1. I_{CC} is specified at $T_J = 25^\circ\text{C}$ and typical V_{CC} .

2. I_{CC} is specified at the respective commercial and industrial maximum T_J and V_{CC} limits.

LatticeSC/M External Switching Characteristics³

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL) ²								
t _{CO}	Global Clock Input to Output - PIO Output Register	2.83	5.74	2.83	6.11	2.83	6.49	ns
t _{SU}	Global Clock Input Setup - PIO Input Register without fixed input delay	-0.66	—	-0.66	—	-0.66	—	ns
t _H	Global Clock Input Hold - PIO Input Register without fixed input delay	1.73	—	1.95	—	2.16	—	ns
t _{SU_IDLY}	Global Clock Input Setup - PIO Input Register with input delay	0.86	—	1.03	—	1.20	—	ns
t _{H_IDLY}	Global Clock Input Hold - PIO Input Register with input delay	-0.17	—	-0.17	—	-0.17	—	ns
f _{MAX_PFU}	Global Clock frequency of PFU register	—	700	—	700	—	700	MHz
f _{MAX_IO}	Global Clock frequency of I/O register	—	1000	—	1000	—	1000	MHz
t _{GC_SKEW}	Global Clock skew	—	89	—	103	—	116	ps
General I/O Pin Parameters (using Primary Clock with PLL) ^{1, 2}								
t _{CO}	Global Clock Input to Output - PIO Output Register	2.25	4.81	2.25	5.08	2.25	5.37	ns
t _{SU}	Global Clock Input Setup - PIO Input Register without fixed input delay	-0.07	—	-0.07	—	-0.07	—	ns
t _H	Global Clock Input Hold - PIO Input Register without fixed input delay	0.80	—	0.93	—	1.04	—	ns
General I/O Pin Parameters (using Edge Clock without PLL) ²								
t _{CO}	Edge Clock Input to Output - PIO Output Register	2.38	4.77	2.38	5.04	2.38	5.33	ns
t _{SU}	Edge Clock Input Setup - PIO Input Register without fixed input delay	-0.08	—	-0.08	—	-0.08	—	ns
t _H	Edge Clock Input Hold - PIO Input Register	0.49	—	0.58	—	0.66	—	ns
t _{SU_IDLY}	Edge Clock Input Setup - PIO Input Register with input delay	0.81	—	0.97	—	1.12	—	ns
t _{H_IDLY}	Edge Clock Input Hold - PIO Input Register with input delay	-0.34	—	-0.34	—	-0.34	—	ns
t _{EC_SKEW}	Edge Clock skew	—	28	—	32	—	36	ps
General I/O Pin Parameters (using Latch FF without PLL) ²								
t _{SU}	Latch FF, Input Setup - PIO Input Register without fixed input delay	-0.14	—	-0.14	—	-0.14	—	ns
t _H	Latch FF, Input Hold - PIO Input Register without fixed input delay	0.58	—	0.68	—	0.77	—	ns
t _{SU_IDLY}	Latch FF, Input Setup - PIO Input Register with input delay	0.70	—	0.68	—	0.77	—	ns
t _{H_IDLY}	Latch FF, Input Hold - PIO Input Register with input delay	-0.30	—	-0.30	—	-0.30	—	ns

1. No PLL delay tuning (clock injection removal mode, system clock feedback).

2. Using LVCMOS25 12mA I/O. Timing adders for other supported I/O technologies are specified in the LatticeSC Family Timing Adders table.

3. Complete Timing Parameters for a user design are incorporated when running ispLEVER. This is a sampling of the key timing parameters.

Timing specs are for non-AIL applications.

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
M4	PL43B	6	
P1	PL45A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
R1	PL45B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
R2	XRES	-	
P3	TEMP	6	
R3	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
N4	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
T3	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
T2	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
N5	PB5D	5	VREF1_5
P5	PB8A	5	
R5	PB8B	5	
T4	PB9A	5	
T5	PB9B	5	
R6	PB12A	5	PCLKT5_3
T6	PB12B	5	PCLKC5_3
L5	PB13C	5	
P6	PB15A	5	PCLKT5_0
T7	PB15B	5	PCLKC5_0
M7	PB15D	5	VREF2_5
R8	PB16A	5	PCLKT5_1
T8	PB16B	5	PCLKC5_1
N7	PB17A	5	PCLKT5_2
N8	PB17B	5	PCLKC5_2
R9	PB20A	5	
T9	PB20B	5	
M8	PB21A	5	
M9	PB21B	5	
P8	PB24A	5	
P9	PB24B	5	
T10	PB28A	4	
R11	PB28B	4	
N9	PB31A	4	
N10	PB31B	4	
T11	PB32A	4	
R12	PB32B	4	
P11	PB35A	4	PCLKT4_2
M10	PB35B	4	PCLKC4_2
T12	PB36A	4	PCLKT4_1
P12	PB36B	4	PCLKC4_1
T13	PB37A	4	PCLKT4_0
T14	PB37B	4	PCLKC4_0
R15	PB37C	4	VREF2_4

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2}

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F7	A_VDDAX25_L	-		A_VDDAX25_L	-	
B1	A_REFCLKP_L	-		A_REFCLKP_L	-	
C1	A_REFCLKN_L	-		A_REFCLKN_L	-	
D5	VCC12	-		VCC12	-	
A2	RESP_ULC	-		RESP_ULC	-	
E5	VCC12	-		VCC12	-	
D4	VCC12	-		VCC12	-	
H5	RESETN	1		RESETN	1	
H6	TSALLN	1		TSALLN	1	
G6	DONE	1		DONE	1	
G5	INITN	1		INITN	1	
F5	M0	1		M0	1	
F6	M1	1		M1	1	
F4	M2	1		M2	1	
E4	M3	1		M3	1	
D3	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
D2	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
J6	PL15C	7		PL16C	7	
J5	PL15D	7		PL16D	7	
E3	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
E2	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
K4	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
J4	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
F3	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
G3	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
K5	PL18C	7		PL18C	7	
K6	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F2	PL19A	7		PL22A	7	
F1	PL19B	7		PL22B	7	
E1	PL19C	7		PL22C	7	
D1	PL19D	7		PL22D	7	
K3	PL22A	7		PL25A	7	
L3	PL22B	7		PL25B	7	
L6	PL22C	7	VREF1_7	PL25C	7	VREF1_7
M6	PL22D	7	DIFFR_7	PL25D	7	DIFFR_7
J1	PL23A	7	PCLKT7_1	PL26A	7	PCLKT7_1
K1	PL23B	7	PCLKC7_1	PL26B	7	PCLKC7_1
L1	PL24A	7	PCLKT7_0	PL27A	7	PCLKT7_0
M1	PL24B	7	PCLKC7_0	PL27B	7	PCLKC7_0
P8	PL24C	7	PCLKT7_2	PL27C	7	PCLKT7_2
R8	PL24D	7	PCLKC7_2	PL27D	7	PCLKC7_2
N2	PL26A	6	PCLKT6_0	PL29A	6	PCLKT6_0
N1	PL26B	6	PCLKC6_0	PL29B	6	PCLKC6_0
R7	PL26C	6	PCLKT6_1	PL29C	6	PCLKT6_1
R6	PL26D	6	PCLKC6_1	PL29D	6	PCLKC6_1

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G1	NC	-		PL20B	7	
M4	NC	-		NC	-	
J3	NC	-		NC	-	
P5	NC	-		NC	-	
W5	NC	-		PL48C	6	
T6	NC	-		PL35C	6	
U3	NC	-		PL36A	6	
V3	NC	-		PL36B	6	
T5	NC	-		PL39A	6	
T4	NC	-		PL39B	6	
V5	NC	-		PL43C	6	
U6	NC	-		PL42C	6	
U4	NC	-		PL40A	6	
U5	NC	-		PL40B	6	
V4	NC	-		PL43D	6	
Y2	NC	-		PL47A	6	
AA2	NC	-		PL47B	6	
W3	NC	-		PL47D	6	
Y3	NC	-		PL47C	6	
AB3	NC	-		NC	-	
AC4	NC	-		PL53A	6	
AD4	NC	-		PL53B	6	
AE3	NC	-		PL56A	6	
AF3	NC	-		PL56B	6	
AF7	NC	-		PB7A	5	
AF6	NC	-		PB7B	5	
AH4	NC	-		PB8A	5	
AG5	NC	-		PB8B	5	
AF8	NC	-		PB9A	5	
AG8	NC	-		PB9B	5	
AG7	NC	-		NC	-	
AG10	NC	-		NC	-	
AF12	NC	-		NC	-	
AH7	NC	-		PB15A	5	
AE13	NC	-		PB15D	5	
AG13	NC	-		PB23C	5	
AH8	NC	-		PB15B	5	
AJ5	NC	-		PB17A	5	
AJ6	NC	-		PB17B	5	
AF15	NC	-		PB21D	5	
AJ7	NC	-		PB19A	5	
AJ8	NC	-		PB19B	5	
AE12	NC	-		PB15C	5	
AF16	NC	-		PB38D	4	
AF19	NC	-		PB49D	4	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG11	VCCIO5	-		VCCIO5	-	
AJ9	VCCIO5	-		VCCIO5	-	
AJ23	VCCIO4	-		VCCIO4	-	
AG20	VCCIO4	-		VCCIO4	-	
AJ26	VCCIO4	-		VCCIO4	-	
AG23	VCCIO4	-		VCCIO4	-	
AC29	VCCIO3	-		VCCIO3	-	
AA26	VCCIO3	-		VCCIO3	-	
Y28	VCCIO3	-		VCCIO3	-	
AA29	VCCIO3	-		VCCIO3	-	
G30	VCCIO2	-		VCCIO2	-	
J29	VCCIO2	-		VCCIO2	-	
K27	VCCIO2	-		VCCIO2	-	
N25	VCCIO2	-		VCCIO2	-	
F20	VCCIO1	-		VCCIO1	-	
C19	VCCIO1	-		VCCIO1	-	
C12	VCCIO1	-		VCCIO1	-	
F11	VCCIO1	-		VCCIO1	-	
H1	GND	-		GND	-	
L4	GND	-		GND	-	
M3	GND	-		GND	-	
N5	GND	-		GND	-	
K2	GND	-		GND	-	
M2	GND	-		GND	-	
P6	GND	-		GND	-	
G4	GND	-		GND	-	
H3	GND	-		GND	-	
AC2	GND	-		GND	-	
AA3	GND	-		GND	-	
AE1	GND	-		GND	-	
Y4	GND	-		GND	-	
AB4	GND	-		GND	-	
AA5	GND	-		GND	-	
AE6	GND	-		GND	-	
AE8	GND	-		GND	-	
AH5	GND	-		GND	-	
AG9	GND	-		GND	-	
AG6	GND	-		GND	-	
AF11	GND	-		GND	-	
AG12	GND	-		GND	-	
AJ10	GND	-		GND	-	
AK26	GND	-		GND	-	
AJ22	GND	-		GND	-	
AF20	GND	-		GND	-	
AJ25	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2}

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C28	A_REFCLKP_L	-		A_REFCLKP_L	-	
D28	A_REFCLKN_L	-		A_REFCLKN_L	-	
B28	VCC12	-		VCC12	-	
F28	RESP_ULC	-		RESP_ULC	-	
J21	RESETN	1		RESETN	1	
J20	TSALLN	1		TSALLN	1	
K20	DONE	1		DONE	1	
K21	INITN	1		INITN	1	
K23	M0	1		M0	1	
J23	M1	1		M1	1	
J24	M2	1		M2	1	
K24	M3	1		M3	1	
K25	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J25	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
K26	PL16C	7		PL16C	7	
K27	PL16D	7		PL16D	7	
D32	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
D31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
M23	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
N23	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
E32	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E31	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
J28	PL18C	7		PL18C	7	
K28	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F32	PL20A	7		PL21A	7	
F31	PL20B	7		PL21B	7	
L25	PL20C	7		PL21C	7	
L26	PL20D	7		PL21D	7	
G31	PL21A	7		PL22A	7	
G32	PL21B	7		PL22B	7	
J29	PL22A	7		PL25A	7	
H29	PL22B	7		PL25B	7	
M25	PL22C	7		PL25C	7	
N25	PL22D	7		PL25D	7	
H31	PL25A	7		PL23A	7	
H32	PL25B	7		PL23B	7	
M24	PL25C	7	VREF1_7	PL23C	7	VREF1_7
N24	PL25D	7	DIFFR_7	PL23D	7	DIFFR_7
L32	PL26A	7	PCLKT7_1	PL35A	7	PCLKT7_1
M32	PL26B	7	PCLKC7_1	PL35B	7	PCLKC7_1
R25	PL26C	7	PCLKT7_3	PL35C	7	PCLKT7_3
R24	PL26D	7	PCLKC7_3	PL35D	7	PCLKC7_3
N31	PL27A	7	PCLKT7_0	PL36A	7	PCLKT7_0
N32	PL27B	7	PCLKC7_0	PL36B	7	PCLKC7_0
P27	PL27C	7	PCLKT7_2	PL36C	7	PCLKT7_2
P28	PL27D	7	PCLKC7_2	PL36D	7	PCLKC7_2
P30	PL29A	6	PCLKT6_0	PL38A	6	PCLKT6_0
P29	PL29B	6	PCLKC6_0	PL38B	6	PCLKC6_0
T23	PL29C	6	PCLKT6_1	PL38C	6	PCLKT6_1
T24	PL29D	6	PCLKC6_1	PL38D	6	PCLKC6_1

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E16	PT45C	1	D3/MPI_DATA3	PT54C	1	D3/MPI_DATA3
C13	PT45B	1	D2/MPI_DATA2	PT53B	1	D2/MPI_DATA2
C14	PT45A	1	D1/MPI_DATA1	PT53A	1	D1/MPI_DATA1
B14	PT43B	1	D0/MPI_DATA0	PT51B	1	D0/MPI_DATA0
B13	PT43A	1	QOUT/CEON	PT51A	1	QOUT/CEON
L13	PT42D	1	VREF2_1	PT50D	1	VREF2_1
C15	PT42B	1	DOUT	PT50B	1	DOUT
D15	PT42A	1	MCA_DONE_IN	PT50A	1	MCA_DONE_IN
J16	PT41B	1	MCA_CLK_P1_OUT	PT49B	1	MCA_CLK_P1_OUT
K16	PT41A	1	MCA_CLK_P1_IN	PT49A	1	MCA_CLK_P1_IN
H15	PT39D	1	D21/PCLKC1_1/MPI_DATA21	PT47D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT39C	1	D22/PCLKT1_1/MPI_DATA22	PT47C	1	D22/PCLKT1_1/MPI_DATA22
A14	PT39B	1	MCA_CLK_P2_OUT	PT47B	1	MCA_CLK_P2_OUT
A13	PT39A	1	MCA_CLK_P2_IN	PT47A	1	MCA_CLK_P2_IN
G16	PT38D	1	MCA_DONE_OUT	PT46D	1	MCA_DONE_OUT
F16	PT38C	1	BUSYN/RCLK/SCK	PT46C	1	BUSYN/RCLK/SCK
B16	PT38B	1	DP0/MPI_PAR0	PT46B	1	DP0/MPI_PAR0
B15	PT38A	1	MPI_TA	PT46A	1	MPI_TA
L16	PT37C	1	DP2/MPI_PAR2	PT45C	1	DP2/MPI_PAR2
A16	PT37B	1	PCLKC1_0	PT45B	1	PCLKC1_0
A15	PT37A	1	PCLKT1_0/MPI_CLK	PT45A	1	PCLKT1_0/MPI_CLK
L17	PT35C	1	D24/PCLKT1_4/MPI_DATA24	PT43C	1	D24/PCLKT1_4/MPI_DATA24
A17	PT35B	1	MPI_RETRY	PT43B	1	MPI_RETRY
A18	PT35A	1	A0/MPI_ADDR14	PT43A	1	A0/MPI_ADDR14
F17	PT33D	1	A1/MPI_ADDR15	PT42D	1	A1/MPI_ADDR15
G17	PT33C	1	A2/MPI_ADDR16	PT42C	1	A2/MPI_ADDR16
B17	PT33B	1	A3/MPI_ADDR17	PT42B	1	A3/MPI_ADDR17
B18	PT33A	1	A4/MPI_ADDR18	PT42A	1	A4/MPI_ADDR18
H17	PT32D	1	D25/PCLKC1_5/MPI_DATA25	PT41D	1	D25/PCLKC1_5/MPI_DATA25
H18	PT32C	1	D26/PCLKT1_5/MPI_DATA26	PT41C	1	D26/PCLKT1_5/MPI_DATA26
A19	PT32B	1	A5/MPI_ADDR19	PT41B	1	A5/MPI_ADDR19
A20	PT32A	1	A6/MPI_ADDR20	PT41A	1	A6/MPI_ADDR20
L20	PT31C	1	VREF1_1	PT39C	1	VREF1_1
J17	PT31B	1	A7/MPI_ADDR21	PT39B	1	A7/MPI_ADDR21
K17	PT31A	1	A8/MPI_ADDR22	PT39A	1	A8/MPI_ADDR22
C18	PT29B	1	A9/MPI_ADDR23	PT38B	1	A9/MPI_ADDR23
D18	PT29A	1	A10/MPI_ADDR24	PT38A	1	A10/MPI_ADDR24
B19	PT28B	1	A11/MPI_ADDR25	PT37B	1	A11/MPI_ADDR25
B20	PT28A	1	A12/MPI_ADDR26	PT37A	1	A12/MPI_ADDR26
E17	PT27D	1	D11/MPI_DATA11	PT35D	1	D11/MPI_DATA11
E18	PT27C	1	D12/MPI_DATA12	PT35C	1	D12/MPI_DATA12
C20	PT27B	1	A13/MPI_ADDR27	PT35B	1	A13/MPI_ADDR27
C19	PT27A	1	A14/MPI_ADDR28	PT35A	1	A14/MPI_ADDR28
H19	PT25D	1	A16/MPI_ADDR30	PT33D	1	A16/MPI_ADDR30
G19	PT25C	1	D13/MPI_DATA13	PT33C	1	D13/MPI_DATA13
D20	PT25B	1	A15/MPI_ADDR29	PT33B	1	A15/MPI_ADDR29
D19	PT25A	1	A17/MPI_ADDR31	PT33A	1	A17/MPI_ADDR31
H20	PT24D	1	A19/MPI_TSI21	PT30D	1	A19/MPI_TSI21
G20	PT24C	1	A20/MPI_BDIP	PT30C	1	A20/MPI_BDIP
E19	PT24B	1	A18/MPI_TSI20	PT30B	1	A18/MPI_TSI20

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD8	PR65C	3		PR89C	3	
AJ3	PR65B	3		PR89B	3	
AH3	PR65A	3		PR89A	3	
AD7	PR62D	3		PR86D	3	
AC7	PR62C	3		PR86C	3	
AJ2	PR62B	3		PR86B	3	
AH2	PR62A	3		PR86A	3	
AF6	PR61D	3		PR85D	3	
AF5	PR61C	3		PR85C	3	
AF4	PR61B	3		PR85B	3	
AE4	PR61A	3		PR85A	3	
AD6	PR60D	3		PR84D	3	
AC6	PR60C	3		PR84C	3	
AG2	PR60B	3		PR84B	3	
AF2	PR60A	3		PR84A	3	
AC8	PR58D	3		PR82D	3	
AB8	PR58C	3		PR82C	3	
AK1	PR58B	3		PR82B	3	
AJ1	PR58A	3		PR82A	3	
AB10	PR57D	3		PR81D	3	
AA10	PR57C	3		PR81C	3	
AF3	PR57B	3		PR81B	3	
AE3	PR57A	3		PR81A	3	
AE5	PR56D	3		PR80D	3	
AD5	PR56C	3		PR80C	3	
AE2	PR56B	3		PR80B	3	
AD2	PR56A	3		PR80A	3	
AC5	PR53D	3		PR78D	3	
AB5	PR53C	3		PR78C	3	
AF1	PR53B	3		PR78B	3	
AE1	PR53A	3		PR78A	3	
AA11	PR52D	3		PR77D	3	
Y11	PR52C	3		PR77C	3	
AC4	PR52B	3		PR77B	3	
AB4	PR52A	3		PR77A	3	
AA8	PR51D	3	DIFFR_3	PR76D	3	DIFFR_3
AA9	PR51C	3		PR76C	3	
AC3	PR51B	3		PR76B	3	
AB3	PR51A	3		PR76A	3	
AA7	PR49D	3		PR65D	3	
Y7	PR49C	3		PR65C	3	
AA2	PR49B	3		PR65B	3	
Y2	PR49A	3		PR65A	3	
AA6	PR48D	3		PR63D	3	
Y6	PR48C	3		PR63C	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AD5	PR94C	3	
AE2	PR94B	3	
AD2	PR94A	3	
AC5	PR92D	3	
AB5	PR92C	3	
AF1	PR92B	3	
AE1	PR92A	3	
AA11	PR91D	3	
Y11	PR91C	3	
AC4	PR91B	3	
AB4	PR91A	3	
AA8	PR90D	3	DIFFR_3
AA9	PR90C	3	
AC3	PR90B	3	
AB3	PR90A	3	
AA7	PR79D	3	
Y7	PR79C	3	
AA2	PR79B	3	
Y2	PR79A	3	
AA6	PR77D	3	
Y6	PR77C	3	
Y4	PR77B	3	
W4	PR77A	3	
W11	PR74D	3	
V11	PR74C	3	
W2	PR74B	3	
V2	PR74A	3	
W9	PR71D	3	
V9	PR71C	3	
V1	PR71B	3	
U1	PR71A	3	
W10	PR70D	3	
V10	PR70C	3	
U2	PR70B	3	
T2	PR70A	3	
Y8	PR69D	3	
W8	PR69C	3	VREF1_3
W5	PR69B	3	
V5	PR69A	3	
V7	PR66D	3	PCLKC3_2
U7	PR66C	3	PCLKT3_2
T1	PR66B	3	
R1	PR66A	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
V8	PR65D	3	PCLKC3_3
U8	PR65C	3	PCLKT3_3
U5	PR65B	3	
T5	PR65A	3	
V6	PR64D	3	PCLKC3_1
U6	PR64C	3	PCLKT3_1
T4	PR64B	3	PCLKC3_0
T3	PR64A	3	PCLKT3_0
U9	PR62D	2	PCLKC2_2
T9	PR62C	2	PCLKT2_2
R2	PR62B	2	PCLKC2_0
P2	PR62A	2	PCLKT2_0
T11	PR61D	2	PCLKC2_3
U11	PR61C	2	PCLKT2_3
R4	PR61B	2	PCLKC2_1
R3	PR61A	2	PCLKT2_1
T8	PR60D	2	
R8	PR60C	2	
P1	PR60B	2	
N1	PR60A	2	
R6	PR57D	2	
P6	PR57C	2	
M1	PR57B	2	
L1	PR57A	2	
T10	PR56D	2	
U10	PR56C	2	
N2	PR56B	2	
M2	PR56A	2	
R11	PR51D	2	
P11	PR51C	2	
N4	PR51B	2	
M4	PR51A	2	
N5	PR49D	2	
M5	PR49C	2	
L2	PR49B	2	
K2	PR49A	2	
P8	PR47D	2	
N8	PR47C	2	
J2	PR47B	2	
H2	PR47A	2	
M6	PR45D	2	
L6	PR45C	2	
K3	PR45B	2	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
D9	B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-	
E9	B_VDDIB3_R	-	
L13	VCC12	-	
J11	B_REFCLKN_R	-	
H11	B_REFCLKP_R	-	
M15	PT93D	1	HDC/SI
M16	PT93C	1	LDCN/SCS
F14	PT93B	1	D8/MPI_DATA8
G14	PT93A	1	CS1/MPI_CS1
L15	PT90D	1	D9/MPI_DATA9
L14	PT90C	1	D10/MPI_DATA10
D14	PT90B	1	CS0N/MPI_CS0N
E14	PT90A	1	RDN/MPI_STRB_N
L16	PT89D	1	WRN/MPI_WR_N
K16	PT89C	1	D7/MPI_DATA7
G15	PT89B	1	D6/MPI_DATA6
F15	PT89A	1	D5/MPI_DATA5
K14	PT87D	1	D4/MPI_DATA4
K13	PT87C	1	D3/MPI_DATA3
B15	PT87B	1	D2/MPI_DATA2
A15	PT87A	1	D1/MPI_DATA1
J14	PT86D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT86C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT86B	1	D0/MPI_DATA0
B16	PT86A	1	QOUT/CEON
J13	PT83D	1	VREF2_1
H13	PT83C	1	D18/MPI_DATA18
D15	PT83B	1	DOUT
E15	PT83A	1	MCA_DONE_IN
J16	PT81D	1	D19/PCLKC1_2/MPI_DATA19

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2}

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G34	A_REFCLKP_L	-		A_REFCLKP_L	-	
H34	A_REFCLKN_L	-		A_REFCLKN_L	-	
N30	VCC12	-		VCC12	-	
H33	RESP_ULC	-		RESP_ULC	-	
P25	RESETN	1		RESETN	1	
P26	TSALLN	1		TSALLN	1	
P31	DONE	1		DONE	1	
P23	INITN	1		INITN	1	
P30	M0	1		M0	1	
P22	M1	1		M1	1	
P24	M2	1		M2	1	
R22	M3	1		M3	1	
J37	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J38	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
P32	PL16C	7		PL15C	7	
R32	PL16D	7		PL15D	7	
G40	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
H40	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N33	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P33	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
G41	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
H41	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
T29	PL18C	7		PL18C	7	
U29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
G42	PL20A	7		PL19A	7	
H42	PL20B	7		PL19B	7	
M34	PL20C	7		PL19C	7	
M35	PL20D	7		PL19D	7	
K37	PL21A	7		PL26A	7	
L37	PL21B	7		PL26B	7	
N34	PL21C	7		PL26C	7	
P34	PL21D	7		PL26D	7	
K38	PL22A	7		PL30A	7	
L38	PL22B	7		PL30B	7	
T33	PL22C	7		PL30C	7	
R33	PL22D	7		PL30D	7	
J41	PL24A	7		PL34A	7	
K41	PL24B	7		PL34B	7	
U31	PL24C	7		PL34C	7	
V31	PL24D	7		PL34D	7	
K42	PL25A	7		PL38A	7	
J42	PL25B	7		PL38B	7	
J36	PL25C	7		PL38C	7	
K36	PL25D	7		PL38D	7	
N38	PL26A	7		PL40A	7	

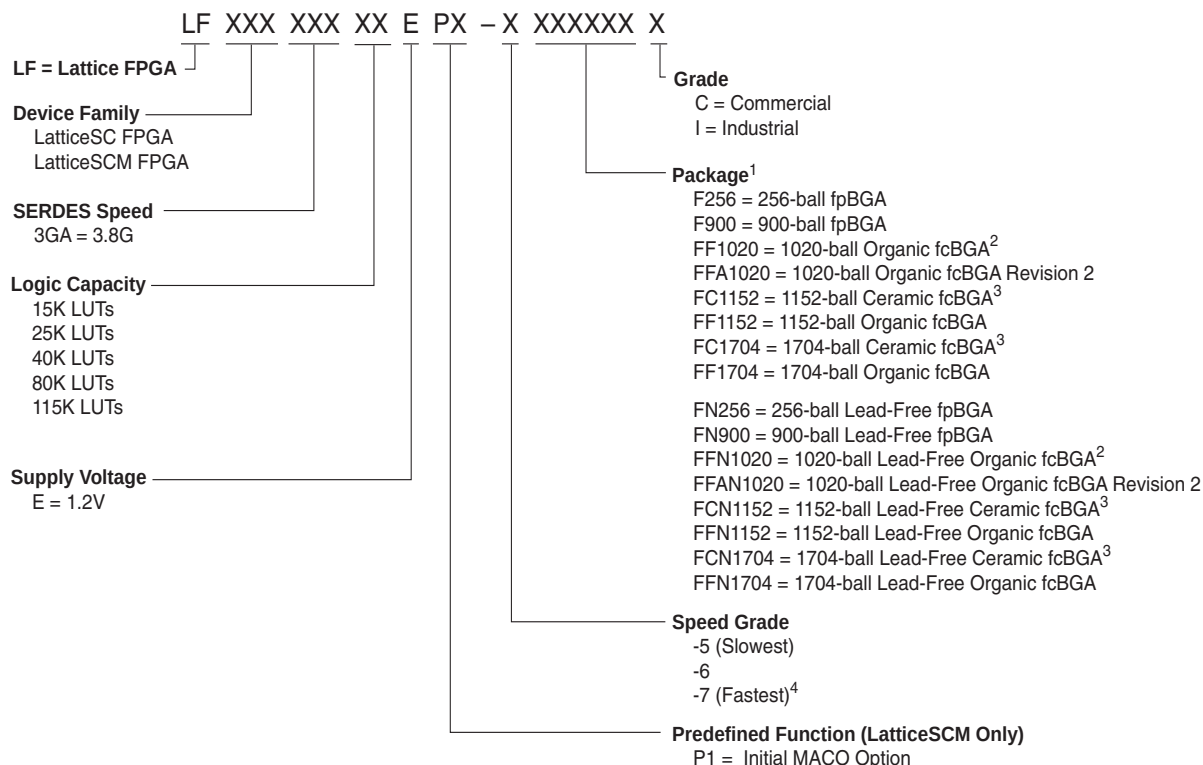
LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB6	PR57D	3		PR71D	3	
AA6	PR57C	3		PR71C	3	
Y2	PR57B	3		PR71B	3	
W2	PR57A	3		PR71A	3	
AB7	PR56D	3		PR70D	3	
AA7	PR56C	3		PR70C	3	
Y3	PR56B	3		PR70B	3	
W3	PR56A	3		PR70A	3	
AC11	PR55D	3		PR69D	3	
AB11	PR55C	3	VREF1_3	PR69C	3	VREF1_3
Y4	PR55B	3		PR69B	3	
W4	PR55A	3		PR69A	3	
AB8	PR52D	3	PCLKC3_2	PR66D	3	PCLKC3_2
AA8	PR52C	3	PCLKT3_2	PR66C	3	PCLKT3_2
Y5	PR52B	3		PR66B	3	
W5	PR52A	3		PR66A	3	
AC12	PR51D	3	PCLKC3_3	PR65D	3	PCLKC3_3
AB12	PR51C	3	PCLKT3_3	PR65C	3	PCLKT3_3
V1	PR51B	3		PR65B	3	
U1	PR51A	3		PR65A	3	
W7	PR50D	3	PCLKC3_1	PR64D	3	PCLKC3_1
V7	PR50C	3	PCLKT3_1	PR64C	3	PCLKT3_1
V2	PR50B	3	PCLKC3_0	PR64B	3	PCLKC3_0
U2	PR50A	3	PCLKT3_0	PR64A	3	PCLKT3_0
AB9	PR48D	2	PCLKC2_2	PR62D	2	PCLKC2_2
AA9	PR48C	2	PCLKT2_2	PR62C	2	PCLKT2_2
T1	PR48B	2	PCLKC2_0	PR62B	2	PCLKC2_0
R1	PR48A	2	PCLKT2_0	PR62A	2	PCLKT2_0
AB10	PR47D	2	PCLKC2_3	PR61D	2	PCLKC2_3
AA10	PR47C	2	PCLKT2_3	PR61C	2	PCLKT2_3
U3	PR47B	2	PCLKC2_1	PR61B	2	PCLKC2_1
T3	PR47A	2	PCLKT2_1	PR61A	2	PCLKT2_1
Y9	PR46D	2		PR60D	2	
W9	PR46C	2		PR60C	2	
V5	PR46B	2		PR60B	2	
U5	PR46A	2		PR60A	2	
AA11	PR43D	2		PR57D	2	
Y11	PR43C	2		PR57C	2	
Y6	PR43B	2		PR57B	2	
W6	PR43A	2		PR57A	2	
Y10	PR42D	2		PR56D	2	
W10	PR42C	2		PR56C	2	
T2	PR42B	2		PR56B	2	
R2	PR42A	2		PR56A	2	
W8	PR41D	2		PR55D	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
V21	VCC	-		VCC	-	
V22	VCC	-		VCC	-	
V23	VCC	-		VCC	-	
V25	VCC	-		VCC	-	
V27	VCC	-		VCC	-	
W17	VCC	-		VCC	-	
W19	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
W22	VCC	-		VCC	-	
W24	VCC	-		VCC	-	
W26	VCC	-		VCC	-	
Y16	VCC	-		VCC	-	
Y18	VCC	-		VCC	-	
Y20	VCC	-		VCC	-	
Y23	VCC	-		VCC	-	
Y25	VCC	-		VCC	-	
Y27	VCC	-		VCC	-	
AG22	VCC12	-		VCC12	-	
AG26	VCC12	-		VCC12	-	
T17	VCC12	-		VCC12	-	
T21	VCC12	-		VCC12	-	
T22	VCC12	-		VCC12	-	
T26	VCC12	-		VCC12	-	
U16	VCC12	-		VCC12	-	
U27	VCC12	-		VCC12	-	
AC15	VCCAUX	-		VCCAUX	-	
AC28	VCCAUX	-		VCCAUX	-	
AD15	VCCAUX	-		VCCAUX	-	
AD28	VCCAUX	-		VCCAUX	-	
AE15	VCCAUX	-		VCCAUX	-	
AE28	VCCAUX	-		VCCAUX	-	
AF15	VCCAUX	-		VCCAUX	-	
AF28	VCCAUX	-		VCCAUX	-	
AG15	VCCAUX	-		VCCAUX	-	
AG28	VCCAUX	-		VCCAUX	-	
AH14	VCCAUX	-		VCCAUX	-	
AH16	VCCAUX	-		VCCAUX	-	
AH17	VCCAUX	-		VCCAUX	-	
AH18	VCCAUX	-		VCCAUX	-	
AH19	VCCAUX	-		VCCAUX	-	
AH20	VCCAUX	-		VCCAUX	-	
AH23	VCCAUX	-		VCCAUX	-	
AH24	VCCAUX	-		VCCAUX	-	
AH25	VCCAUX	-		VCCAUX	-	
AH26	VCCAUX	-		VCCAUX	-	

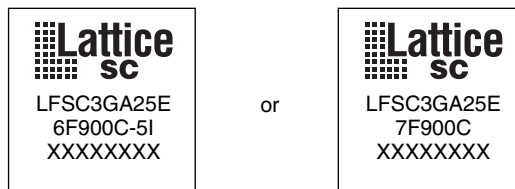
Part Number Description



1. fpBGA = 1.0 mm pitch BGA, fcBGA = 1.0 mm flip-chip BGA (organic and ceramic).
2. Converted to organic fcBGA per PCN #02A-10.
3. Converted to organic fcBGA per PCN #01A-10.
4. Not available in the LatticeSC115 and LatticeSCM115 devices.

Ordering Information

Depending on the speed and temperature grade, the device can either be dual marked or single marked. The commercial grade is one speed grade faster than the associated dual marked industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:



Temperature Grade	Speed Grade	Single or Dual Mark?
Commercial	-7	Either OK
	-6	Dual Only
	-5	Single Only
Industrial	-6	Either OK
	-5	Dual Only

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-6FFN1020I ¹	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-5FFN1020I ¹	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-6FCN1152I ²	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FCN1152I ²	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSC3GA80E-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).