Lattice Semiconductor Corporation - LFSC3GA25E-7FFA1020C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

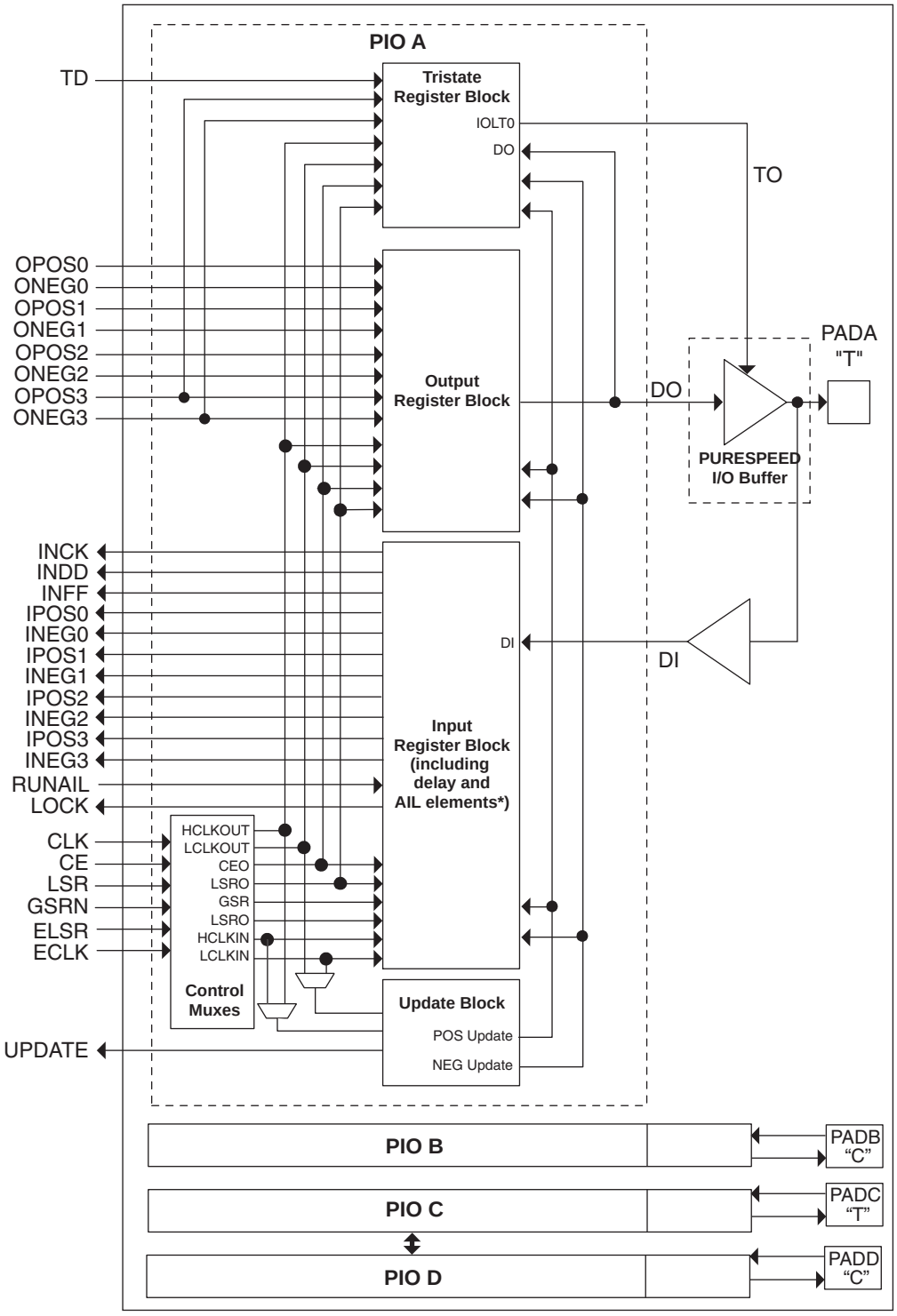
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	476
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFcBGA Rev 2 (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga25e-7ffa1020c

Figure 2-17. PIC Diagram



*AIL only on A or C pads located on the left, right and bottom of the device.

The A/B PIOs on the left and the right of the device can be paired to form a differentiated driver. The A/B and C/D PIOs on all sides of the device can be paired to form differential receivers. Either A or C PIOs on all sides except the one on top also provide a connection to an adaptive input logic capability that facilitates the implementation of

Table 2-6. Input/Output/Tristate Gearing Resource Rules

PIO	Input/Output Logic			Tri-State/Bidi	
	x1	x2	x4	x1	x2/x4
A	?	?	?	?	N/A
B	?	No I/O Logic	No I/O Logic	?	N/A
C	?	?	No I/O Logic	?	N/A
D	?	No I/O Logic	No I/O Logic	?	N/A

Note: Pin can still be used without I/O logic.

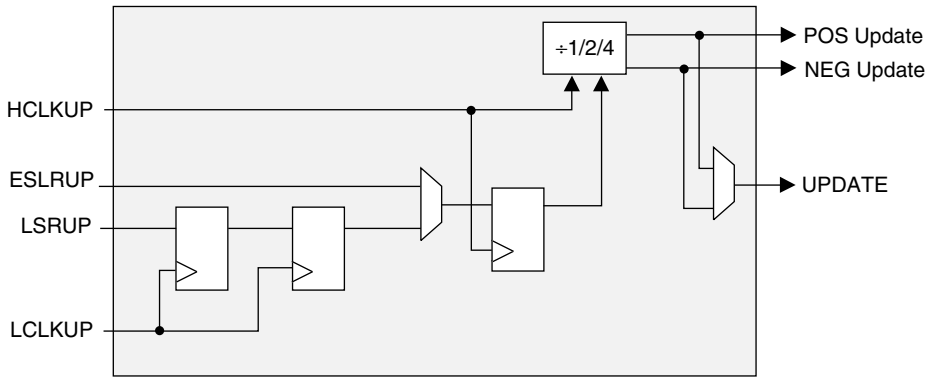
Control Logic Block

The control logic block allows the modification of control signals selected by the routing before they are used in the PIO. It can optionally invert all signals passing through it except the Global Set/Reset. Global Set/Reset can be enabled or disabled. It can route either the edge clock or the clock to the high-speed clock nets. The clock provided to the PIO by routing is used as the slow-speed clocks. In addition this block contains delays that can be inserted in the clock nets to enable Lattice's unique cycle boosting capability.

Update Block

The update block is used to generate the POS update and NEG update signals used by the DDR/Shift register blocks within the PIO. Note the update block is only required in shift modes. This is required in order to do the high speed to low speed handoff. One of these update signals is also selected and output from the PIC as the signal UPDATE. It consists of a shift chain that operates off either the high-speed input or output clock. The values of each register in the chain are set or reset depending on the desired mode of operation. The set/reset signal is generated from either the edge reset ELSR or the local reset LSR. These signals are optionally inverted by the Control Logic Block and provided to the update block as ELSRUP and LSRUP. The Lattice design tools automatically configure and connect the update block when one of the DDR or shift register primitives is used.

Figure 2-25. Update Block



PURESPEED I/O Buffer

Each I/O is associated with a flexible buffer referred to as PURESPEED I/O buffer. These buffers are arranged around the periphery of the device in seven groups referred to as Banks. The PURESPEED I/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL. The availability of programmable on-chip termination for both input and output use, further enhances the utility of these buffers.

Density Shifting

The LatticeSC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

LatticeSC/M Family Data Sheet DC and Switching Characteristics

December 2011 **Data Sheet DS1004**

Absolute Maximum Ratings

Supply Voltage V_{CC}, V_{CC12}, V_{DDIB}, V_{DDOB} . . . . . -0.5 to 1.6V

Supply Voltage V_{CCAUX}, V_{DDAX25}, V_{TT} . . . . . -0.5 to 2.75V

Supply Voltage V_{CCJ} . . . . . -0.5 to 3.6V

Supply Voltage V_{CCIO} (Banks 1, 4, 5) . . . . . -0.5 to 3.6V

Supply Voltage V_{CCIO} (Banks 2, 3, 6, 7) . . . . . -0.5 to 2.75V

Input or I/O Tristate Voltage Applied (Banks 1, 4, 5) . . . . . -0.5 to 3.6V

Input or I/O Tristate Voltage Applied (Banks 2, 3, 6, 7) . . . . . -0.5 to 2.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temperature Under Bias (Tj) . . . . . +125°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot and overshoot of -2V to (VIHMAX +2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}[5]	Core Supply Voltage (Nominal 1.2V Operation)	0.95	1.26	V
V_{CCAUX}[6]	Programmable I/O Auxiliary Supply Voltage	2.375	2.625	V
V_{CCIO}[1, 2, 5, 6]	Programmable I/O Driver Supply Voltage (Banks 1, 4, 5)	1.14	3.45	V
V_{CCIO}[1, 2, 5, 6]	Programmable I/O Driver Supply Voltage (Banks 2, 3, 6, 7)	1.14	2.625	V
V_{CC12}[4, 5]	Internal 1.2V Power Supply Voltage for Configuration Logic and FPGA PLL, SERDES PLL Power Supply Voltage and SERDES Analog Supply Voltage	1.14	1.26	V
V_{DDIB}	SERDES Input Buffer Supply Voltage	1.14	1.575	V
V_{DDOB}	SERDES Output Buffer Supply Voltage	1.14	1.575	V
V_{DDAX25}	SERDES Termination Auxiliary Supply Voltage	2.375	2.625	V
V_{CCJ}[1, 5]	Supply Voltage for IEEE 1149.1 Test Access Port	1.71	3.45	V
V_{TT}[2, 3]	Programmable I/O Termination Power Supply	0.5	V_{CCAUX} - 0.5	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	+85	C
t_{JIND}	Junction Temperature, Industrial Operation	-40	105	C

1. If V_{CCIO} or V_{CCJ} is set to 2.5V, they must be connected to the same power supply as V_{CCAUX}.
2. See recommended voltages by I/O standard in subsequent table.
3. When V_{TT} termination is not required, or used to provide the common mode termination voltage (V_{CMT}), these pins can be left unconnected on the device.
4. V_{CC12} cannot be lower than V_{CC} at any time. For 1.2V operation, it is recommended that the V_{CC} and V_{CC12} supplies be tied together with proper noise decoupling between the digital VCC and analog VCC12 supplies.
5. V_{CC}, V_{CCIO} (all banks), V_{CC12} and V_{CCJ} must reach their minimum values before configuration will proceed.
6. If V_{CCIO} for a bank is nominally 1.2V/1.5V/1.8V, then V_{CCAUX} must always be higher than V_{CCIO} during power up.

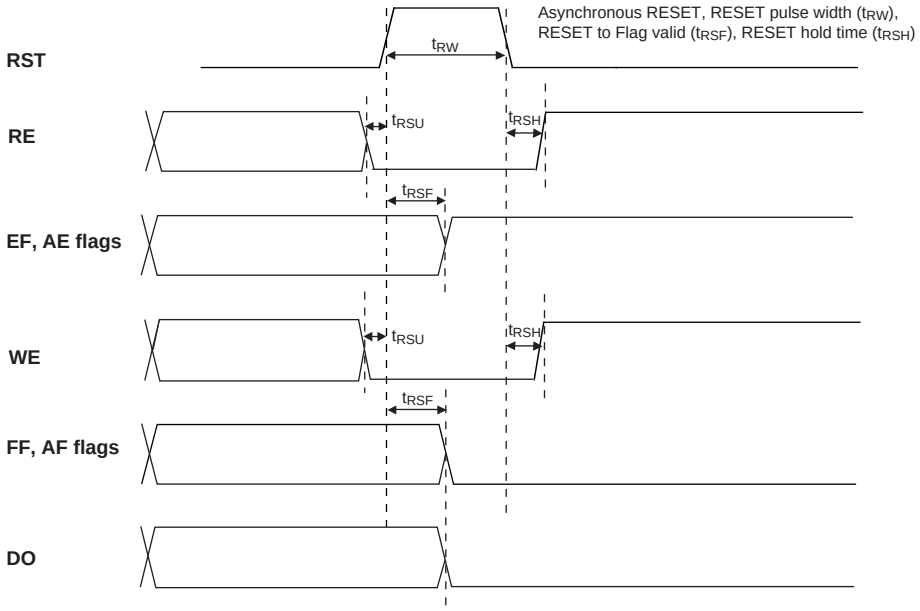
RSDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
V_{OD}	Output voltage, differential, R_T = 100 ohms	100	200	600	mV
V_{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I_{RSDS}	Differential driver output current	1	2	6	mA
V_{THD}	Input voltage differential	100	—	—	mV
V_{CM}	Input common mode voltage	0.3	—	1.5	V
T_R, T_F	Output rise and fall times, 20% to 80%	—	500	—	ps
T_{ODUTY}	Output clock duty cycle	45	50	55	%

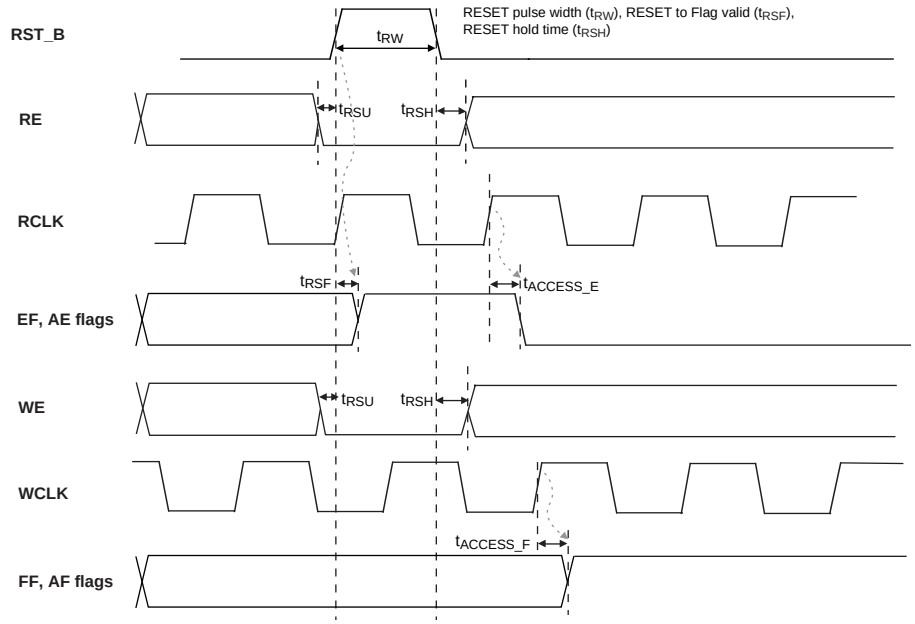
Note: Data is for 2mA drive. Other differential driver current options are available.

Figure 3-10. FIFO Reset Waveform



Note: RE and WE must be deactivated t_{RSU} before the Positive FIFO reset edge and enabled t_{RSH} after the FIFO reset negative edge.

Figure 3-11. Read Pointer Reset Waveform



Note: RE and WE must be deactivated t_{RSU} before the Positive FIFO reset edge and enabled t_{RSH} after the FIFO reset negative edge.

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
M4	PL43B	6	
P1	PL45A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
R1	PL45B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
R2	XRES	-	
P3	TEMP	6	
R3	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
N4	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
T3	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
T2	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
N5	PB5D	5	VREF1_5
P5	PB8A	5	
R5	PB8B	5	
T4	PB9A	5	
T5	PB9B	5	
R6	PB12A	5	PCLKT5_3
T6	PB12B	5	PCLKC5_3
L5	PB13C	5	
P6	PB15A	5	PCLKT5_0
T7	PB15B	5	PCLKC5_0
M7	PB15D	5	VREF2_5
R8	PB16A	5	PCLKT5_1
T8	PB16B	5	PCLKC5_1
N7	PB17A	5	PCLKT5_2
N8	PB17B	5	PCLKC5_2
R9	PB20A	5	
T9	PB20B	5	
M8	PB21A	5	
M9	PB21B	5	
P8	PB24A	5	
P9	PB24B	5	
T10	PB28A	4	
R11	PB28B	4	
N9	PB31A	4	
N10	PB31B	4	
T11	PB32A	4	
R12	PB32B	4	
P11	PB35A	4	PCLKT4_2
M10	PB35B	4	PCLKC4_2
T12	PB36A	4	PCLKT4_1
P12	PB36B	4	PCLKC4_1
T13	PB37A	4	PCLKT4_0
T14	PB37B	4	PCLKC4_0
R15	PB37C	4	VREF2_4

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
C5	A_VDDIB1_L	-	
A5	A_HDINP1_L	-	PCS 360 CH 1 IN P
B5	A_HDINN1_L	-	PCS 360 CH 1 IN N
A4	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B4	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
C4	A_VDDOB1_L	-	
B3	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
C3	A_VDDOB0_L	-	
A3	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
B2	A_HDINN0_L	-	PCS 360 CH 0 IN N
A2	A_HDINP0_L	-	PCS 360 CH 0 IN P
C2	A_VDDIB0_L	-	
A1	GND	-	
A16	GND	-	
B10	GND	-	
C13	GND	-	
D15	GND	-	
D3	GND	-	
E11	GND	-	
F13	GND	-	
G14	GND	-	
G2	GND	-	
G8	GND	-	
H10	GND	-	
J7	GND	-	
K15	GND	-	
K3	GND	-	
K9	GND	-	
M6	GND	-	
N11	GND	-	
N14	GND	-	
N2	GND	-	
P10	GND	-	
P4	GND	-	
R13	GND	-	
R7	GND	-	
G10	VCC	-	
G7	VCC	-	
G9	VCC	-	
H7	VCC	-	
H8	VCC	-	
H9	VCC	-	
J10	VCC	-	
J8	VCC	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
N17	GND	-		GND	-	
N18	GND	-		GND	-	
N19	GND	-		GND	-	
N20	GND	-		GND	-	
P11	GND	-		GND	-	
P12	GND	-		GND	-	
P13	GND	-		GND	-	
P14	GND	-		GND	-	
P15	GND	-		GND	-	
P16	GND	-		GND	-	
P17	GND	-		GND	-	
P18	GND	-		GND	-	
P19	GND	-		GND	-	
P20	GND	-		GND	-	
R10	GND	-		GND	-	
R11	GND	-		GND	-	
R12	GND	-		GND	-	
R13	GND	-		GND	-	
R14	GND	-		GND	-	
R15	GND	-		GND	-	
R16	GND	-		GND	-	
R17	GND	-		GND	-	
R18	GND	-		GND	-	
R19	GND	-		GND	-	
R20	GND	-		GND	-	
R21	GND	-		GND	-	
T10	GND	-		GND	-	
T11	GND	-		GND	-	
T12	GND	-		GND	-	
T13	GND	-		GND	-	
T14	GND	-		GND	-	
T15	GND	-		GND	-	
T16	GND	-		GND	-	
T17	GND	-		GND	-	
T18	GND	-		GND	-	
T19	GND	-		GND	-	
T20	GND	-		GND	-	
T21	GND	-		GND	-	
U11	GND	-		GND	-	
U12	GND	-		GND	-	
U13	GND	-		GND	-	
U14	GND	-		GND	-	
U15	GND	-		GND	-	
U16	GND	-		GND	-	
U17	GND	-		GND	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT24A	1	MPI_TEA	PT30A	1	MPI_TEA
J18	PT23D	1	D14/MPI_DATA14	PT28D	1	D14/MPI_DATA14
K18	PT23C	1	DP1/MPI_PAR1	PT28C	1	DP1/MPI_PAR1
E20	PT23B	1	A21/MPI_BURST	PT27B	1	A21/MPI_BURST
F20	PT23A	1	D15/MPI_DATA15	PT27A	1	D15/MPI_DATA15
C23	B_REFCLKP_L	-		B_REFCLKP_L	-	
D23	B_REFCLKN_L	-		B_REFCLKN_L	-	
B23	VCC12	-		VCC12	-	
H21	B_VDDIB3_L	-		B_VDDIB3_L	-	
F21	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
G21	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D21	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D22	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G22	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
F22	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H22	B_VDDIB2_L	-		B_VDDIB2_L	-	
H24	B_VDDIB1_L	-		B_VDDIB1_L	-	
G23	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
H23	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
A24	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
B24	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-		B_VDDOB1_L	-	
B25	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-		B_VDDOB0_L	-	
A25	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
G25	B_HDINN0_L	-	PCS 361 CH 0 IN N	B_HDINN0_L	-	PCS 361 CH 0 IN N
F25	B_HDINP0_L	-	PCS 361 CH 0 IN P	B_HDINP0_L	-	PCS 361 CH 0 IN P
H25	B_VDDIB0_L	-		B_VDDIB0_L	-	
H26	A_VDDIB3_L	-		A_VDDIB3_L	-	
F26	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
G26	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
D26	A_VDDOB3_L	-		A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
D27	A_VDDOB2_L	-		A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
G27	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
F27	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
H27	A_VDDIB2_L	-		A_VDDIB2_L	-	
F29	A_VDDIB1_L	-		A_VDDIB1_L	-	
G28	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
H28	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A29	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B29	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
D29	A_VDDOB1_L	-		A_VDDOB1_L	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D7	B_VDDIB0_R	-		B_VDDIB0_R	-	
E10	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
F10	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
K10	VCC12	-		VCC12	-	
A11	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D10	B_VDDOB0_R	-		B_VDDOB0_R	-	
B11	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D11	B_VDDOB1_R	-		B_VDDOB1_R	-	
B12	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L10	VCC12	-		VCC12	-	
A12	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
F11	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
E11	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
G11	VCC12	-		VCC12	-	
D8	B_VDDIB1_R	-		B_VDDIB1_R	-	
G12	VCC12	-		VCC12	-	
D9	B_VDDIB2_R	-		B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-		VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-		B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-		B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-		VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-		VCC12	-	
E9	B_VDDIB3_R	-		B_VDDIB3_R	-	
L13	VCC12	-		VCC12	-	
J11	B_REFCLKN_R	-		B_REFCLKN_R	-	
H11	B_REFCLKP_R	-		B_REFCLKP_R	-	
M15	PT61D	1	HDC/SI	PT77D	1	HDC/SI
M16	PT61C	1	LDCN/SCS	PT77C	1	LDCN/SCS
F14	PT59B	1	D8/MPI_DATA8	PT77B	1	D8/MPI_DATA8
G14	PT59A	1	CS1/MPI_CS1	PT77A	1	CS1/MPI_CS1
L15	PT58D	1	D9/MPI_DATA9	PT75D	1	D9/MPI_DATA9
L14	PT58C	1	D10/MPI_DATA10	PT75C	1	D10/MPI_DATA10
D14	PT57B	1	CS0N/MPI_CS0N	PT75B	1	CS0N/MPI_CS0N
E14	PT57A	1	RDN/MPI_STRB_N	PT75A	1	RDN/MPI_STRB_N
L16	PT55D	1	WRN/MPI_WR_N	PT74D	1	WRN/MPI_WR_N
K16	PT55C	1	D7/MPI_DATA7	PT74C	1	D7/MPI_DATA7
G15	PT55B	1	D6/MPI_DATA6	PT74B	1	D6/MPI_DATA6

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K20	GND	-		GND	-	
K23	GND	-		GND	-	
K26	GND	-		GND	-	
K28	GND	-		GND	-	
K6	GND	-		GND	-	
K9	GND	-		GND	-	
L12	GND	-		GND	-	
L32	GND	-		GND	-	
L4	GND	-		GND	-	
M10	GND	-		GND	-	
M17	GND	-		GND	-	
M24	GND	-		GND	-	
N29	GND	-		GND	-	
N7	GND	-		GND	-	
P15	GND	-		GND	-	
P20	GND	-		GND	-	
P3	GND	-		GND	-	
P31	GND	-		GND	-	
R10	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
T15	GND	-		GND	-	
T17	GND	-		GND	-	
T18	GND	-		GND	-	
T20	GND	-		GND	-	
T28	GND	-		GND	-	
T6	GND	-		GND	-	
U16	GND	-		GND	-	
U19	GND	-		GND	-	
U23	GND	-		GND	-	
U32	GND	-		GND	-	
U4	GND	-		GND	-	
V12	GND	-		GND	-	
V16	GND	-		GND	-	
V19	GND	-		GND	-	
V3	GND	-		GND	-	
V31	GND	-		GND	-	
W15	GND	-		GND	-	
W17	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W29	GND	-		GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP27	PB26A	5	
AP26	PB26B	5	
AK25	PB26C	5	
AK24	PB26D	5	
AN25	PB29A	5	
AN24	PB29B	5	
AE22	PB29C	5	
AE21	PB29D	5	
AM26	PB31A	5	
AM25	PB31B	5	
AF22	PB31C	5	
AF21	PB31D	5	
AN23	PB47A	5	
AN22	PB47B	5	
AP23	PB57A	5	
AP22	PB57B	5	
AG21	PB57C	5	
AG20	PB57D	5	
AP25	PB50A	5	PCLKT5_3
AP24	PB50B	5	PCLKC5_3
AD21	PB50C	5	PCLKT5_4
AD20	PB50D	5	PCLKC5_4
AL23	PB51A	5	PCLKT5_5
AL22	PB51B	5	PCLKC5_5
AH24	PB51C	5	
AH23	PB51D	5	
AM23	PB53A	5	PCLKT5_0
AM22	PB53B	5	PCLKC5_0
AJ24	PB53C	5	
AJ23	PB53D	5	VREF2_5
AN21	PB54A	5	PCLKT5_1
AN20	PB54B	5	PCLKC5_1
AE19	PB54C	5	PCLKT5_6
AD19	PB54D	5	PCLKC5_6
AK21	PB55A	5	PCLKT5_2
AK20	PB55B	5	PCLKC5_2
AK23	PB55C	5	PCLKT5_7
AK22	PB55D	5	PCLKC5_7
AL20	PB58A	5	
AL19	PB58B	5	
AG19	PB58C	5	
AF19	PB58D	5	
AP21	PB61A	5	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP20	PB61B	5	
AH21	PB61C	5	
AH20	PB61D	5	
AM20	PB63A	5	
AM19	PB63B	5	
AJ21	PB63C	5	
AJ20	PB63D	5	
AK19	PB66A	5	
AK18	PB66B	5	
AE18	PB66C	5	
AD18	PB66D	5	
AN19	PB69A	5	
AN18	PB69B	5	
AG18	PB69C	5	
AF18	PB69D	5	
AP19	PB71A	5	
AP18	PB71B	5	
AJ18	PB71C	5	
AH18	PB71D	5	
AP17	PB73A	4	
AP16	PB73B	4	
AJ17	PB73C	4	
AH17	PB73D	4	
AN17	PB75A	4	
AN16	PB75B	4	
AE17	PB75C	4	
AD17	PB75D	4	
AK17	PB78A	4	
AK16	PB78B	4	
AG17	PB78C	4	
AF17	PB78D	4	
AM16	PB81A	4	
AM15	PB81B	4	
AJ15	PB81C	4	
AJ14	PB81D	4	
AL16	PB83A	4	
AL15	PB83B	4	
AG16	PB83C	4	
AF16	PB83D	4	
AP15	PB86A	4	
AP14	PB86B	4	
AH15	PB86C	4	
AH14	PB86D	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN8	PB123B	4	
AG11	PB123C	4	
AG10	PB123D	4	
AP7	PB125A	4	
AP6	PB125B	4	
AG13	PB125C	4	
AG12	PB125D	4	
AN7	PB127A	4	
AN6	PB127B	4	
AK9	PB127C	4	
AK8	PB127D	4	
AP5	PB129A	4	
AP4	PB129B	4	
AD11	PB129C	4	
AE11	PB129D	4	
AM7	PB131A	4	
AM6	PB131B	4	
AJ9	PB131C	4	
AJ8	PB131D	4	
AP3	PB133A	4	
AN3	PB133B	4	
AF10	PB133C	4	
AE10	PB133D	4	
AL7	PB135A	4	
AL6	PB135B	4	
AK7	PB135C	4	
AK6	PB135D	4	
AN5	PB138A	4	
AN4	PB138B	4	
AH9	PB138C	4	VREF1_4
AH8	PB138D	4	
AM3	PB139A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB139B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB139C	4	
AG8	PB139D	4	
AN2	PB141A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB141B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB141C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB141D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-	
AF8	PROBE_GND	-	
AG7	PR117D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR117C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL4	PR117B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR117A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR116D	3	
AD9	PR116C	3	
AH4	PR116B	3	
AJ4	PR116A	3	
AK5	PR115D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR115C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR115B	3	
AL1	PR115A	3	
AH5	PR112D	3	
AG5	PR112C	3	
AL2	PR112B	3	
AK2	PR112A	3	
AB9	PR109D	3	
AC9	PR109C	3	
AH1	PR109B	3	
AG1	PR109A	3	
AE8	PR107D	3	VREF2_3
AD8	PR107C	3	
AJ3	PR107B	3	
AH3	PR107A	3	
AD7	PR104D	3	
AC7	PR104C	3	
AJ2	PR104B	3	
AH2	PR104A	3	
AF6	PR103D	3	
AF5	PR103C	3	
AF4	PR103B	3	
AE4	PR103A	3	
AD6	PR99D	3	
AC6	PR99C	3	
AG2	PR99B	3	
AF2	PR99A	3	
AC8	PR98D	3	
AB8	PR98C	3	
AK1	PR98B	3	
AJ1	PR98A	3	
AB10	PR96D	3	
AA10	PR96C	3	
AF3	PR96B	3	
AE3	PR96A	3	
AE5	PR94D	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
T16	GND	-		GND	-	
T19	GND	-		GND	-	
T24	GND	-		GND	-	
T27	GND	-		GND	-	
T32	GND	-		GND	-	
U18	GND	-		GND	-	
U20	GND	-		GND	-	
U23	GND	-		GND	-	
U25	GND	-		GND	-	
U36	GND	-		GND	-	
U7	GND	-		GND	-	
G36	GND	-		GND	-	
G7	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V24	GND	-		GND	-	
V26	GND	-		GND	-	
V4	GND	-		GND	-	
V40	GND	-		GND	-	
W12	GND	-		GND	-	
W16	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W25	GND	-		GND	-	
W27	GND	-		GND	-	
W31	GND	-		GND	-	
Y17	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y22	GND	-		GND	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AA22	VCC	-		VCC	-	
AA24	VCC	-		VCC	-	
AA25	VCC	-		VCC	-	
AA26	VCC	-		VCC	-	
AB17	VCC	-		VCC	-	
AB18	VCC	-		VCC	-	
AB19	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
AB22	VCC	-		VCC	-	
AB24	VCC	-		VCC	-	

Lead-Free Packaging

Commercial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.