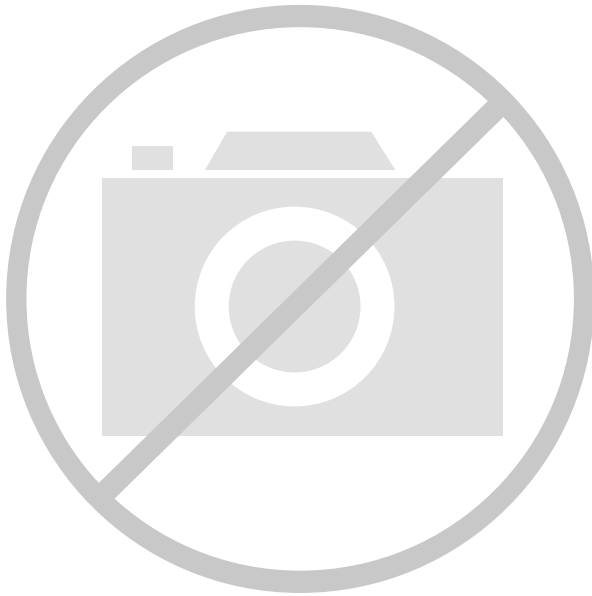




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

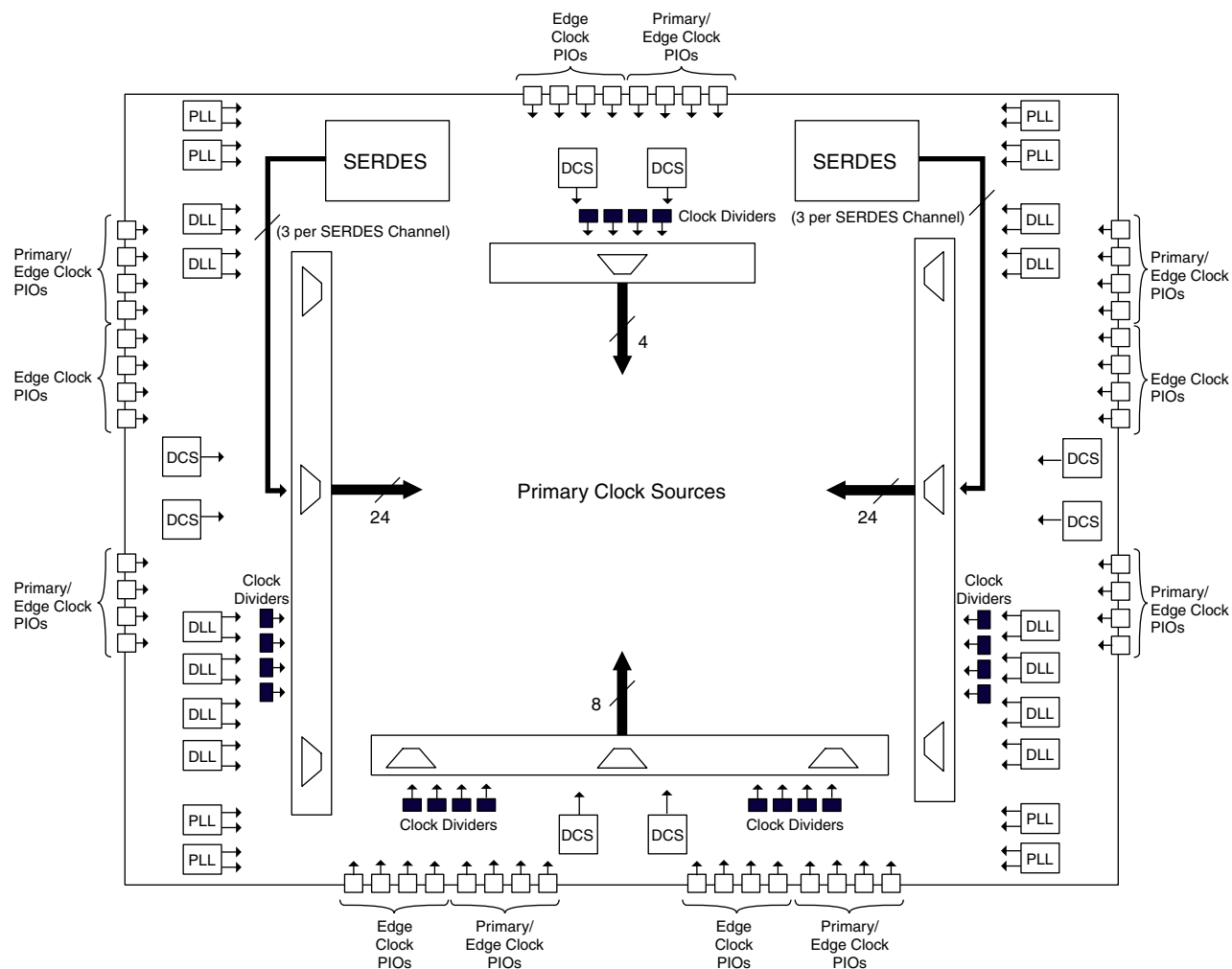
Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BCBGA, FCBGA
Supplier Device Package	1152-CFCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga40e-5fc1152c

- Two outputs per PLL
- Clock divider outputs
- Digital Clock Select (DCS) block outputs
- Three outputs per SERDES quad

Figure 2-5 shows the arrangement of the primary clock sources.

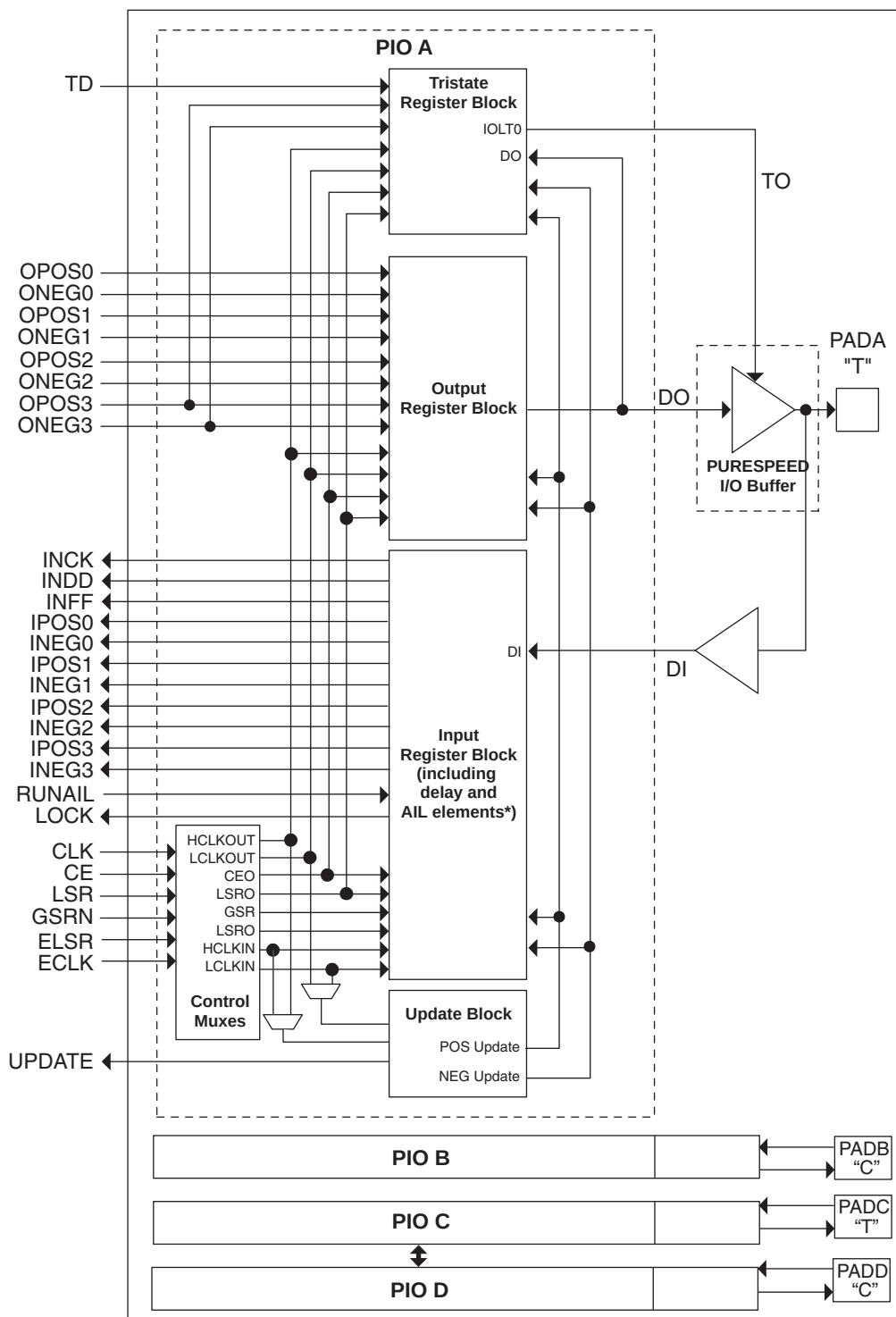
Figure 2-5. Clock Sources



Primary Clock Routing

The clock routing structure in LatticeSC devices consists of 12 Primary Clock lines per quadrant. The primary clocks are generated from 64:1 MUXs located in each quadrant. Three of the inputs to each 64:1 MUX comes from local routing, one is connected to GND and rest of the 60 inputs are from the primary clock sources. Figure 2-6 shows this clock routing.

Figure 2-17. PIC Diagram



*AIL only on A or C pads located on the left, right and bottom of the device.

The A/B PIOs on the left and the right of the device can be paired to form a differentiated driver. The A/B and C/D PIOs on all sides of the device can be paired to form differential receivers. Either A or C PIOs on all sides except the one on top also provide a connection to an adaptive input logic capability that facilitates the implementation of

Table 2-9. Supported Input Standards

Input Standard	V _{REF} (Nom.)	V _{CCIO} ¹ (Nom.)	On-chip Termination
Single Ended Interfaces			
LVTTL33 ³	—	3.3	None
LVC MOS 33, 25, 18, 15, 12 ³	—	3.3/2.5/1.8/1.5/1.2	None
PCI33, PCIX33, AGP1X33 ³	—	3.3	None
PCIX15	0.75	1.5 ²	None / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
AGP2X33	1.32	—	None
HSTL18_I, II	0.9	1.8 ²	None / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
HSTL18_III, IV	1.08	1.8 ²	None / V _{CCIO} : 50
HSTL15_I, II	0.75	1.5 ²	None / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
HSTL15_III, IV	0.9	1.5 ²	None / V _{CCIO} : 50
SSTL33_I, II	1.5	3.3	None
SSTL25_I, II	1.25	2.5 ²	None / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
SSTL18_I, II	0.9	1.8 ²	None / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
GTL+, GTL	1.0 / 0.8	1.5 / 1.2 ²	None / V _{CCIO} : 50
Differential Interfaces			
SSTL18D_I, II	—	1.8 ²	None / Diff: 120, 150, 220, 420/ Diff to V _{CMT} : 120, 150, 220, 420 / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
SSTL25D_I, II	—	2.5 ²	None / Diff: 120, 150, 220, 420/ Diff to V _{CMT} : 120, 150, 220, 420 / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
SSTL33D_I, II	—	3.3	None
HSTL15D_I, II	—	1.5 ²	None / Diff: 120, 150, 220, 420/ Diff to V _{CMT} : 120, 150, 220, 420 / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
HSTL18D_I, II	—	1.8 ²	None / Diff: 120, 150, 220, 420/ Diff to V _{CMT} : 120, 150, 220, 420 / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
LVDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V _{CMT} : 120, 150, 220, 240
Mini-LVDS	—	—	None / Diff: 120, 150 / Diff to V _{CMT} : 120, 150
BLVDS25	—	—	None
MLVDS25	—	—	None
RSDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V _{CMT} : 120, 150, 220, 240
LVPECL33	—	≤2.5	None / Diff: 120, 150, 220, 240/ Diff to V _{CMT} : 120, 150, 220, 240

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.

2. V_{CCIO} needed for on-chip termination to V_{CCIO}/2 or V_{CCIO} only. V_{CCIO} is not specified for off-chip termination or V_{TT} termination.

3. All ratioed input buffers and dedicated pin input buffers include hysteresis with a typical value of 50mV.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		2	—	1000	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		1.5625	—	1000	MHz
f_{VCO}	PLL VCO Frequency		100	—	1000	MHz
f_{PFD}	Phase Detector Input Frequency		2	—	700	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected (at 50% levels)	45	—	55	%
t_{OPJIT}^1	Output Clock Period Jitter	$2 \text{ MHz} \leq f_{PFD} \leq 10 \text{ MHz}$	—	—	200	ps
		$f_{PFD} > 10 \text{ MHz}$	—	—	100	ps
t_{CPJIT}^1	Output Clock Cycle-to-Cycle Jitter		—	—	100	ps
t_{SKEW}	Output Clock-to-Clock Skew (Between Two Outputs with the Same Phase Setting)		—	—	20	ps
t_{LOCK}	PLL Lock-in Time		—	—	1	ms
t_{IPJIT}	Input Clock Period Jitter		—	—	± 250	ps
t_{HI}	Input Clock High Time	At 80% level	350	—	—	ps
t_{LO}	Input Clock Low Time	At 20% level	350	—	—	ps
t_{RSWA}	Analog Reset Signal Pulse Width		100	—	—	ns
t_{RSWD}	Digital Reset Signal Pulse Width		3	—	—	ns
t_{DEL}	Timeshift Delay Step Size		40	80	120	ps
t_{RANGE}	Timeshift Delay Range		—	± 560	—	ps
f_{SS}	Spread Spectrum Modulation Frequency		30	—	500	KHz
% Spread	Percentage Downspread for SS Mode		0.5	—	1.5	%
	VCO Clock Phase Adjustment Accuracy		-5	—	5	°

1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps

Signal Descriptions (Cont.)

Signal Name	I/O	Description
MPI_STRBN	I	Driven active low indicates the start of a transaction on the PowerPC bus. MPI will strobe the address bus at next rising edge of clock.
MPI_ADDR[31:14]	I	Address bus driven by a PowerPC bus master. Only 18-bit width is needed. It has to be the least significant bit of the PowerPC 32-bit address A[31:14].
MPI_DAT[n:0]	I/O	Selectable data bus width from 8, and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
MPI_PAR[m:0]	I/O	Selectable parity bus width from 1, 2, and 3-bit. MPI_DP[0] for MPI_D[7:0], MPI_DP[1] for MPI_D[15:8] and MPI_DP[2] for MPI_D[23:16].
MPI_TA	O	Transfer acknowledge. Driven active low indicates that MPI received the data on the write cycle or returned data on the read cycle.
MPI_TEA	O	Transfer Error Acknowledge. Driven active low indicates that MPI detects a bus error on the internal system bus for current transaction.
MPI_RETRY	O	Active low MPI Retry requests the MPC860 to relinquish the bus and retry the cycle.
Multi-chip Alignment (User I/O if not used.)		
MCA_DONE_OUT	O	Multi-chip alignment done output (to second MCA chip)
MCA_DONE_IN	I	Multi-chip alignment done input (from second MCA chip)
MCA_CLK_P[1:2]_OUT	O	Multi-chip alignment clock [1:2] output (sourced by MCA master chip)
MCA_CLK_P[1:2]_IN	I	Multi-chip alignment clock [1:2] input (from MCA master chip)
TEMP	—	Temperature sensing diode pin. Dedicated pin. Accuracy is typically +/- 10°C.
Miscellaneous Dedicated Pins		
XRES	—	External reference resistor between this pin and ground. The reference resistor is used to calibrate the programmable terminating resistors used in the I/Os. Dedicated pin. Value: 1K ± 1% ohm.
DIFFRx	—	Only used if a differential driver is used in a bank. This DIFFRx must be connected to ground via an external 1K ± 1% ohm resistor for all banks that have a differential driver.
SERDES Block (Dedicated Pins)		
[A:D]_HDINPx_[L/R]	I	High-speed input (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDINNx_[L/R]	I	High-speed input (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTPx_[L/R]	O	High-speed output (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTNx_[L/R]	O	High-speed output (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_REFCLKP_[L/R]	I	Ref clock input (positive), aux channel on left [L] or right [R] side of device.
[A:D]_REFCLKN_[L/R]	I	Ref clock input (negative), aux channel on left [L] or right [R] side of device.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
RESP_[ULC/URC]	—	Calibration resistor to be placed between this pin and either ground or RESPN_[ULC/URC]. RESPN_[ULC/URC] is available on select packages. If available, connection of calibration resistor between RESP_[ULC/URC] and RESPN_[ULC/URC] takes precedence over connection of calibration resistor between RESP_[ULC/URC] and ground. Note: only one per side of the device. Value: 4.02K ohm +/- 1% ohm.
RESPN_[ULC/URC]	—	Available on selected packages. If available, calibration resistor should be placed between RESP_[ULC/URC] and RESPN_[ULC/URC] instead of between RESP_[ULC/URC] and ground. Note: only one per side of the device. Value: 4.02K ohm +/- 1% ohm.
[A:D]_VDDIBx_[L/R]	—	Input buffer power supply for channel x (1.2V/1.5V) on left [L] or right [R] side of device.
[A:D]_VDDOBx_[L/R]	—	Output buffer power supply for channel x (1.2V/1.5V) on left [L] or right [R] side of device.
[A:D]_VDDAX25_[L/R]	—	Auxiliary power for input and output termination (2.5V) on left [L] or right [R] side of device.

1. The ispLEVER software tools may specify VDDR_X, VDDT_X, VDDP and VCCL pins. These pins should be considered VCC12 pins.
Note: Signals listed as Signal A / Signal B define the same physical pin that is used for different functions based on configuration mode.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF4	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AE5	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AG3	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AH2	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AD6	PB4C	5		PB4C	5	
AJ2	PB5A	5		PB5A	5	
AK2	PB5B	5		PB5B	5	
AD7	PB5C	5		PB5C	5	
AD8	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AH3	PB7A	5		PB11A	5	
AJ3	PB7B	5		PB11B	5	
AF9	PB7C	5		PB11C	5	
AE10	PB7D	5		PB11D	5	
AK3	PB8A	5		PB12A	5	
AJ4	PB8B	5		PB12B	5	
AE11	PB9A	5		PB13A	5	
AF10	PB9B	5		PB13B	5	
AK4	PB11A	5		PB16A	5	
AK5	PB11B	5		PB16B	5	
AH10	PB12A	5	PCLKT5_3	PB20A	5	PCLKT5_3
AH11	PB12B	5	PCLKC5_3	PB20B	5	PCLKC5_3
AF13	PB12C	5	PCLKT5_4	PB20C	5	PCLKT5_4
AE14	PB12D	5	PCLKC5_4	PB20D	5	PCLKC5_4
AK6	PB13A	5	PCLKT5_5	PB21A	5	PCLKT5_5
AK7	PB13B	5	PCLKC5_5	PB21B	5	PCLKC5_5
AF14	PB13C	5		PB21C	5	
AJ11	PB15A	5	PCLKT5_0	PB23A	5	PCLKT5_0
AJ12	PB15B	5	PCLKC5_0	PB23B	5	PCLKC5_0
AH13	PB15D	5	VREF2_5	PB23D	5	VREF2_5
AK8	PB16A	5	PCLKT5_1	PB24A	5	PCLKT5_1
AK9	PB16B	5	PCLKC5_1	PB24B	5	PCLKC5_1
AH14	PB17A	5	PCLKT5_2	PB25A	5	PCLKT5_2
AG14	PB17B	5	PCLKC5_2	PB25B	5	PCLKC5_2
AK10	PB19A	5		PB28A	5	
AK11	PB19B	5		PB28B	5	
AH15	PB20A	5		PB29A	5	
AG15	PB20B	5		PB29B	5	
AH12	PB21A	5		PB31A	5	
AJ13	PB21B	5		PB31B	5	
AD15	PB21C	5		PB31C	5	
AE15	PB21D	5		PB31D	5	
AK12	PB23A	5		PB32A	5	
AK13	PB23B	5		PB32B	5	
AJ14	PB24A	5		PB33A	5	
AJ15	PB24B	5		PB33B	5	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AK14	PB25A	5		PB35A	5	
AK15	PB25B	5		PB35B	5	
AK16	PB27A	4		PB37A	4	
AK17	PB27B	4		PB37B	4	
AJ16	PB28A	4		PB38A	4	
AJ17	PB28B	4		PB38B	4	
AE16	PB28C	4		PB38C	4	
AH16	PB29A	4		PB39A	4	
AG16	PB29B	4		PB39B	4	
AK18	PB31A	4		PB41A	4	
AK19	PB31B	4		PB41B	4	
AH17	PB32A	4		PB42A	4	
AH18	PB32B	4		PB42B	4	
AG17	PB32D	4		PB42D	4	
AJ18	PB33A	4		PB43A	4	
AJ19	PB33B	4		PB43B	4	
AK20	PB35A	4	PCLKT4_2	PB46A	4	PCLKT4_2
AK21	PB35B	4	PCLKC4_2	PB46B	4	PCLKC4_2
AF18	PB36A	4	PCLKT4_1	PB47A	4	PCLKT4_1
AG18	PB36B	4	PCLKC4_1	PB47B	4	PCLKC4_1
AJ20	PB37A	4	PCLKT4_0	PB49A	4	PCLKT4_0
AJ21	PB37B	4	PCLKC4_0	PB49B	4	PCLKC4_0
AG19	PB37C	4	VREF2_4	PB49C	4	VREF2_4
AK22	PB39A	4	PCLKT4_5	PB51A	4	PCLKT4_5
AK23	PB39B	4	PCLKC4_5	PB51B	4	PCLKC4_5
AH19	PB39C	4		PB51C	4	
AK24	PB40A	4	PCLKT4_3	PB52A	4	PCLKT4_3
AK25	PB40B	4	PCLKC4_3	PB52B	4	PCLKC4_3
AE19	PB40C	4	PCLKT4_4	PB52C	4	PCLKT4_4
AE20	PB40D	4	PCLKC4_4	PB52D	4	PCLKC4_4
AE21	PB41A	4		PB53A	4	
AF21	PB41B	4		PB53B	4	
AG21	PB43A	4		PB55A	4	
AG22	PB43B	4		PB55B	4	
AH22	PB44A	4		PB56A	4	
AH23	PB44B	4		PB56B	4	
AH21	PB44C	4		PB56C	4	
AK28	PB45A	4		PB60A	4	
AK29	PB45B	4		PB60B	4	
AE22	PB45C	4		PB60C	4	
AJ28	PB47A	4		PB67A	4	
AH28	PB47B	4		PB67B	4	
AE24	PB47C	4	VREF1_4	PB67C	4	VREF1_4
AE25	PB47D	4		PB67D	4	
AJ29	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT24A	1	MPI_TEA	PT30A	1	MPI_TEA
J18	PT23D	1	D14/MPI_DATA14	PT28D	1	D14/MPI_DATA14
K18	PT23C	1	DP1/MPI_PAR1	PT28C	1	DP1/MPI_PAR1
E20	PT23B	1	A21/MPI_BURST	PT27B	1	A21/MPI_BURST
F20	PT23A	1	D15/MPI_DATA15	PT27A	1	D15/MPI_DATA15
C23	B_REFCLKP_L	-		B_REFCLKP_L	-	
D23	B_REFCLKN_L	-		B_REFCLKN_L	-	
B23	VCC12	-		VCC12	-	
H21	B_VDDIB3_L	-		B_VDDIB3_L	-	
F21	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
G21	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D21	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D22	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G22	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
F22	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H22	B_VDDIB2_L	-		B_VDDIB2_L	-	
H24	B_VDDIB1_L	-		B_VDDIB1_L	-	
G23	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
H23	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
A24	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
B24	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-		B_VDDOB1_L	-	
B25	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-		B_VDDOB0_L	-	
A25	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
G25	B_HDINN0_L	-	PCS 361 CH 0 IN N	B_HDINN0_L	-	PCS 361 CH 0 IN N
F25	B_HDINP0_L	-	PCS 361 CH 0 IN P	B_HDINP0_L	-	PCS 361 CH 0 IN P
H25	B_VDDIB0_L	-		B_VDDIB0_L	-	
H26	A_VDDIB3_L	-		A_VDDIB3_L	-	
F26	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
G26	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
D26	A_VDDOB3_L	-		A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
D27	A_VDDOB2_L	-		A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
G27	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
F27	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
H27	A_VDDIB2_L	-		A_VDDIB2_L	-	
F29	A_VDDIB1_L	-		A_VDDIB1_L	-	
G28	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
H28	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A29	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B29	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
D29	A_VDDOB1_L	-		A_VDDOB1_L	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F15	PT55A	1	D5/MPI_DATA5	PT74A	1	D5/MPI_DATA5
K14	PT54D	1	D4/MPI_DATA4	PT73D	1	D4/MPI_DATA4
K13	PT54C	1	D3/MPI_DATA3	PT73C	1	D3/MPI_DATA3
B15	PT53B	1	D2/MPI_DATA2	PT73B	1	D2/MPI_DATA2
A15	PT53A	1	D1/MPI_DATA1	PT73A	1	D1/MPI_DATA1
J14	PT51D	1	D16/PCLKC1_3/MPI_DATA16	PT71D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT51C	1	D17/PCLKT1_3/MPI_DATA17	PT71C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT51B	1	D0/MPI_DATA0	PT71B	1	D0/MPI_DATA0
B16	PT51A	1	QOUT/CEON	PT71A	1	QOUT/CEON
J13	PT50D	1	VREF2_1	PT70D	1	VREF2_1
H13	PT50C	1	D18/MPI_DATA18	PT70C	1	D18/MPI_DATA18
D15	PT50B	1	DOUT	PT70B	1	DOUT
E15	PT50A	1	MCA_DONE_IN	PT70A	1	MCA_DONE_IN
J16	PT49D	1	D19/PCLKC1_2/MPI_DATA19	PT69D	1	D19/PCLKC1_2/MPI_DATA19
J17	PT49C	1	D20/PCLKT1_2/MPI_DATA20	PT69C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT49B	1	MCA_CLK_P1_OUT	PT69B	1	MCA_CLK_P1_OUT
E16	PT49A	1	MCA_CLK_P1_IN	PT69A	1	MCA_CLK_P1_IN
H15	PT47D	1	D21/PCLKC1_1/MPI_DATA21	PT67D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT47C	1	D22/PCLKT1_1/MPI_DATA22	PT67C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT47B	1	MCA_CLK_P2_OUT	PT67B	1	MCA_CLK_P2_OUT
C16	PT47A	1	MCA_CLK_P2_IN	PT67A	1	MCA_CLK_P2_IN
L17	PT46D	1	MCA_DONE_OUT	PT66D	1	MCA_DONE_OUT
K17	PT46C	1	BUSYN/RCLK/SCK	PT66C	1	BUSYN/RCLK/SCK
E17	PT46B	1	DP0/MPI_PAR0	PT66B	1	DP0/MPI_PAR0
F17	PT46A	1	MPI_TA	PT66A	1	MPI_TA
G17	PT45D	1	D23/MPI_DATA23	PT65D	1	D23/MPI_DATA23
H17	PT45C	1	DP2/MPI_PAR2	PT65C	1	DP2/MPI_PAR2
A17	PT45B	1	PCLKC1_0	PT65B	1	PCLKC1_0
B17	PT45A	1	PCLKT1_0/MPI_CLK	PT65A	1	PCLKT1_0/MPI_CLK
G18	PT43D	1	DP3/PCLKC1_4/MPI_PAR3	PT63D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT43C	1	D24/PCLKT1_4/MPI_DATA24	PT63C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT43B	1	MPI_RETRY	PT63B	1	MPI_RETRY
F18	PT43A	1	A0/MPI_ADDR14	PT63A	1	A0/MPI_ADDR14
J18	PT42D	1	A1/MPI_ADDR15	PT61D	1	A1/MPI_ADDR15
J19	PT42C	1	A2/MPI_ADDR16	PT61C	1	A2/MPI_ADDR16
C20	PT42B	1	A3/MPI_ADDR17	PT61B	1	A3/MPI_ADDR17
C19	PT42A	1	A4/MPI_ADDR18	PT61A	1	A4/MPI_ADDR18
K18	PT41D	1	D25/PCLKC1_5/MPI_DATA25	PT60D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT41C	1	D26/PCLKT1_5/MPI_DATA26	PT60C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT41B	1	A5/MPI_ADDR19	PT60B	1	A5/MPI_ADDR19
E19	PT41A	1	A6/MPI_ADDR20	PT60A	1	A6/MPI_ADDR20
H19	PT39D	1	D27/MPI_DATA27	PT59D	1	D27/MPI_DATA27
H20	PT39C	1	VREF1_1	PT59C	1	VREF1_1
A18	PT39B	1	A7/MPI_ADDR21	PT59B	1	A7/MPI_ADDR21
B18	PT39A	1	A8/MPI_ADDR22	PT59A	1	A8/MPI_ADDR22

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W7	GND	-		GND	-	
AA14	VCC	-		VCC	-	
AA16	VCC	-		VCC	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AB13	VCC	-		VCC	-	
AB22	VCC	-		VCC	-	
N13	VCC	-		VCC	-	
N22	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	
P17	VCC	-		VCC	-	
P18	VCC	-		VCC	-	
P19	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
R15	VCC	-		VCC	-	
R17	VCC	-		VCC	-	
R18	VCC	-		VCC	-	
R20	VCC	-		VCC	-	
T14	VCC	-		VCC	-	
T16	VCC	-		VCC	-	
T19	VCC	-		VCC	-	
T21	VCC	-		VCC	-	
U14	VCC	-		VCC	-	
U15	VCC	-		VCC	-	
U17	VCC	-		VCC	-	
U18	VCC	-		VCC	-	
U20	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V14	VCC	-		VCC	-	
V15	VCC	-		VCC	-	
V17	VCC	-		VCC	-	
V18	VCC	-		VCC	-	
V20	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W14	VCC	-		VCC	-	
W16	VCC	-		VCC	-	
W19	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y15	VCC	-		VCC	-	
Y17	VCC	-		VCC	-	
Y18	VCC	-		VCC	-	
Y20	VCC	-		VCC	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
F25	B_HDINN0_L	-	PCS 361 CH 0 IN N
E25	B_HDINP0_L	-	PCS 361 CH 0 IN P
D28	B_VDDIB0_L	-	
G25	VCC12	-	
D29	A_VDDIB3_L	-	
C25	VCC12	-	
A25	A_HDINP3_L	-	PCS 360 CH 3 IN P
B25	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
E27	VCC12	-	
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
F26	A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
F27	A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E28	VCC12	-	
B28	A_HDINN2_L	-	PCS 360 CH 2 IN N
A28	A_HDINP2_L	-	PCS 360 CH 2 IN P
D30	A_VDDIB2_L	-	
C28	VCC12	-	
D31	A_VDDIB1_L	-	
C29	VCC12	-	
A29	A_HDINP1_L	-	PCS 360 CH 1 IN P
B29	A_HDINN1_L	-	PCS 360 CH 1 IN N
A30	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
E29	VCC12	-	
B30	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
F28	A_VDDOB1_L	-	
B31	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
F29	A_VDDOB0_L	-	
A31	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E30	VCC12	-	
B32	A_HDINN0_L	-	PCS 360 CH 0 IN N
A32	A_HDINP0_L	-	PCS 360 CH 0 IN P
D32	A_VDDIB0_L	-	
C32	VCC12	-	
E34	PL30A	7	
F34	PL30B	7	
F33	PL34A	7	
G33	PL34B	7	
K30	PL38A	7	
L30	PL38B	7	
G34	PL40A	7	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
H34	PL40B	7	
M32	PL53A	7	
N32	PL53B	7	
P28	PL53C	7	
R28	PL53D	7	
J34	PL55A	7	
K34	PL55B	7	
P30	PL55C	7	
R30	PL55D	7	
W34	PL73A	6	
Y34	PL73B	6	
W32	PL75A	6	
Y32	PL75B	6	
AA34	PL78A	6	
AB34	PL78B	6	
AC34	PL81A	6	
AD34	PL81B	6	
Y30	PL82A	6	
AA30	PL82B	6	
AB33	PL83A	6	
AC33	PL83B	6	
AC2	PR83B	3	
AB2	PR83A	3	
AA5	PR82B	3	
Y5	PR82A	3	
AD1	PR81B	3	
AC1	PR81A	3	
AB1	PR78B	3	
AA1	PR78A	3	
Y3	PR75B	3	
W3	PR75A	3	
Y1	PR73B	3	
W1	PR73A	3	
R5	PR55D	2	
P5	PR55C	2	
K1	PR55B	2	
J1	PR55A	2	
R7	PR53D	2	
P7	PR53C	2	
N3	PR53B	2	
M3	PR53A	2	
H1	PR40B	2	
G1	PR40A	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B22	PT61B	1	A3/MPI_ADDR17	PT69B	1	A3/MPI_ADDR17
B23	PT61A	1	A4/MPI_ADDR18	PT69A	1	A4/MPI_ADDR18
K23	PT60D	1	D25/PCLKC1_5/MPI_DATA25	PT66D	1	D25/PCLKC1_5/MPI_DATA25
J23	PT60C	1	D26/PCLKT1_5/MPI_DATA26	PT66C	1	D26/PCLKT1_5/MPI_DATA26
D22	PT60B	1	A5/MPI_ADDR19	PT66B	1	A5/MPI_ADDR19
E22	PT60A	1	A6/MPI_ADDR20	PT66A	1	A6/MPI_ADDR20
K22	PT59D	1	D27/MPI_DATA27	PT63D	1	D27/MPI_DATA27
J22	PT59C	1	VREF1_1	PT63C	1	VREF1_1
D23	PT59B	1	A7/MPI_ADDR21	PT63B	1	A7/MPI_ADDR21
C23	PT59A	1	A8/MPI_ADDR22	PT63A	1	A8/MPI_ADDR22
L23	PT57D	1	D28/PCLKC1_6/MPI_DATA28	PT61D	1	D28/PCLKC1_6/MPI_DATA28
M23	PT57C	1	D29/PCLKT1_6/MPI_DATA29	PT61C	1	D29/PCLKT1_6/MPI_DATA29
A24	PT57B	1	A9/MPI_ADDR23	PT61B	1	A9/MPI_ADDR23
B24	PT57A	1	A10/MPI_ADDR24	PT61A	1	A10/MPI_ADDR24
K25	PT56D	1	D30/PCLKC1_7/MPI_DATA30	PT58D	1	D30/PCLKC1_7/MPI_DATA30
J25	PT56C	1	D31/PCLKT1_7/MPI_DATA31	PT58C	1	D31/PCLKT1_7/MPI_DATA31
F23	PT56B	1	A11/MPI_ADDR25	PT58B	1	A11/MPI_ADDR25
F22	PT56A	1	A12/MPI_ADDR26	PT58A	1	A12/MPI_ADDR26
J26	PT55D	1	D11/MPI_DATA11	PT57D	1	D11/MPI_DATA11
K26	PT55C	1	D12/MPI_DATA12	PT57C	1	D12/MPI_DATA12
E23	PT55B	1	A13/MPI_ADDR27	PT57B	1	A13/MPI_ADDR27
E24	PT55A	1	A14/MPI_ADDR28	PT57A	1	A14/MPI_ADDR28
G23	PT53D	1	A16/MPI_ADDR30	PT55D	1	A16/MPI_ADDR30
G24	PT53C	1	D13/MPI_DATA13	PT55C	1	D13/MPI_DATA13
F26	PT53B	1	A15/MPI_ADDR29	PT55B	1	A15/MPI_ADDR29
F27	PT53A	1	A17/MPI_ADDR31	PT55A	1	A17/MPI_ADDR31
H25	PT52D	1	A19/MPI_TSI21	PT54D	1	A19/MPI_TSI21
H24	PT52C	1	A20/MPI_BDIP	PT54C	1	A20/MPI_BDIP
C25	PT52B	1	A18/MPI_TSI20	PT54B	1	A18/MPI_TSI20
C26	PT52A	1	MPI_TEA	PT54A	1	MPI_TEA
K24	PT51D	1	D14/MPI_DATA14	PT51D	1	D14/MPI_DATA14
J24	PT51C	1	DP1/MPI_PAR1	PT51C	1	DP1/MPI_PAR1
F24	PT51B	1	A21/MPI_BURST	PT51B	1	A21/MPI_BURST
F25	PT51A	1	D15/MPI_DATA15	PT51A	1	D15/MPI_DATA15
L26	D_REFCLKP_L	-		D_REFCLKP_L	-	
M26	D_REFCLKN_L	-		D_REFCLKN_L	-	
G27	VCC12	-		VCC12	-	
C29	D_VDDIB3_L	-		D_VDDIB3_L	-	
F28	VCC12	-		VCC12	-	
D26	D_HDINP3_L	-	PCS 363 CH 3 IN P	D_HDINP3_L	-	PCS 363 CH 3 IN P
E26	D_HDINN3_L	-	PCS 363 CH 3 IN N	D_HDINN3_L	-	PCS 363 CH 3 IN N
B25	D_HDOUTP3_L	-	PCS 363 CH 3 OUT P	D_HDOUTP3_L	-	PCS 363 CH 3 OUT P
D24	VCC12	-		VCC12	-	
A25	D_HDOUTN3_L	-	PCS 363 CH 3 OUT N	D_HDOUTN3_L	-	PCS 363 CH 3 OUT N
E25	D_VDDOB3_L	-		D_VDDOB3_L	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L8	VCCIO2	-		VCCIO2	-	
M3	VCCIO2	-		VCCIO2	-	
P7	VCCIO2	-		VCCIO2	-	
R4	VCCIO2	-		VCCIO2	-	
T12	VCCIO2	-		VCCIO2	-	
U8	VCCIO2	-		VCCIO2	-	
V3	VCCIO2	-		VCCIO2	-	
W11	VCCIO2	-		VCCIO2	-	
Y7	VCCIO2	-		VCCIO2	-	
AB3	VCCIO3	-		VCCIO3	-	
AC7	VCCIO3	-		VCCIO3	-	
AD11	VCCIO3	-		VCCIO3	-	
AE4	VCCIO3	-		VCCIO3	-	
AF8	VCCIO3	-		VCCIO3	-	
AG12	VCCIO3	-		VCCIO3	-	
AH3	VCCIO3	-		VCCIO3	-	
AJ7	VCCIO3	-		VCCIO3	-	
AK11	VCCIO3	-		VCCIO3	-	
AL4	VCCIO3	-		VCCIO3	-	
AM8	VCCIO3	-		VCCIO3	-	
AP3	VCCIO3	-		VCCIO3	-	
AR7	VCCIO3	-		VCCIO3	-	
AU4	VCCIO3	-		VCCIO3	-	
AL16	VCCIO4	-		VCCIO4	-	
AM13	VCCIO4	-		VCCIO4	-	
AM19	VCCIO4	-		VCCIO4	-	
AR11	VCCIO4	-		VCCIO4	-	
AR17	VCCIO4	-		VCCIO4	-	
AT14	VCCIO4	-		VCCIO4	-	
AT20	VCCIO4	-		VCCIO4	-	
AT8	VCCIO4	-		VCCIO4	-	
AW15	VCCIO4	-		VCCIO4	-	
AW21	VCCIO4	-		VCCIO4	-	
AW9	VCCIO4	-		VCCIO4	-	
AY12	VCCIO4	-		VCCIO4	-	
AY18	VCCIO4	-		VCCIO4	-	
AY6	VCCIO4	-		VCCIO4	-	
AL27	VCCIO5	-		VCCIO5	-	
AM24	VCCIO5	-		VCCIO5	-	
AM30	VCCIO5	-		VCCIO5	-	
AR26	VCCIO5	-		VCCIO5	-	
AR32	VCCIO5	-		VCCIO5	-	
AT23	VCCIO5	-		VCCIO5	-	
AT29	VCCIO5	-		VCCIO5	-	
AT35	VCCIO5	-		VCCIO5	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AW25	VCCIO5	-		VCCIO5	-	
AW31	VCCIO5	-		VCCIO5	-	
AW37	VCCIO5	-		VCCIO5	-	
AY22	VCCIO5	-		VCCIO5	-	
AY28	VCCIO5	-		VCCIO5	-	
AY34	VCCIO5	-		VCCIO5	-	
AB39	VCCIO6	-		VCCIO6	-	
AC36	VCCIO6	-		VCCIO6	-	
AD32	VCCIO6	-		VCCIO6	-	
AE40	VCCIO6	-		VCCIO6	-	
AF35	VCCIO6	-		VCCIO6	-	
AG31	VCCIO6	-		VCCIO6	-	
AH39	VCCIO6	-		VCCIO6	-	
AJ36	VCCIO6	-		VCCIO6	-	
AK32	VCCIO6	-		VCCIO6	-	
AL40	VCCIO6	-		VCCIO6	-	
AM35	VCCIO6	-		VCCIO6	-	
AP39	VCCIO6	-		VCCIO6	-	
AR36	VCCIO6	-		VCCIO6	-	
AU40	VCCIO6	-		VCCIO6	-	
AA40	VCCIO7	-		VCCIO7	-	
H36	VCCIO7	-		VCCIO7	-	
J40	VCCIO7	-		VCCIO7	-	
L35	VCCIO7	-		VCCIO7	-	
M39	VCCIO7	-		VCCIO7	-	
P36	VCCIO7	-		VCCIO7	-	
R40	VCCIO7	-		VCCIO7	-	
T31	VCCIO7	-		VCCIO7	-	
U35	VCCIO7	-		VCCIO7	-	
V39	VCCIO7	-		VCCIO7	-	
W32	VCCIO7	-		VCCIO7	-	
Y36	VCCIO7	-		VCCIO7	-	
AA14	VTT_2	2		VTT_2	2	
AA15	VTT_2	2		VTT_2	2	
R12	VTT_2	2		VTT_2	2	
V14	VTT_2	2		VTT_2	2	
AB14	VTT_3	3		VTT_3	3	
AB15	VTT_3	3		VTT_3	3	
AE14	VTT_3	3		VTT_3	3	
AJ13	VTT_3	3		VTT_3	3	
AH21	VTT_4	4		VTT_4	4	
AJ18	VTT_4	4		VTT_4	4	
AJ19	VTT_4	4		VTT_4	4	
AJ20	VTT_4	4		VTT_4	4	
AJ21	VTT_4	4		VTT_4	4	

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1101 - Power Estimation and Management for LatticeSC Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-6FFN1020I ¹	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-5FFN1020I ¹	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-6FCN1152I ²	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FCN1152I ²	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSC3GA80E-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Date	Version	Section	Change Summary
December 2011	02.4	DC and Switching Characteristics	Updated JTAG Port Timing Specifications table.