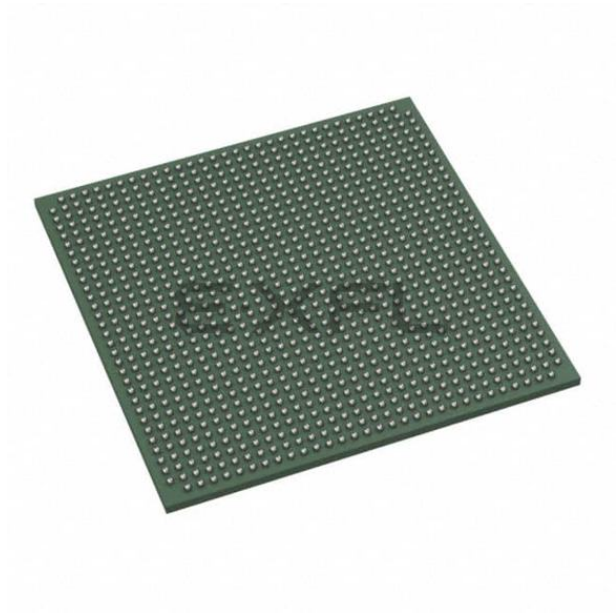
# Lattice Semiconductor Corporation - LFSC3GA40E-5FF1020C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 10000 |
| Number of Logic Elements/Cells | 40000 |
| Total RAM Bits | 4075520 |
| Number of I/O | 562 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1020-BBGA, FCBGA |
| Supplier Device Package | 1020-OFCBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga40e-5ff1020c |

*Table 1-1. LatticeSC Family Selection Guide*[1]

| Device | SC15 | SC25 | SC40 | SC80 | SC115 |
|---|---|---|---|---|---|
| LUT4s (K) | 15 | 25 | 40 | 80 | 115 |
| sysMEM Blocks (18Kb) | 56 | 104 | 216 | 308 | 424 |
| Embedded Memory (Mbits) | 1.03 | 1.92 | 3.98 | 5.68 | 7.8 |
| Max. Distributed Memory (Mbits) | 0.24 | 0.41 | 0.65 | 1.28 | 1.84 |
| Number of 3.8Gbps SERDES (Max.) | 8 | 16 | 16 | 32 | 32 |
| DLLs | 12 | 12 | 12 | 12 | 12 |
| Analog PLLs | 8 | 8 | 8 | 8 | 8 |
| MACO Blocks | 4 | 6 | 10 | 10 | 12 |
| **Package I/O/SERDES Combinations (1mm ball pitch)** | | | | | |
| 256-ball fpBGA (17 x 17mm) | 139/4 | | | | |
| 900-ball fpBGA (31 x 31mm) | 300/8 | 378/8 | | | |
| 1020-ball fcBGA (33 x 33mm)[2] | | 476/16 | 562/16 | | |
| 1152-ball fcBGA (35 x 35mm)[3] | | | 604/16 | 660/16 | 660/16 |
| 1704-ball fcBGA (42.5 x 42.5mm)[3] | | | | 904/32 | 942/32 |

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per PCN #02A-10.
3. Ceramic fcBGA converted to organic fcBGA per PCN #01A-10.

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

*Table 1-2. LatticeSCM Family*

| Device | SCM15 | SCM25 | SCM40 | SCM80 | SCM115 |
|---|---|---|---|---|---|
| flexiMAC Blocks<br>• 1GbE Mode<br>• 10GbE Mode<br>• PCI Express Mode | 1 | 2 | 2 | 2 | 4 |
| SPI4.2 Blocks | 1 | 2 | 2 | 2 | 2 |
| Memory Controller Blocks<br>• DDR/DDR2 DRAM Mode<br>• QDR II/II+ SRAM Mode<br>• RLDRAM I<br>• RLDRAM II CIO/SIO | 1 | 2 | 2 | 2 | 2 |
| Low-Speed CDR Blocks | 0 | 0 | 2 | 2 | 2 |
| PCI Express LTSSM (PHY) Blocks | 1 | 0 | 2 | 2 | 2 |

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

## Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

*Figure 2-3. Slice Diagram*

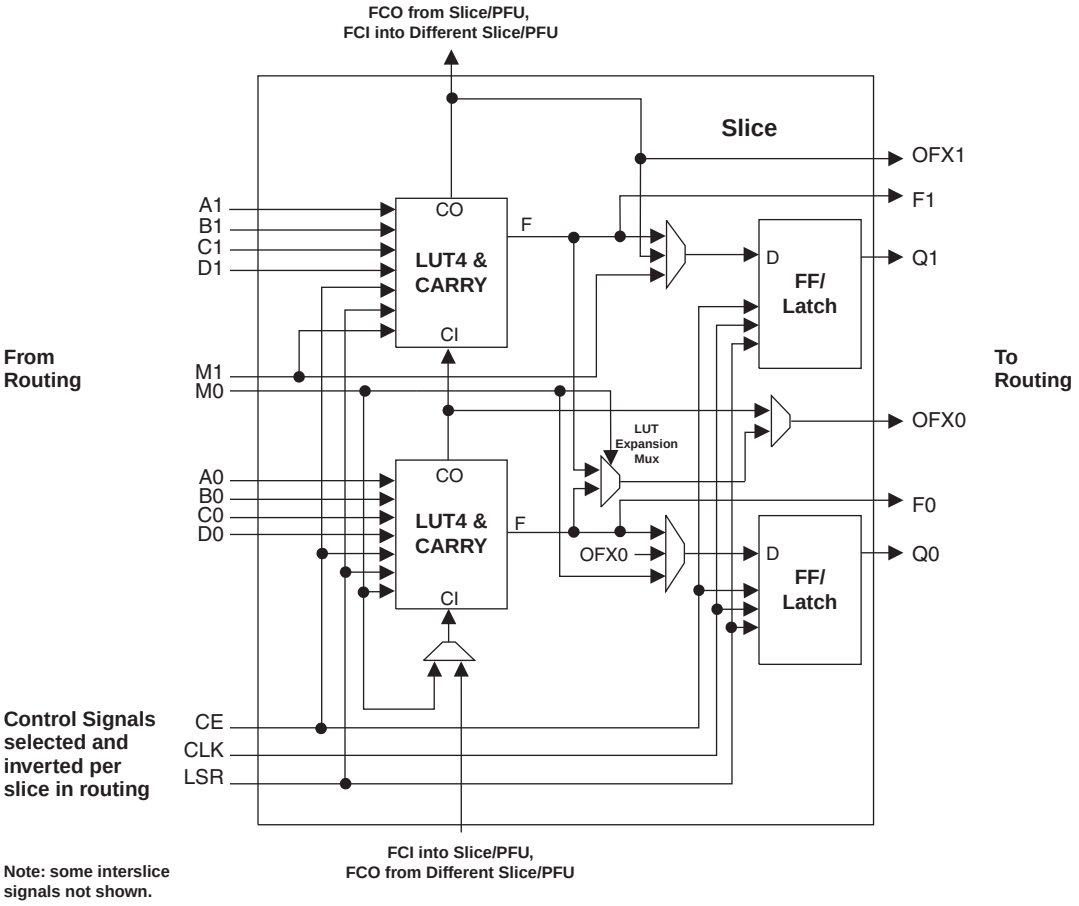


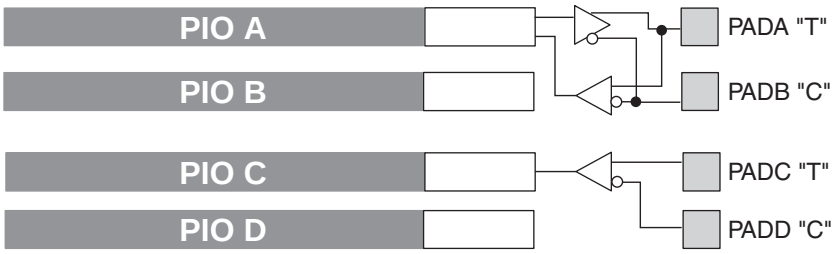

*Table 2-1. Slice Signal Descriptions*

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCI | Fast Carry In[1] |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register Outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice |
| Output | Inter-PFU signal | FCO | For the right most PFU the fast carry chain output[2] |

1. See Figure 2-2 for connection details.
2. Requires two PFUs.

high-speed interfaces in the LatticeSC devices. Figure 2-18 shows how differential receivers and drivers are arranged between PIOs.

***Figure 2-18. Differential Drivers and Receivers***




*Differential Driver only available on right and left of the device.

## PIO

The PIO contains five blocks: an input register block, output register block, tristate register block, update block, and a control logic block. These blocks contain registers for both single data rate (SDR), double data rate (DDR), and shift register operation along with the necessary clock and selection logic.

## Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 show the diagram of the input register block. The signal from the PURESPEED I/O buffer (DI) enters the input register block and can be used for three purposes, as a source for the combinatorial (INDD) and clock outputs (INCK), the input into the SDR register/latch block and the input to the delay block. The output of the delay block can be used as combinatorial (INDD) and clock (INCK) outputs, an input to the DDR/Shift Register Block or an input into the SDR register block.

### Input SDR Register/Latch Block

The SDR register/latch block has a latch and a register/latch that can be used in a variety of combinations to provide a registered or latched output (INFF). The latch operates off high-speed input clocks and latches data on the positive going edge. The register/latch operates off the low-speed input clock and registers/latches data on the positive going edge. Both the latch and the register/latch have a clock enable input that is driven by the input clock enable. In addition both have a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register and latch LSR inputs are driven from LSRI, which is generated from the PIO control MUX. The GSR inputs are driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

### Input Delay Block

The delay block uses 144 tapped delay lines to obtain coarse and fine delay resolution. These delays can be adjusted during configuration or automatically via DLL or AIL blocks. The Adaptive Input Logic (AIL) uses this delay block to adjust automatically the delay in the data path to ensure that it has sufficient setup and hold time.

The delay line in this block matches the delay line that is used in the 12 on-chip DLLs. The delay line can be set via configuration bits or driven from a calibration bus that allows the setting to be controlled either from one of the on-chip DLLs or user logic. Controlling the delay from one of the on-chip DLLs allow the delay to be calibrated to the DLL clock and hence compensated for the variations in process, voltage and temperature.

# LatticeSC/M Internal Timing Parameters[1]

**Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%**

| Parameter | Symbol | Description | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU Logic Mode Timing** | | | | | | | | | |
| $t_{LUT4\_PFU}$ | CTOF_DEL | LUT4 delay (A to D inputs to F output) | — | 0.045 | — | 0.050 | — | 0.054 | ns |
| $t_{LUT5\_PFU}$ | MTOOFX_DEL | LUT5 delay (inputs to output) | — | 0.152 | — | 0.172 | — | 0.192 | ns |
| $t_{LSR\_PFU}$ | LSR_DEL | Set/Reset to output (asynchronous) | — | 0.378 | — | 0.426 | — | 0.474 | ns |
| $t_{SUM\_PFU}$ | M_SET | Clock to Mux (M0,M1) input setup time | 0.113 | — | 0.131 | — | 0.148 | — | ns |
| $t_{HM\_PFU}$ | M_HLD | Clock to Mux (M0,M1) input hold time | -0.041 | — | -0.046 | — | -0.052 | — | ns |
| $t_{SUD\_PFU}$ | DIN_SET | Clock to D input setup time | 0.072 | — | 0.083 | — | 0.094 | — | ns |
| $t_{HD\_PFU}$ | DIN_HLD | Clock to D input hold time | -0.028 | — | -0.032 | — | -0.035 | — | ns |
| $t_{CK2Q\_PFU}$ | REG_DEL | Clock to Q delay, D-type register configuration | — | 0.224 | — | 0.252 | — | 0.279 | ns |
| $t_{LE2Q\_PFU}$ | LTCH_DEL | Clock to Q delay latch configuration | — | 0.294 | — | 0.331 | — | 0.367 | ns |
| $t_{LD2Q\_PFU}$ | TLTCH_DEL | D to Q throughput delay when latch is enabled | — | 0.300 | — | 0.338 | — | 0.376 | ns |
| **PFU Memory Mode Timing** | | | | | | | | | |
| $t_{CORAM\_PFU}$ | CLKTOF_DEL | Clock to Output | — | 0.575 | — | 0.649 | — | 0.724 | ns |
| $t_{SUDATA\_PFU}$ | DIN_SET | Data Setup Time | -0.024 | — | -0.026 | — | -0.027 | — | ns |
| $t_{HDATA\_PFU}$ | DIN_HLD | Data Hold Time | 0.075 | — | 0.084 | — | 0.094 | — | ns |
| $t_{SUADDR\_PFU}$ | WAD_SET | Address Setup Time | -0.176 | — | -0.196 | — | -0.215 | — | ns |
| $t_{HADDR\_PFU}$ | WAD_HLD | Address Hold Time | 0.110 | — | 0.124 | — | 0.138 | — | ns |
| $t_{SUWREN\_PFU}$ | WE_SET | Write/Read Enable Setup Time | 0.014 | — | 0.019 | — | 0.024 | — | ns |
| $t_{HWREN\_PFU}$ | WE_HLD | Write/Read Enable Hold Time | 0.078 | — | 0.086 | — | 0.094 | — | ns |
| **PIC Timing** | | | | | | | | | |
| **PIO Input/Output Buffer Timing** | | | | | | | | | |
| $t_{IN\_PIO}$ | IN_DEL | Input Buffer Delay(LVCMOS25) | — | 0.578 | — | 0.661 | — | 0.744 | ns |
| $t_{OUT\_PIO}$ | DOPADI_DEL | Output Buffer Delay(LVCMOS25) | — | 2.712 | — | 3.027 | — | 3.395 | ns |
| $t_{SUI\_PIO}$ | DIN_SET | Input Register Setup Time (Data Before Clock) | 0.277 | — | 0.312 | — | 0.348 | — | ns |
| $t_{HI\_PIO}$ | DIN_HLD | Input Register Hold Time (Data after Clock) | -0.267 | — | -0.306 | — | -0.345 | — | ns |
| $t_{COO\_PIO}$ | CK_DEL | Output Register Clock to Output Delay | — | 0.513 | — | 0.571 | — | 0.639 | ns |
| $t_{SUCE\_PIO}$ | CE_SET | Input Register Clock Enable Setup Time | — | 0.000 | — | 0.000 | — | 0.000 | ns |
| $t_{HCE\_PIO}$ | CE_HLD | Input Register Clock Enable Hold Time | — | 0.129 | — | 0.145 | — | 0.161 | ns |
| $t_{SULSR\_PIO}$ | LSR_SET | Set/Reset Setup Time | 0.057 | — | 0.060 | — | 0.063 | — | ns |
| $t_{HLSR\_PIO}$ | LSR_HLD | Set/Reset Hold Time | -0.151 | — | -0.159 | — | -0.169 | — | ns |
| $t_{LE2Q\_PIO}$ | CK_DEL | Input Register Clock to Q delay latch configuration | — | 0.335 | — | 0.372 | — | 0.410 | ns |
| $t_{LD2Q\_PIO}$ | DIN_DEL | Input Register D to Q throughput delay when latch is enabled | — | 0.578 | — | 0.647 | — | 0.717 | ns |

## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| D[n:0] | I/O | In parallel configuration modes, D[7:0] receives configuration data, and each pin is pull-up enabled. For slave serial mode, D0 is the data input.<br><br>D[7:3] is the output internal status for peripheral mode when RDN is low.<br><br>D[7:0] is also the first byte of MPI data pins.<br><br>In MPI configuration mode, MPI selectable data bus width from 8 and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction. |
| DP[m:0] | I/O | MPI selectable parity data bus width from 1, 2, and 3-bit DP[0] for D[7:0], DP[1] for D[15:8], and DP[2] for D[23:16]. |
| BUSYN/RCLK/SCK | O | During configuration in peripheral mode, high on BUSYN indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D[7] in asynchronous peripheral mode.<br><br>During configuration in slave parallel mode, low on BUSYN inhibits the external host from sending new data. The output is used by slave parallel and master serial modes only for decompression.<br><br>During configuration in master parallel and master byte modes, RCLK is a read clock output signal to an external memory. The RCLK frequency is the same as CCLK when used with uncompressed bitstreams. RCLK will be 1/8 the frequency of CCLK when the bitstream is compressed.<br><br>During configuration in SPI modes, SCK is generated by the device and connected to the CLK input of the FLASH memory. |
| **MPI Interface (Dedicated pin)** | | |
| MPI_IRQ_N | O | MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins. |
| **MPI Interface (User I/O if MPI is not used.)** | | |
| MPI_CS0N MPI_CS1 | I | MPI chip select pins, active low on MPI_CS0N while active high on MPI_CS1. Both have to be active during the whole transfer data phase. During transfer address phase, both can be inactive so that the decoding for them from address can be slow. If they are active during address phase, one cycle can be saved for sync read. |
| MPI_CLK | I | This is the PowerPC bus clock. It can be a source of the clock for embedded system bus. If MPI_CLK is used as system bus clock, MPI will be set into sync mode by default. All of the operation on PowerPC side of MPI are synchronized to the rising edge of this clock. |
| MPI_TSIZ[1:0] | I | Driven by a bus master to indicate the data transfer size for the transaction. 01 for byte, 10 for half-word, and 00 for word. |
| MPI_WR_N | I | Driven high indicates that a read access is in progress. Driven low indicates that a write access is in process. |
| MPI_BURST | I | Driven active low indicates that a burst transfer is in progress. Driven high indicates that the current transfer is not a burst. |
| MPI_BDIP | I | Active low “Burst Data in Process” is driven by a PowerPC processor. Asserted indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase. |

## LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| B29 | NC | - | | NC | - | |

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M15 and LatticeSC/M25 in a 900-pin package supports a 16-bit MPI interface.

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AJ1 | PB69A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B | PB85A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B |
| AK1 | PB69B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B | PB85B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B |
| AJ2 | PB69C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C | PB85C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C |
| AH3 | PB69D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C | PB85D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C |
| AH1 | PROBE_VCC | - | | PROBE_VCC | - | |
| AH2 | PROBE_GND | - | | PROBE_GND | - | |
| AD9 | PR57D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A | PR71D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A |
| AC10 | PR57C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A | PR71C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A |
| AG2 | PR57B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E | PR71B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E |
| AG1 | PR57A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E | PR71A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E |
| AD8 | PR56D | 3 | | PR70D | 3 | |
| AC9 | PR56C | 3 | | PR70C | 3 | |
| AF2 | PR56B | 3 | | PR70B | 3 | |
| AF1 | PR56A | 3 | | PR70A | 3 | |
| AE6 | PR55D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F | PR69D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F |
| AE7 | PR55C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F | PR69C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F |
| AE1 | PR55B | 3 | | PR69B | 3 | |
| AE2 | PR55A | 3 | | PR69A | 3 | |
| AB8 | PR53D | 3 | | PR67D | 3 | |
| AC8 | PR53C | 3 | | PR67C | 3 | |
| AE4 | PR53B | 3 | | PR67B | 3 | |
| AE3 | PR53A | 3 | | PR67A | 3 | |
| AA10 | PR52D | 3 | | PR66D | 3 | |
| AA9 | PR52C | 3 | | PR66C | 3 | |
| AD1 | PR52B | 3 | | PR66B | 3 | |
| AC1 | PR52A | 3 | | PR66A | 3 | |
| AC7 | PR51D | 3 | VREF2_3 | PR65D | 3 | VREF2_3 |
| AB7 | PR51C | 3 | | PR65C | 3 | |
| AD5 | PR51B | 3 | | PR65B | 3 | |
| AC5 | PR51A | 3 | | PR65A | 3 | |
| AE5 | PR49D | 3 | | PR62D | 3 | |
| AF5 | PR49C | 3 | | PR62C | 3 | |
| AD3 | PR49B | 3 | | PR62B | 3 | |
| AD4 | PR49A | 3 | | PR62A | 3 | |
| Y10 | PR48D | 3 | | PR61D | 3 | |
| Y9 | PR48C | 3 | | PR61C | 3 | |
| AC2 | PR48B | 3 | | PR61B | 3 | |
| AD2 | PR48A | 3 | | PR61A | 3 | |
| AC6 | PR47D | 3 | | PR60D | 3 | |
| AB6 | PR47C | 3 | | PR60C | 3 | |
| AA1 | PR47B | 3 | | PR60B | 3 | |
| AB1 | PR47A | 3 | | PR60A | 3 | |
| AA5 | PR44D | 3 | | PR53D | 3 | |
| AB5 | PR44C | 3 | | PR53C | 3 | |
| Y1 | PR44B | 3 | | PR53B | 3 | |
| W1 | PR44A | 3 | | PR53A | 3 | |
| W8 | PR43D | 3 | | PR52D | 3 | |
| Y7 | PR43C | 3 | | PR52C | 3 | |
| Y5 | PR43B | 3 | | PR52B | 3 | |
| W5 | PR43A | 3 | | PR52A | 3 | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| E22 | VCC12 | - | | VCC12 | - | |
| E21 | VCC12 | - | | VCC12 | - | |
| E3 | VCC12 | - | | VCC12 | - | |
| E4 | VCC12 | - | | VCC12 | - | |
| E6 | VCC12 | - | | VCC12 | - | |
| E7 | VCC12 | - | | VCC12 | - | |
| E8 | VCC12 | - | | VCC12 | - | |
| E9 | VCC12 | - | | VCC12 | - | |
| E11 | VCC12 | - | | VCC12 | - | |
| E12 | VCC12 | - | | VCC12 | - | |
| A23 | GND | - | | GND | - | |
| A31 | GND | - | | GND | - | |
| AA13 | GND | - | | GND | - | |
| AA15 | GND | - | | GND | - | |
| AA18 | GND | - | | GND | - | |
| AA20 | GND | - | | GND | - | |
| AA26 | GND | - | | GND | - | |
| AA6 | GND | - | | GND | - | |
| AB10 | GND | - | | GND | - | |
| AB24 | GND | - | | GND | - | |
| AC14 | GND | - | | GND | - | |
| AC22 | GND | - | | GND | - | |
| AC29 | GND | - | | GND | - | |
| AC3 | GND | - | | GND | - | |
| AD11 | GND | - | | GND | - | |
| AD19 | GND | - | | GND | - | |
| AD27 | GND | - | | GND | - | |
| AD7 | GND | - | | GND | - | |
| AF12 | GND | - | | GND | - | |
| AF18 | GND | - | | GND | - | |
| AF24 | GND | - | | GND | - | |
| AF30 | GND | - | | GND | - | |
| AF4 | GND | - | | GND | - | |
| AG15 | GND | - | | GND | - | |
| AG21 | GND | - | | GND | - | |
| AG9 | GND | - | | GND | - | |
| AJ10 | GND | - | | GND | - | |
| AJ16 | GND | - | | GND | - | |
| AJ20 | GND | - | | GND | - | |
| AJ26 | GND | - | | GND | - | |
| AJ29 | GND | - | | GND | - | |
| AJ4 | GND | - | | GND | - | |
| AK13 | GND | - | | GND | - | |
| AK17 | GND | - | | GND | - | |
| AK23 | GND | - | | GND | - | |
| AK7 | GND | - | | GND | - | |
| AL1 | GND | - | | GND | - | |
| AL32 | GND | - | | GND | - | |
| AM2 | GND | - | | GND | - | |
| AM31 | GND | - | | GND | - | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AA7 | VCCIO3 | - | | VCCIO3 | - | |
| AB9 | VCCIO3 | - | | VCCIO3 | - | |
| AC4 | VCCIO3 | - | | VCCIO3 | - | |
| AD6 | VCCIO3 | - | | VCCIO3 | - | |
| AF3 | VCCIO3 | - | | VCCIO3 | - | |
| T3 | VCCIO3 | - | | VCCIO3 | - | |
| U4 | VCCIO3 | - | | VCCIO3 | - | |
| V6 | VCCIO3 | - | | VCCIO3 | - | |
| W10 | VCCIO3 | - | | VCCIO3 | - | |
| Y3 | VCCIO3 | - | | VCCIO3 | - | |
| AC11 | VCCIO4 | - | | VCCIO4 | - | |
| AD14 | VCCIO4 | - | | VCCIO4 | - | |
| AF15 | VCCIO4 | - | | VCCIO4 | - | |
| AF9 | VCCIO4 | - | | VCCIO4 | - | |
| AG12 | VCCIO4 | - | | VCCIO4 | - | |
| AJ13 | VCCIO4 | - | | VCCIO4 | - | |
| AJ7 | VCCIO4 | - | | VCCIO4 | - | |
| AK10 | VCCIO4 | - | | VCCIO4 | - | |
| AK16 | VCCIO4 | - | | VCCIO4 | - | |
| AK4 | VCCIO4 | - | | VCCIO4 | - | |
| AC19 | VCCIO5 | - | | VCCIO5 | - | |
| AD22 | VCCIO5 | - | | VCCIO5 | - | |
| AF21 | VCCIO5 | - | | VCCIO5 | - | |
| AG18 | VCCIO5 | - | | VCCIO5 | - | |
| AG24 | VCCIO5 | - | | VCCIO5 | - | |
| AJ17 | VCCIO5 | - | | VCCIO5 | - | |
| AJ23 | VCCIO5 | - | | VCCIO5 | - | |
| AJ30 | VCCIO5 | - | | VCCIO5 | - | |
| AK20 | VCCIO5 | - | | VCCIO5 | - | |
| AK26 | VCCIO5 | - | | VCCIO5 | - | |
| AA27 | VCCIO6 | - | | VCCIO6 | - | |
| AB23 | VCCIO6 | - | | VCCIO6 | - | |
| AC30 | VCCIO6 | - | | VCCIO6 | - | |
| AD26 | VCCIO6 | - | | VCCIO6 | - | |
| AF29 | VCCIO6 | - | | VCCIO6 | - | |
| T29 | VCCIO6 | - | | VCCIO6 | - | |
| U30 | VCCIO6 | - | | VCCIO6 | - | |
| V26 | VCCIO6 | - | | VCCIO6 | - | |
| W24 | VCCIO6 | - | | VCCIO6 | - | |
| Y29 | VCCIO6 | - | | VCCIO6 | - | |
| G30 | VCCIO7 | - | | VCCIO7 | - | |
| J27 | VCCIO7 | - | | VCCIO7 | - | |
| K29 | VCCIO7 | - | | VCCIO7 | - | |
| L24 | VCCIO7 | - | | VCCIO7 | - | |
| M26 | VCCIO7 | - | | VCCIO7 | - | |
| N30 | VCCIO7 | - | | VCCIO7 | - | |
| P23 | VCCIO7 | - | | VCCIO7 | - | |
| R27 | VCCIO7 | - | | VCCIO7 | - | |
| AA11 | VCCAUX | - | | VCCAUX | - | |
| AA12 | VCCAUX | - | | VCCAUX | - | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AA21 | VCCAUX | - | | VCCAUX | - | |
| AA22 | VCCAUX | - | | VCCAUX | - | |
| AB11 | VCCAUX | - | | VCCAUX | - | |
| AB12 | VCCAUX | - | | VCCAUX | - | |
| AB15 | VCCAUX | - | | VCCAUX | - | |
| AB16 | VCCAUX | - | | VCCAUX | - | |
| AB17 | VCCAUX | - | | VCCAUX | - | |
| AB18 | VCCAUX | - | | VCCAUX | - | |
| AB21 | VCCAUX | - | | VCCAUX | - | |
| AB22 | VCCAUX | - | | VCCAUX | - | |
| L11 | VCCAUX | - | | VCCAUX | - | |
| L12 | VCCAUX | - | | VCCAUX | - | |
| L14 | VCCAUX | - | | VCCAUX | - | |
| L15 | VCCAUX | - | | VCCAUX | - | |
| L18 | VCCAUX | - | | VCCAUX | - | |
| L19 | VCCAUX | - | | VCCAUX | - | |
| L21 | VCCAUX | - | | VCCAUX | - | |
| L22 | VCCAUX | - | | VCCAUX | - | |
| M11 | VCCAUX | - | | VCCAUX | - | |
| M12 | VCCAUX | - | | VCCAUX | - | |
| M21 | VCCAUX | - | | VCCAUX | - | |
| M22 | VCCAUX | - | | VCCAUX | - | |
| P11 | VCCAUX | - | | VCCAUX | - | |
| P22 | VCCAUX | - | | VCCAUX | - | |
| R11 | VCCAUX | - | | VCCAUX | - | |
| R22 | VCCAUX | - | | VCCAUX | - | |
| V11 | VCCAUX | - | | VCCAUX | - | |
| V22 | VCCAUX | - | | VCCAUX | - | |
| W11 | VCCAUX | - | | VCCAUX | - | |
| W22 | VCCAUX | - | | VCCAUX | - | |
| N11 | VTT_2 | 2 | | VTT_2 | 2 | |
| R10 | VTT_2 | 2 | | VTT_2 | 2 | |
| T11 | VTT_3 | 3 | | VTT_3 | 3 | |
| U11 | VTT_3 | 3 | | VTT_3 | 3 | |
| Y11 | VTT_3 | 3 | | VTT_3 | 3 | |
| AB13 | VTT_4 | 4 | | VTT_4 | 4 | |
| AB14 | VTT_4 | 4 | | VTT_4 | 4 | |
| AC15 | VTT_4 | 4 | | VTT_4 | 4 | |
| AB19 | VTT_5 | 5 | | VTT_5 | 5 | |
| AB20 | VTT_5 | 5 | | VTT_5 | 5 | |
| AC18 | VTT_5 | 5 | | VTT_5 | 5 | |
| T22 | VTT_6 | 6 | | VTT_6 | 6 | |
| U22 | VTT_6 | 6 | | VTT_6 | 6 | |
| Y22 | VTT_6 | 6 | | VTT_6 | 6 | |
| N22 | VTT_7 | 7 | | VTT_7 | 7 | |
| R23 | VTT_7 | 7 | | VTT_7 | 7 | |
| M17 | VCC12 | - | | VCC12 | - | |
| M16 | VCC12 | - | | VCC12 | - | |
| T12 | VCC12 | - | | VCC12 | - | |
| T21 | VCC12 | - | | VCC12 | - | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AD29 | PL60D | 6 | | PL84D | 6 | |
| AE31 | PL61A | 6 | | PL85A | 6 | |
| AF31 | PL61B | 6 | | PL85B | 6 | |
| AF30 | PL61C | 6 | | PL85C | 6 | |
| AF29 | PL61D | 6 | | PL85D | 6 | |
| AH33 | PL62A | 6 | | PL86A | 6 | |
| AJ33 | PL62B | 6 | | PL86B | 6 | |
| AC28 | PL62C | 6 | | PL86C | 6 | |
| AD28 | PL62D | 6 | | PL86D | 6 | |
| AH32 | PL65A | 6 | | PL89A | 6 | |
| AJ32 | PL65B | 6 | | PL89B | 6 | |
| AD27 | PL65C | 6 | | PL89C | 6 | |
| AE27 | PL65D | 6 | VREF2_6 | PL89D | 6 | VREF2_6 |
| AG34 | PL66A | 6 | | PL90A | 6 | |
| AH34 | PL66B | 6 | | PL90B | 6 | |
| AC26 | PL66C | 6 | | PL90C | 6 | |
| AB26 | PL66D | 6 | | PL90D | 6 | |
| AK33 | PL67A | 6 | | PL91A | 6 | |
| AL33 | PL67B | 6 | | PL91B | 6 | |
| AG30 | PL67C | 6 | | PL91C | 6 | |
| AH30 | PL67D | 6 | | PL91D | 6 | |
| AL34 | PL69A | 6 | | PL93A | 6 | |
| AM34 | PL69B | 6 | | PL93B | 6 | |
| AJ30 | PL69C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F | PL93C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F |
| AK30 | PL69D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F | PL93D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F |
| AJ31 | PL70A | 6 | | PL94A | 6 | |
| AH31 | PL70B | 6 | | PL94B | 6 | |
| AD26 | PL70C | 6 | | PL94C | 6 | |
| AD25 | PL70D | 6 | | PL94D | 6 | |
| AL32 | PL71A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E | PL95A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E |
| AL31 | PL71B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E | PL95B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E |
| AG29 | PL71C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A | PL95C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A |
| AG28 | PL71D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A | PL95D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A |
| AF28 | XRES | - | | XRES | - | |
| AF27 | TEMP | 6 | | TEMP | 6 | |
| AM33 | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B |
| AN33 | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B |
| AH29 | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| AJ29 | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| AM32 | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C |
| AM31 | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C |
| AG27 | PB4C | 5 | | PB4C | 5 | |
| AG26 | PB4D | 5 | | PB4D | 5 | |
| AL29 | PB5A | 5 | | PB5A | 5 | |
| AL28 | PB5B | 5 | | PB5B | 5 | |

## LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AJ9 | PB78C | 4 | | PB117C | 4 | |
| AJ8 | PB78D | 4 | | PB117D | 4 | |
| AP3 | PB79A | 4 | | PB119A | 4 | |
| AN3 | PB79B | 4 | | PB119B | 4 | |
| AF10 | PB79C | 4 | | PB119C | 4 | |
| AE10 | PB79D | 4 | | PB119D | 4 | |
| AL7 | PB81A | 4 | | PB121A | 4 | |
| AL6 | PB81B | 4 | | PB121B | 4 | |
| AK7 | PB81C | 4 | | PB121C | 4 | |
| AK6 | PB81D | 4 | | PB121D | 4 | |
| AN5 | PB82A | 4 | | PB123A | 4 | |
| AN4 | PB82B | 4 | | PB123B | 4 | |
| AH9 | PB82C | 4 | VREF1_4 | PB123C | 4 | VREF1_4 |
| AH8 | PB82D | 4 | | PB123D | 4 | |
| AM3 | PB83A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D | PB124A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D |
| AM4 | PB83B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D | PB124B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D |
| AG9 | PB83C | 4 | | PB124C | 4 | |
| AG8 | PB83D | 4 | | PB124D | 4 | |
| AN2 | PB85A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B | PB125A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B |
| AM2 | PB85B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B | PB125B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B |
| AJ6 | PB85C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C | PB125C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C |
| AH6 | PB85D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C | PB125D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C |
| AF7 | PROBE_VCC | - | | PROBE_VCC | - | |
| AF8 | PROBE_GND | - | | PROBE_GND | - | |
| AG7 | PR71D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A | PR95D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A |
| AG6 | PR71C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A | PR95C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A |
| AL4 | PR71B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E | PR95B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E |
| AL3 | PR71A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E | PR95A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E |
| AD10 | PR70D | 3 | | PR94D | 3 | |
| AD9 | PR70C | 3 | | PR94C | 3 | |
| AH4 | PR70B | 3 | | PR94B | 3 | |
| AJ4 | PR70A | 3 | | PR94A | 3 | |
| AK5 | PR69D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F | PR93D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F |
| AJ5 | PR69C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F | PR93C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F |
| AM1 | PR69B | 3 | | PR93B | 3 | |
| AL1 | PR69A | 3 | | PR93A | 3 | |
| AH5 | PR67D | 3 | | PR91D | 3 | |
| AG5 | PR67C | 3 | | PR91C | 3 | |
| AL2 | PR67B | 3 | | PR91B | 3 | |
| AK2 | PR67A | 3 | | PR91A | 3 | |
| AB9 | PR66D | 3 | | PR90D | 3 | |
| AC9 | PR66C | 3 | | PR90C | 3 | |
| AH1 | PR66B | 3 | | PR90B | 3 | |
| AG1 | PR66A | 3 | | PR90A | 3 | |
| AE8 | PR65D | 3 | VREF2_3 | PR89D | 3 | VREF2_3 |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| F6 | A_VDDOB0_R | - | |
| B4 | A_HDOUTN0_R | - | PCS 3E0 CH 0 OUT N |
| F7 | A_VDDOB1_R | - | |
| B5 | A_HDOUTN1_R | - | PCS 3E0 CH 1 OUT N |
| E6 | VCC12 | - | |
| A5 | A_HDOUTP1_R | - | PCS 3E0 CH 1 OUT P |
| B6 | A_HDINN1_R | - | PCS 3E0 CH 1 IN N |
| A6 | A_HDINP1_R | - | PCS 3E0 CH 1 IN P |
| C6 | VCC12 | - | |
| D4 | A_VDDIB1_R | - | |
| C7 | VCC12 | - | |
| D5 | A_VDDIB2_R | - | |
| A7 | A_HDINP2_R | - | PCS 3E0 CH 2 IN P |
| B7 | A_HDINN2_R | - | PCS 3E0 CH 2 IN N |
| E7 | VCC12 | - | |
| A8 | A_HDOUTP2_R | - | PCS 3E0 CH 2 OUT P |
| F8 | A_VDDOB2_R | - | |
| B8 | A_HDOUTN2_R | - | PCS 3E0 CH 2 OUT N |
| F9 | A_VDDOB3_R | - | |
| B9 | A_HDOUTN3_R | - | PCS 3E0 CH 3 OUT N |
| E8 | VCC12 | - | |
| A9 | A_HDOUTP3_R | - | PCS 3E0 CH 3 OUT P |
| B10 | A_HDINN3_R | - | PCS 3E0 CH 3 IN N |
| A10 | A_HDINP3_R | - | PCS 3E0 CH 3 IN P |
| C10 | VCC12 | - | |
| D6 | A_VDDIB3_R | - | |
| G10 | VCC12 | - | |
| D7 | B_VDDIB0_R | - | |
| E10 | B_HDINP0_R | - | PCS 3E1 CH 0 IN P |
| F10 | B_HDINN0_R | - | PCS 3E1 CH 0 IN N |
| K10 | VCC12 | - | |
| A11 | B_HDOUTP0_R | - | PCS 3E1 CH 0 OUT P |
| D10 | B_VDDOB0_R | - | |
| B11 | B_HDOUTN0_R | - | PCS 3E1 CH 0 OUT N |
| D11 | B_VDDOB1_R | - | |
| B12 | B_HDOUTN1_R | - | PCS 3E1 CH 1 OUT N |
| L10 | VCC12 | - | |
| A12 | B_HDOUTP1_R | - | PCS 3E1 CH 1 OUT P |
| F11 | B_HDINN1_R | - | PCS 3E1 CH 1 IN N |
| E11 | B_HDINP1_R | - | PCS 3E1 CH 1 IN P |
| G11 | VCC12 | - | |
| D8 | B_VDDIB1_R | - | |
| G12 | VCC12 | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| P38 | PL26B | 7 | | PL40B | 7 | |
| N35 | PL26C | 7 | | PL40C | 7 | |
| N36 | PL26D | 7 | | PL40D | 7 | |
| N39 | PL29A | 7 | | PL43A | 7 | |
| P39 | PL29B | 7 | | PL43B | 7 | |
| R34 | PL29C | 7 | VREF1_7 | PL43C | 7 | VREF1_7 |
| T34 | PL29D | 7 | DIFFR_7 | PL43D | 7 | DIFFR_7 |
| L41 | PL30A | 7 | | PL44A | 7 | |
| M41 | PL30B | 7 | | PL44B | 7 | |
| W29 | PL30C | 7 | | PL44C | 7 | |
| Y29 | PL30D | 7 | | PL44D | 7 | |
| L42 | PL31A | 7 | | PL45A | 7 | |
| M42 | PL31B | 7 | | PL45B | 7 | |
| U32 | PL31C | 7 | | PL45C | 7 | |
| V32 | PL31D | 7 | | PL45D | 7 | |
| R37 | PL33A | 7 | | PL47A | 7 | |
| T37 | PL33B | 7 | | PL47B | 7 | |
| M36 | PL33C | 7 | | PL47C | 7 | |
| M37 | PL33D | 7 | | PL47D | 7 | |
| P40 | PL34A | 7 | | PL48A | 7 | |
| N40 | PL34B | 7 | | PL48B | 7 | |
| R35 | PL34C | 7 | | PL48C | 7 | |
| T35 | PL34D | 7 | | PL48D | 7 | |
| N41 | PL35A | 7 | | PL49A | 7 | |
| P41 | PL35B | 7 | | PL49B | 7 | |
| V33 | PL35C | 7 | | PL49C | 7 | |
| U33 | PL35D | 7 | | PL49D | 7 | |
| R38 | PL37A | 7 | | PL51A | 7 | |
| T38 | PL37B | 7 | | PL51B | 7 | |
| R36 | PL37C | 7 | | PL51C | 7 | |
| T36 | PL37D | 7 | | PL51D | 7 | |
| N42 | PL38A | 7 | | PL52A | 7 | |
| P42 | PL38B | 7 | | PL52B | 7 | |
| Y31 | PL38C | 7 | | PL52C | 7 | |
| AA31 | PL38D | 7 | | PL52D | 7 | |
| U37 | PL39A | 7 | | PL53A | 7 | |
| V37 | PL39B | 7 | | PL53B | 7 | |
| U34 | PL39C | 7 | | PL53C | 7 | |
| V34 | PL39D | 7 | | PL53D | 7 | |
| U39 | PL41A | 7 | | PL55A | 7 | |
| T39 | PL41B | 7 | | PL55B | 7 | |
| V35 | PL41C | 7 | | PL55C | 7 | |
| W35 | PL41D | 7 | | PL55D | 7 | |
| R41 | PL42A | 7 | | PL56A | 7 | |
| T41 | PL42B | 7 | | PL56B | 7 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| W33 | PL42C | 7 | | PL56C | 7 | |
| Y33 | PL42D | 7 | | PL56D | 7 | |
| W37 | PL43A | 7 | | PL57A | 7 | |
| Y37 | PL43B | 7 | | PL57B | 7 | |
| Y32 | PL43C | 7 | | PL57C | 7 | |
| AA32 | PL43D | 7 | | PL57D | 7 | |
| U38 | PL46A | 7 | | PL60A | 7 | |
| V38 | PL46B | 7 | | PL60B | 7 | |
| W34 | PL46C | 7 | | PL60C | 7 | |
| Y34 | PL46D | 7 | | PL60D | 7 | |
| T40 | PL47A | 7 | PCLKT7_1 | PL61A | 7 | PCLKT7_1 |
| U40 | PL47B | 7 | PCLKC7_1 | PL61B | 7 | PCLKC7_1 |
| AA33 | PL47C | 7 | PCLKT7_3 | PL61C | 7 | PCLKT7_3 |
| AB33 | PL47D | 7 | PCLKC7_3 | PL61D | 7 | PCLKC7_3 |
| R42 | PL48A | 7 | PCLKT7_0 | PL62A | 7 | PCLKT7_0 |
| T42 | PL48B | 7 | PCLKC7_0 | PL62B | 7 | PCLKC7_0 |
| AA34 | PL48C | 7 | PCLKT7_2 | PL62C | 7 | PCLKT7_2 |
| AB34 | PL48D | 7 | PCLKC7_2 | PL62D | 7 | PCLKC7_2 |
| U41 | PL50A | 6 | PCLKT6_0 | PL64A | 6 | PCLKT6_0 |
| V41 | PL50B | 6 | PCLKC6_0 | PL64B | 6 | PCLKC6_0 |
| V36 | PL50C | 6 | PCLKT6_1 | PL64C | 6 | PCLKT6_1 |
| W36 | PL50D | 6 | PCLKC6_1 | PL64D | 6 | PCLKC6_1 |
| U42 | PL51A | 6 | | PL65A | 6 | |
| V42 | PL51B | 6 | | PL65B | 6 | |
| AB31 | PL51C | 6 | PCLKT6_3 | PL65C | 6 | PCLKT6_3 |
| AC31 | PL51D | 6 | PCLKC6_3 | PL65D | 6 | PCLKC6_3 |
| W38 | PL52A | 6 | | PL66A | 6 | |
| Y38 | PL52B | 6 | | PL66B | 6 | |
| AA35 | PL52C | 6 | PCLKT6_2 | PL66C | 6 | PCLKT6_2 |
| AB35 | PL52D | 6 | PCLKC6_2 | PL66D | 6 | PCLKC6_2 |
| W39 | PL55A | 6 | | PL69A | 6 | |
| Y39 | PL55B | 6 | | PL69B | 6 | |
| AB32 | PL55C | 6 | VREF1_6 | PL69C | 6 | VREF1_6 |
| AC32 | PL55D | 6 | | PL69D | 6 | |
| W40 | PL56A | 6 | | PL70A | 6 | |
| Y40 | PL56B | 6 | | PL70B | 6 | |
| AA36 | PL56C | 6 | | PL70C | 6 | |
| AB36 | PL56D | 6 | | PL70D | 6 | |
| W41 | PL57A | 6 | | PL71A | 6 | |
| Y41 | PL57B | 6 | | PL71B | 6 | |
| AA37 | PL57C | 6 | | PL71C | 6 | |
| AB37 | PL57D | 6 | | PL71D | 6 | |
| W42 | PL59A | 6 | | PL73A | 6 | |
| Y42 | PL59B | 6 | | PL73B | 6 | |
| AC33 | PL59C | 6 | | PL73C | 6 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AD33 | PL59D | 6 | | PL73D | 6 | |
| AA38 | PL60A | 6 | | PL74A | 6 | |
| AB38 | PL60B | 6 | | PL74B | 6 | |
| AC29 | PL60C | 6 | | PL74C | 6 | |
| AD29 | PL60D | 6 | | PL74D | 6 | |
| AA41 | PL61A | 6 | | PL75A | 6 | |
| AB41 | PL61B | 6 | | PL75B | 6 | |
| AC34 | PL61C | 6 | | PL75C | 6 | |
| AD34 | PL61D | 6 | | PL75D | 6 | |
| AA42 | PL63A | 6 | | PL77A | 6 | |
| AB42 | PL63B | 6 | | PL77B | 6 | |
| AC37 | PL63C | 6 | | PL77C | 6 | |
| AD37 | PL63D | 6 | | PL77D | 6 | |
| AC38 | PL64A | 6 | | PL78A | 6 | |
| AD38 | PL64B | 6 | | PL78B | 6 | |
| AD36 | PL64C | 6 | | PL78C | 6 | |
| AE36 | PL64D | 6 | | PL78D | 6 | |
| AC39 | PL65A | 6 | | PL79A | 6 | |
| AD39 | PL65B | 6 | | PL79B | 6 | |
| AD35 | PL65C | 6 | | PL79C | 6 | |
| AE35 | PL65D | 6 | | PL79D | 6 | |
| AC40 | PL67A | 6 | | PL81A | 6 | |
| AD40 | PL67B | 6 | | PL81B | 6 | |
| AE37 | PL67C | 6 | | PL81C | 6 | |
| AF37 | PL67D | 6 | | PL81D | 6 | |
| AC41 | PL68A | 6 | | PL82A | 6 | |
| AD41 | PL68B | 6 | | PL82B | 6 | |
| AE34 | PL68C | 6 | | PL82C | 6 | |
| AF34 | PL68D | 6 | | PL82D | 6 | |
| AC42 | PL69A | 6 | | PL83A | 6 | |
| AD42 | PL69B | 6 | | PL83B | 6 | |
| AE33 | PL69C | 6 | | PL83C | 6 | |
| AF33 | PL69D | 6 | | PL83D | 6 | |
| AE38 | PL72A | 6 | | PL86A | 6 | |
| AF38 | PL72B | 6 | | PL86B | 6 | |
| AE32 | PL72C | 6 | | PL86C | 6 | |
| AF32 | PL72D | 6 | | PL86D | 6 | |
| AE41 | PL73A | 6 | | PL87A | 6 | |
| AF41 | PL73B | 6 | | PL87B | 6 | |
| AE31 | PL73C | 6 | | PL87C | 6 | |
| AF31 | PL73D | 6 | | PL87D | 6 | |
| AE42 | PL74A | 6 | | PL88A | 6 | |
| AF42 | PL74B | 6 | | PL88B | 6 | |
| AG37 | PL74C | 6 | | PL88C | 6 | |
| AH37 | PL74D | 6 | | PL88D | 6 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AP1 | PR90B | 3 | | PR109B | 3 | |
| AN1 | PR90A | 3 | | PR109A | 3 | |
| AK10 | PR89D | 3 | VREF2_3 | PR107D | 3 | VREF2_3 |
| AJ10 | PR89C | 3 | | PR107C | 3 | |
| AM5 | PR89B | 3 | | PR107B | 3 | |
| AL5 | PR89A | 3 | | PR107A | 3 | |
| AL7 | PR86D | 3 | | PR104D | 3 | |
| AK7 | PR86C | 3 | | PR104C | 3 | |
| AM1 | PR86B | 3 | | PR104B | 3 | |
| AL1 | PR86A | 3 | | PR104A | 3 | |
| AJ11 | PR85D | 3 | | PR103D | 3 | |
| AH11 | PR85C | 3 | | PR103C | 3 | |
| AK5 | PR85B | 3 | | PR103B | 3 | |
| AJ5 | PR85A | 3 | | PR103A | 3 | |
| AK9 | PR84D | 3 | | PR99D | 3 | |
| AJ9 | PR84C | 3 | | PR99C | 3 | |
| AK3 | PR84B | 3 | | PR99B | 3 | |
| AJ3 | PR84A | 3 | | PR99A | 3 | |
| AK6 | PR82D | 3 | | PR98D | 3 | |
| AJ6 | PR82C | 3 | | PR98C | 3 | |
| AK2 | PR82B | 3 | | PR98B | 3 | |
| AJ2 | PR82A | 3 | | PR98A | 3 | |
| AH10 | PR81D | 3 | | PR96D | 3 | |
| AG10 | PR81C | 3 | | PR96C | 3 | |
| AK1 | PR81B | 3 | | PR96B | 3 | |
| AJ1 | PR81A | 3 | | PR96A | 3 | |
| AH9 | PR80D | 3 | | PR94D | 3 | |
| AG9 | PR80C | 3 | | PR94C | 3 | |
| AH2 | PR80B | 3 | | PR94B | 3 | |
| AG2 | PR80A | 3 | | PR94A | 3 | |
| AH8 | PR78D | 3 | | PR92D | 3 | |
| AG8 | PR78C | 3 | | PR92C | 3 | |
| AG1 | PR78B | 3 | | PR92B | 3 | |
| AH1 | PR78A | 3 | | PR92A | 3 | |
| AG14 | PR77D | 3 | | PR91D | 3 | |
| AF14 | PR77C | 3 | | PR91C | 3 | |
| AG4 | PR77B | 3 | | PR91B | 3 | |
| AF4 | PR77A | 3 | | PR91A | 3 | |
| AH7 | PR76D | 3 | DIFFR_3 | PR90D | 3 | DIFFR_3 |
| AG7 | PR76C | 3 | | PR90C | 3 | |
| AG3 | PR76B | 3 | | PR90B | 3 | |
| AF3 | PR76A | 3 | | PR90A | 3 | |
| AH6 | PR74D | 3 | | PR88D | 3 | |
| AG6 | PR74C | 3 | | PR88C | 3 | |
| AF1 | PR74B | 3 | | PR88B | 3 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AG38 | NC | - | | PL95A | 6 | |
| AH38 | NC | - | | PL95B | 6 | |
| AJ39 | NC | - | | PL100A | 6 | |
| AK39 | NC | - | | PL100B | 6 | |
| AL41 | NC | - | | PL105A | 6 | |
| AM41 | NC | - | | PL105B | 6 | |
| AN40 | NC | - | | PL108A | 6 | |
| AM40 | NC | - | | PL108B | 6 | |
| AM39 | NC | - | | PL111A | 6 | |
| AN39 | NC | - | | PL111B | 6 | |
| AR42 | NC | - | | PL113A | 6 | |
| AT42 | NC | - | | PL113B | 6 | |
| AT1 | NC | - | | PR113B | 3 | |
| AR1 | NC | - | | PR113A | 3 | |
| AN4 | NC | - | | PR111B | 3 | |
| AM4 | NC | - | | PR111A | 3 | |
| AM3 | NC | - | | PR108B | 3 | |
| AN3 | NC | - | | PR108A | 3 | |
| AM2 | NC | - | | PR105B | 3 | |
| AL2 | NC | - | | PR105A | 3 | |
| AK4 | NC | - | | PR100B | 3 | |
| AJ4 | NC | - | | PR100A | 3 | |
| AH5 | NC | - | | PR95B | 3 | |
| AG5 | NC | - | | PR95A | 3 | |
| P6 | NC | - | | PR39B | 2 | |
| N6 | NC | - | | PR39A | 2 | |
| L3 | NC | - | | PR36B | 2 | |
| K3 | NC | - | | PR36A | 2 | |
| M5 | NC | - | | PR35A | 2 | |
| L4 | NC | - | | PR32B | 2 | |
| K4 | NC | - | | PR32A | 2 | |
| A2 | GND | - | | GND | - | |
| A41 | GND | - | | GND | - | |
| AA20 | GND | - | | GND | - | |
| AA23 | GND | - | | GND | - | |
| AA3 | GND | - | | GND | - | |
| AA39 | GND | - | | GND | - | |
| AB20 | GND | - | | GND | - | |
| AB23 | GND | - | | GND | - | |
| AB4 | GND | - | | GND | - | |
| AB40 | GND | - | | GND | - | |
| AC17 | GND | - | | GND | - | |
| AC19 | GND | - | | GND | - | |
| AC21 | GND | - | | GND | - | |
| AC22 | GND | - | | GND | - | |

**Industrial, Cont.**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA40EP1-6FF1020I[1] | -6 | Organic fcBGA | 1020 | IND | 40.4 |
| LFSCM3GA40EP1-5FF1020I[1] | -5 | Organic fcBGA | 1020 | IND | 40.4 |
| LFSCM3GA40EP1-6FFA1020I | -6 | Organic fcBGA Revision 2 | 1020 | IND | 40.4 |
| LFSCM3GA40EP1-5FFA1020I | -5 | Organic fcBGA Revision 2 | 1020 | IND | 40.4 |
| LFSCM3GA40EP1-6FC1152I[2] | -6 | Ceramic fcBGA | 1152 | IND | 40.4 |
| LFSCM3GA40EP1-5FC1152I[2] | -5 | Ceramic fcBGA | 1152 | IND | 40.4 |
| LFSCM3GA40EP1-6FF1152I | -6 | Organic fcBGA | 1152 | IND | 40.4 |
| LFSCM3GA40EP1-5FF1152I | -5 | Organic fcBGA | 1152 | IND | 40.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA80E-6FC1152I[1] | -6 | Ceramic fcBGA | 1152 | IND | 80.1 |
| LFSC3GA80E-5FC1152I[1] | -5 | Ceramic fcBGA | 1152 | IND | 80.1 |
| LFSC3GA80E-6FF1152I | -6 | Organic fcBGA | 1152 | IND | 80.1 |
| LFSC3GA80E-5FF1152I | -5 | Organic fcBGA | 1152 | IND | 80.1 |
| LFSC3GA80E-6FC1704I[1] | -6 | Ceramic fcBGA | 1704 | IND | 80.1 |
| LFSC3GA80E-5FC1704I[1] | -5 | Ceramic fcBGA | 1704 | IND | 80.1 |
| LFSC3GA80E-6FF1704I | -6 | Organic fcBGA | 1704 | IND | 80.1 |
| LFSC3GA80E-5FF1704I | -5 | Organic fcBGA | 1704 | IND | 80.1 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA80EP1-6FC1152I[1] | -6 | Ceramic fcBGA | 1152 | IND | 80.1 |
| LFSCM3GA80EP1-5FC1152I[1] | -5 | Ceramic fcBGA | 1152 | IND | 80.1 |
| LFSCM3GA80EP1-6FF1152I | -6 | Organic fcBGA | 1152 | IND | 80.1 |
| LFSCM3GA80EP1-5FF1152I | -5 | Organic fcBGA | 1152 | IND | 80.1 |
| LFSCM3GA80EP1-6FC1704I[1] | -6 | Ceramic fcBGA | 1704 | IND | 80.1 |
| LFSCM3GA80EP1-5FC1704I[1] | -5 | Ceramic fcBGA | 1704 | IND | 80.1 |
| LFSCM3GA80EP1-6FF1704I | -6 | Organic fcBGA | 1704 | IND | 80.1 |
| LFSCM3GA80EP1-5FF1704I | -5 | Organic fcBGA | 1704 | IND | 80.1 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

**Commercial, Cont.**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA40E-7FFN1020C[1] | -7 | Lead-Free Organic fcBGA | 1020 | COM | 40.4 |
| LFSC3GA40E-6FFN1020C[1] | -6 | Lead-Free Organic fcBGA | 1020 | COM | 40.4 |
| LFSC3GA40E-5FFN1020C[1] | -5 | Lead-Free Organic fcBGA | 1020 | COM | 40.4 |
| LFSC3GA40E-7FFAN1020C | -7 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSC3GA40E-6FFAN1020C | -6 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSC3GA40E-5FFAN1020C | -5 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSC3GA40E-7FCN1152C[2] | -7 | Lead-Free Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSC3GA40E-6FCN1152C[2] | -6 | Lead-Free Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSC3GA40E-5FCN1152C[2] | -5 | Lead-Free Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSC3GA40E-7FFN1152C | -7 | Lead-Free Organic fcBGA | 1152 | COM | 40.4 |
| LFSC3GA40E-6FFN1152C | -6 | Lead-Free Organic fcBGA | 1152 | COM | 40.4 |
| LFSC3GA40E-5FFN1152C | -5 | Lead-Free Organic fcBGA | 1152 | COM | 40.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA40EP1-7FFN1020C[1] | -7 | Organic fcBGA | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-6FFN1020C[1] | -6 | Organic fcBGA | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-5FFN1020C[1] | -5 | Organic fcBGA | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-7FFAN1020C | -7 | Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-6FFAN1020C | -6 | Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-5FFAN1020C | -5 | Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-7FCN1152C[2] | -7 | Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSCM3GA40EP1-6FCN1152C[2] | -6 | Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSCM3GA40EP1-5FCN1152C[2] | -5 | Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSCM3GA40EP1-7FFN1152C | -7 | Organic fcBGA | 1152 | COM | 40.4 |
| LFSCM3GA40EP1-6FFN1152C | -6 | Organic fcBGA | 1152 | COM | 40.4 |
| LFSCM3GA40EP1-5FFN1152C | -5 | Organic fcBGA | 1152 | COM | 40.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.