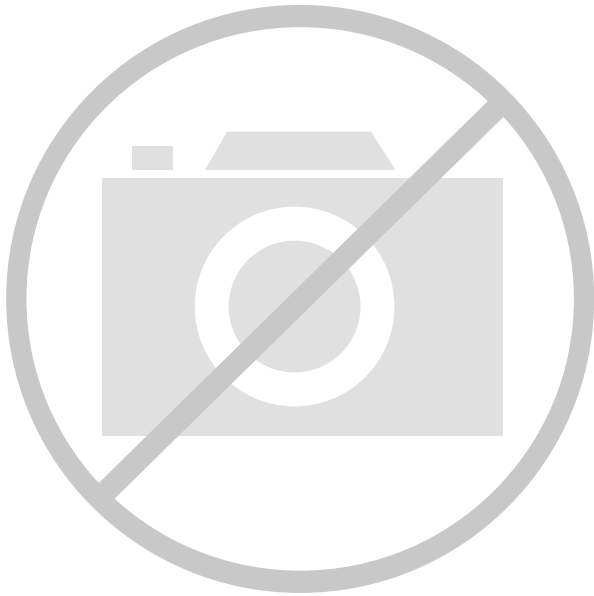




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga40e-5ff1152c

Table 2-9. Supported Input Standards

Input Standard	V _{REF} (Nom.)	V _{CCIO} ¹ (Nom.)	On-chip Termination
Single Ended Interfaces			
LVTTL33 ³	—	3.3	None
LVC MOS 33, 25, 18, 15, 12 ³	—	3.3/2.5/1.8/1.5/1.2	None
PCI33, PCIX33, AGP1X33 ³	—	3.3	None
PCIX15	0.75	1.5 ²	None / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
AGP2X33	1.32	—	None
HSTL18_I, II	0.9	1.8 ²	None / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
HSTL18_III, IV	1.08	1.8 ²	None / V _{CCIO} : 50
HSTL15_I, II	0.75	1.5 ²	None / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
HSTL15_III, IV	0.9	1.5 ²	None / V _{CCIO} : 50
SSTL33_I, II	1.5	3.3	None
SSTL25_I, II	1.25	2.5 ²	None / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
SSTL18_I, II	0.9	1.8 ²	None / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
GTL+, GTL	1.0 / 0.8	1.5 / 1.2 ²	None / V _{CCIO} : 50
Differential Interfaces			
SSTL18D_I, II	—	1.8 ²	None / Diff: 120, 150, 220, 420/ Diff to V _{CMT} : 120, 150, 220, 420 / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
SSTL25D_I, II	—	2.5 ²	None / Diff: 120, 150, 220, 420/ Diff to V _{CMT} : 120, 150, 220, 420 / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
SSTL33D_I, II	—	3.3	None
HSTL15D_I, II	—	1.5 ²	None / Diff: 120, 150, 220, 420/ Diff to V _{CMT} : 120, 150, 220, 420 / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
HSTL18D_I, II	—	1.8 ²	None / Diff: 120, 150, 220, 420/ Diff to V _{CMT} : 120, 150, 220, 420 / V _{CCIO} / 2: 50, 60/ V _{TT} : 60, 75, 120, 210
LVDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V _{CMT} : 120, 150, 220, 240
Mini-LVDS	—	—	None / Diff: 120, 150 / Diff to V _{CMT} : 120, 150
BLVDS25	—	—	None
MLVDS25	—	—	None
RSDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V _{CMT} : 120, 150, 220, 240
LVPECL33	—	≤2.5	None / Diff: 120, 150, 220, 240/ Diff to V _{CMT} : 120, 150, 220, 240

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.

2. V_{CCIO} needed for on-chip termination to V_{CCIO}/2 or V_{CCIO} only. V_{CCIO} is not specified for off-chip termination or V_{TT} termination.

3. All ratioed input buffers and dedicated pin input buffers include hysteresis with a typical value of 50mV.

Density Shifting

The LatticeSC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

PURESPEED I/O Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V _{IL}		V _{IH}		V _{OL} Max. (V)	V _{OH} Min. (V)	I _{OL} (mA)	I _{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 33	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 25	-0.3	0.7	1.7	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 18	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 15	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVC MOS 12	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.3	VCCIO - 0.3	12, 8, 4, 2	-12, -8, -4, -2
					0.2	VCCIO - 0.2	0.1	-0.1
PCIX15	-0.3	0.3VCCIO	0.5VCCIO	1.5	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCI33	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCIX33	-0.3	0.35VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
AGP-1X, AGP-2X	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
SSTL3_I	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.7	VCCIO - 1.1	8	-8
SSTS3_I OST ²	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 1.3	8	-8
SSTL3_II	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.5	VCCIO - 0.9	16	-16
SSTL3_II OST ²	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 0.13	16	-16
SSTL2_I	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.54	VCCIO - 0.62	7.6	-7.6
SSTL2_I OST ²	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	7.6	-7.6
SSTL2_II	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.35	VCCIO - 0.43	15.2	-15.2
SSTL2_II OST ²	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	15.2	-15.2
SSTL18_I	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
SSTL18_II	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
HSTL15_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	8	-8
HSTL15_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	16	-16
HSTL15_III ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL15_IV ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	9.6	-9.6
HSTL18_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	19.2	-19.2
HSTL18_III ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_IV ¹	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
GTL12 ¹ , GTLPLUS15 ¹	-0.3	VREF - 0.2	VREF + 0.2	N/A	N/A	N/A	N/A	N/A

1. Input only.

2. Input with on-chip series termination.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
MPI_STRBN	I	Driven active low indicates the start of a transaction on the PowerPC bus. MPI will strobe the address bus at next rising edge of clock.
MPI_ADDR[31:14]	I	Address bus driven by a PowerPC bus master. Only 18-bit width is needed. It has to be the least significant bit of the PowerPC 32-bit address A[31:14].
MPI_DAT[n:0]	I/O	Selectable data bus width from 8, and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
MPI_PAR[m:0]	I/O	Selectable parity bus width from 1, 2, and 3-bit. MPI_DP[0] for MPI_D[7:0], MPI_DP[1] for MPI_D[15:8] and MPI_DP[2] for MPI_D[23:16].
MPI_TA	O	Transfer acknowledge. Driven active low indicates that MPI received the data on the write cycle or returned data on the read cycle.
MPI_TEA	O	Transfer Error Acknowledge. Driven active low indicates that MPI detects a bus error on the internal system bus for current transaction.
MPI_RETRY	O	Active low MPI Retry requests the MPC860 to relinquish the bus and retry the cycle.
Multi-chip Alignment (User I/O if not used.)		
MCA_DONE_OUT	O	Multi-chip alignment done output (to second MCA chip)
MCA_DONE_IN	I	Multi-chip alignment done input (from second MCA chip)
MCA_CLK_P[1:2]_OUT	O	Multi-chip alignment clock [1:2] output (sourced by MCA master chip)
MCA_CLK_P[1:2]_IN	I	Multi-chip alignment clock [1:2] input (from MCA master chip)
TEMP	—	Temperature sensing diode pin. Dedicated pin. Accuracy is typically +/- 10°C.
Miscellaneous Dedicated Pins		
XRES	—	External reference resistor between this pin and ground. The reference resistor is used to calibrate the programmable terminating resistors used in the I/Os. Dedicated pin. Value: 1K ± 1% ohm.
DIFFRx	—	Only used if a differential driver is used in a bank. This DIFFRx must be connected to ground via an external 1K ±1% ohm resistor for all banks that have a differential driver.
SERDES Block (Dedicated Pins)		
[A:D]_HDINPx_[L/R]	I	High-speed input (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDINNx_[L/R]	I	High-speed input (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOuTPx_[L/R]	O	High-speed output (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOuTNx_[L/R]	O	High-speed output (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_REFCLKP_[L/R]	I	Ref clock input (positive), aux channel on left [L] or right [R] side of device.
[A:D]_REFCLKN_[L/R]	I	Ref clock input (negative), aux channel on left [L] or right [R] side of device.

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
F14	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
E15	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
E14	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
D9	VCCJ	-	
C16	TDO	-	TDO
B15	TMS	-	
B16	TCK	-	
E13	TDI	-	
C14	PROGRAMN	1	
C15	CCLK	1	
A15	PT43D	1	HDC/SI
A14	PT43C	1	LDCN/SCS
B14	PT41A	1	CS1
E12	PT39B	1	CS0N
D13	PT39A	1	RDN
D12	PT37D	1	WRN
E10	PT37C	1	D7
C11	PT37B	1	D6
D10	PT37A	1	D5
A13	PT36D	1	D4
B12	PT36C	1	D3
A12	PT35B	1	D2
C12	PT35A	1	D1
A11	PT33B	1	D0
B11	PT33A	1	QOUT/CEON
E9	PT32D	1	VREF2_1
E8	PT32B	1	DOUT
D8	PT28C	1	BUSYN/RCLK/SCK
A10	PT27B	1	PCLKC1_0
C10	PT27A	1	PCLKT1_0
E7	PT21C	1	VREF1_1
C9	A_VDDIB3_L	-	
A9	A_HDINP3_L	-	PCS 360 CH 3 IN P
B9	A_HDINN3_L	-	PCS 360 CH 3 IN N
A8	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B8	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
C8	A_VDDOB3_L	-	
B7	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
C7	A_VDDOB2_L	-	
A7	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
B6	A_HDINN2_L	-	PCS 360 CH 2 IN N
A6	A_HDINP2_L	-	PCS 360 CH 2 IN P
C6	A_VDDIB2_L	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
N3	PL27A	6		PL30A	6	
P3	PL27B	6		PL30B	6	
P4	PL27C	6	PCLKT6_3	PL30C	6	PCLKT6_3
P2	PL28A	6		PL31A	6	
R2	PL28B	6		PL31B	6	
T3	PL28C	6	PCLKT6_2	PL31C	6	PCLKT6_2
R3	PL28D	6	PCLKC6_2	PL31D	6	PCLKC6_2
P1	PL31A	6		PL34A	6	
R1	PL31B	6		PL34B	6	
R5	PL31C	6	VREF1_6	PL34C	6	VREF1_6
R4	PL31D	6		PL34D	6	
T2	PL32A	6		PL35A	6	
U2	PL32B	6		PL35B	6	
T1	PL33A	6		PL38A	6	
U1	PL33B	6		PL38B	6	
V1	PL35A	6		PL42A	6	
W1	PL35B	6		PL42B	6	
V6	PL35D	6	DIFFR_6	PL42D	6	DIFFR_6
V2	PL36A	6		PL43A	6	
W2	PL36B	6		PL43B	6	
Y1	PL37A	6		PL44A	6	
AA1	PL37B	6		PL44B	6	
AB1	PL39A	6		PL48A	6	
AC1	PL39B	6		PL48B	6	
Y5	PL40A	6		PL49A	6	
Y6	PL40B	6		PL49B	6	
AD2	PL41A	6		PL51A	6	
AE2	PL41B	6		PL51B	6	
AB5	PL41D	6	VREF2_6	PL51D	6	VREF2_6
AC3	PL43A	6		PL52A	6	
AD3	PL43B	6		PL52B	6	
AF1	PL44A	6		PL55A	6	
AG1	PL44B	6		PL55B	6	
AB6	PL44C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AC5	PL44D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF2	PL45A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG2	PL45B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC6	PL45C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AC7	PL45D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AE4	XRES	-		XRES	-	
AG4	VCC12	-		VCC12	-	
AD5	TEMP	6		TEMP	6	
AF5	VCC12	-		VCC12	-	
AH1	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AJ1	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF4	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AE5	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AG3	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AH2	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AD6	PB4C	5		PB4C	5	
AJ2	PB5A	5		PB5A	5	
AK2	PB5B	5		PB5B	5	
AD7	PB5C	5		PB5C	5	
AD8	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AH3	PB7A	5		PB11A	5	
AJ3	PB7B	5		PB11B	5	
AF9	PB7C	5		PB11C	5	
AE10	PB7D	5		PB11D	5	
AK3	PB8A	5		PB12A	5	
AJ4	PB8B	5		PB12B	5	
AE11	PB9A	5		PB13A	5	
AF10	PB9B	5		PB13B	5	
AK4	PB11A	5		PB16A	5	
AK5	PB11B	5		PB16B	5	
AH10	PB12A	5	PCLKT5_3	PB20A	5	PCLKT5_3
AH11	PB12B	5	PCLKC5_3	PB20B	5	PCLKC5_3
AF13	PB12C	5	PCLKT5_4	PB20C	5	PCLKT5_4
AE14	PB12D	5	PCLKC5_4	PB20D	5	PCLKC5_4
AK6	PB13A	5	PCLKT5_5	PB21A	5	PCLKT5_5
AK7	PB13B	5	PCLKC5_5	PB21B	5	PCLKC5_5
AF14	PB13C	5		PB21C	5	
AJ11	PB15A	5	PCLKT5_0	PB23A	5	PCLKT5_0
AJ12	PB15B	5	PCLKC5_0	PB23B	5	PCLKC5_0
AH13	PB15D	5	VREF2_5	PB23D	5	VREF2_5
AK8	PB16A	5	PCLKT5_1	PB24A	5	PCLKT5_1
AK9	PB16B	5	PCLKC5_1	PB24B	5	PCLKC5_1
AH14	PB17A	5	PCLKT5_2	PB25A	5	PCLKT5_2
AG14	PB17B	5	PCLKC5_2	PB25B	5	PCLKC5_2
AK10	PB19A	5		PB28A	5	
AK11	PB19B	5		PB28B	5	
AH15	PB20A	5		PB29A	5	
AG15	PB20B	5		PB29B	5	
AH12	PB21A	5		PB31A	5	
AJ13	PB21B	5		PB31B	5	
AD15	PB21C	5		PB31C	5	
AE15	PB21D	5		PB31D	5	
AK12	PB23A	5		PB32A	5	
AK13	PB23B	5		PB32B	5	
AJ14	PB24A	5		PB33A	5	
AJ15	PB24B	5		PB33B	5	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT37D	1	WRN/MPI_WR_N	PT46D	1	WRN/MPI_WR_N
F18	PT37C	1	D7/MPI_DATA7	PT46C	1	D7/MPI_DATA7
C18	PT37B	1	D6/MPI_DATA6	PT46B	1	D6/MPI_DATA6
C17	PT37A	1	D5/MPI_DATA5	PT46A	1	D5/MPI_DATA5
E17	PT36D	1	D4/MPI_DATA4	PT45D	1	D4/MPI_DATA4
E16	PT36C	1	D3/MPI_DATA3	PT45C	1	D3/MPI_DATA3
G18	PT35B	1	D2/MPI_DATA2	PT45B	1	D2/MPI_DATA2
G17	PT35A	1	D1/MPI_DATA1	PT45A	1	D1/MPI_DATA1
B18	PT33B	1	D0/MPI_DATA0	PT43B	1	D0/MPI_DATA0
B17	PT33A	1	QOUT/CEON	PT43A	1	QOUT/CEON
G16	PT32D	1	VREF2_1	PT42D	1	VREF2_1
A18	PT32B	1	DOUT	PT42B	1	DOUT
A17	PT32A	1	MCA_DONE_IN	PT42A	1	MCA_DONE_IN
H18	PT31B	1	MCA_CLK_P1_OUT	PT41B	1	MCA_CLK_P1_OUT
H17	PT31A	1	MCA_CLK_P1_IN	PT41A	1	MCA_CLK_P1_IN
D17	PT29B	1	MCA_CLK_P2_OUT	PT39B	1	MCA_CLK_P2_OUT
D16	PT29A	1	MCA_CLK_P2_IN	PT39A	1	MCA_CLK_P2_IN
F17	PT28D	1	MCA_DONE_OUT	PT38D	1	MCA_DONE_OUT
F16	PT28C	1	BUSYN/RCLK/SCK	PT38C	1	BUSYN/RCLK/SCK
C16	PT28B	1	DP0/MPI_PAR0	PT38B	1	DP0/MPI_PAR0
C15	PT28A	1	MPI_TA	PT38A	1	MPI_TA
B16	PT27B	1	PCLKC1_0	PT37B	1	PCLKC1_0
B15	PT27A	1	PCLKT1_0/MPI_CLK	PT37A	1	PCLKT1_0/MPI_CLK
H16	PT25D	1	DP3/PCLKC1_4/MPI_PAR3	PT35D	1	DP3/PCLKC1_4/MPI_PAR3
A16	PT25B	1	MPI_RETRY	PT35B	1	MPI_RETRY
A15	PT25A	1	A0/MPI_ADDR14	PT35A	1	A0/MPI_ADDR14
G15	PT24D	1	A1/MPI_ADDR15	PT33D	1	A1/MPI_ADDR15
F15	PT24C	1	A2/MPI_ADDR16	PT33C	1	A2/MPI_ADDR16
E15	PT24B	1	A3/MPI_ADDR17	PT33B	1	A3/MPI_ADDR17
D15	PT24A	1	A4/MPI_ADDR18	PT33A	1	A4/MPI_ADDR18
C14	PT23B	1	A5/MPI_ADDR19	PT32B	1	A5/MPI_ADDR19
C13	PT23A	1	A6/MPI_ADDR20	PT32A	1	A6/MPI_ADDR20
H14	PT21C	1	VREF1_1	PT31C	1	VREF1_1
B14	PT21B	1	A7/MPI_ADDR21	PT31B	1	A7/MPI_ADDR21
B13	PT21A	1	A8/MPI_ADDR22	PT31A	1	A8/MPI_ADDR22
G14	PT20B	1	A9/MPI_ADDR23	PT29B	1	A9/MPI_ADDR23
F14	PT20A	1	A10/MPI_ADDR24	PT29A	1	A10/MPI_ADDR24
A14	PT19B	1	A11/MPI_ADDR25	PT28B	1	A11/MPI_ADDR25
A13	PT19A	1	A12/MPI_ADDR26	PT28A	1	A12/MPI_ADDR26
G13	PT17D	1	D11/MPI_DATA11	PT27D	1	D11/MPI_DATA11
H13	PT17C	1	D12/MPI_DATA12	PT27C	1	D12/MPI_DATA12
E14	PT17B	1	A13/MPI_ADDR27	PT27B	1	A13/MPI_ADDR27
E13	PT17A	1	A14/MPI_ADDR28	PT27A	1	A14/MPI_ADDR28
G12	PT15D	1	A16/MPI_ADDR30	PT25D	1	A16/MPI_ADDR30
G11	PT15C	1	D13/MPI_DATA13	PT25C	1	D13/MPI_DATA13

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG11	VCCIO5	-		VCCIO5	-	
AJ9	VCCIO5	-		VCCIO5	-	
AJ23	VCCIO4	-		VCCIO4	-	
AG20	VCCIO4	-		VCCIO4	-	
AJ26	VCCIO4	-		VCCIO4	-	
AG23	VCCIO4	-		VCCIO4	-	
AC29	VCCIO3	-		VCCIO3	-	
AA26	VCCIO3	-		VCCIO3	-	
Y28	VCCIO3	-		VCCIO3	-	
AA29	VCCIO3	-		VCCIO3	-	
G30	VCCIO2	-		VCCIO2	-	
J29	VCCIO2	-		VCCIO2	-	
K27	VCCIO2	-		VCCIO2	-	
N25	VCCIO2	-		VCCIO2	-	
F20	VCCIO1	-		VCCIO1	-	
C19	VCCIO1	-		VCCIO1	-	
C12	VCCIO1	-		VCCIO1	-	
F11	VCCIO1	-		VCCIO1	-	
H1	GND	-		GND	-	
L4	GND	-		GND	-	
M3	GND	-		GND	-	
N5	GND	-		GND	-	
K2	GND	-		GND	-	
M2	GND	-		GND	-	
P6	GND	-		GND	-	
G4	GND	-		GND	-	
H3	GND	-		GND	-	
AC2	GND	-		GND	-	
AA3	GND	-		GND	-	
AE1	GND	-		GND	-	
Y4	GND	-		GND	-	
AB4	GND	-		GND	-	
AA5	GND	-		GND	-	
AE6	GND	-		GND	-	
AE8	GND	-		GND	-	
AH5	GND	-		GND	-	
AG9	GND	-		GND	-	
AG6	GND	-		GND	-	
AF11	GND	-		GND	-	
AG12	GND	-		GND	-	
AJ10	GND	-		GND	-	
AK26	GND	-		GND	-	
AJ22	GND	-		GND	-	
AF20	GND	-		GND	-	
AJ25	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT24A	1	MPI_TEA	PT30A	1	MPI_TEA
J18	PT23D	1	D14/MPI_DATA14	PT28D	1	D14/MPI_DATA14
K18	PT23C	1	DP1/MPI_PAR1	PT28C	1	DP1/MPI_PAR1
E20	PT23B	1	A21/MPI_BURST	PT27B	1	A21/MPI_BURST
F20	PT23A	1	D15/MPI_DATA15	PT27A	1	D15/MPI_DATA15
C23	B_REFCLKP_L	-		B_REFCLKP_L	-	
D23	B_REFCLKN_L	-		B_REFCLKN_L	-	
B23	VCC12	-		VCC12	-	
H21	B_VDDIB3_L	-		B_VDDIB3_L	-	
F21	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
G21	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D21	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D22	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G22	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
F22	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H22	B_VDDIB2_L	-		B_VDDIB2_L	-	
H24	B_VDDIB1_L	-		B_VDDIB1_L	-	
G23	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
H23	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
A24	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
B24	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-		B_VDDOB1_L	-	
B25	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-		B_VDDOB0_L	-	
A25	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
G25	B_HDINN0_L	-	PCS 361 CH 0 IN N	B_HDINN0_L	-	PCS 361 CH 0 IN N
F25	B_HDINP0_L	-	PCS 361 CH 0 IN P	B_HDINP0_L	-	PCS 361 CH 0 IN P
H25	B_VDDIB0_L	-		B_VDDIB0_L	-	
H26	A_VDDIB3_L	-		A_VDDIB3_L	-	
F26	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
G26	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
D26	A_VDDOB3_L	-		A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
D27	A_VDDOB2_L	-		A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
G27	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
F27	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
H27	A_VDDIB2_L	-		A_VDDIB2_L	-	
F29	A_VDDIB1_L	-		A_VDDIB1_L	-	
G28	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
H28	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A29	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B29	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
D29	A_VDDOB1_L	-		A_VDDOB1_L	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B1	GND	-		GND	-	
B32	GND	-		GND	-	
C11	GND	-		GND	-	
C12	GND	-		GND	-	
C16	GND	-		GND	-	
C21	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C25	GND	-		GND	-	
C26	GND	-		GND	-	
C27	GND	-		GND	-	
C29	GND	-		GND	-	
C3	GND	-		GND	-	
C30	GND	-		GND	-	
C4	GND	-		GND	-	
C6	GND	-		GND	-	
C7	GND	-		GND	-	
C8	GND	-		GND	-	
C9	GND	-		GND	-	
D17	GND	-		GND	-	
F18	GND	-		GND	-	
F3	GND	-		GND	-	
F30	GND	-		GND	-	
F9	GND	-		GND	-	
G15	GND	-		GND	-	
G24	GND	-		GND	-	
G29	GND	-		GND	-	
G3	GND	-		GND	-	
J14	GND	-		GND	-	
J22	GND	-		GND	-	
J26	GND	-		GND	-	
J6	GND	-		GND	-	
K11	GND	-		GND	-	
K19	GND	-		GND	-	
K30	GND	-		GND	-	
K4	GND	-		GND	-	
L23	GND	-		GND	-	
L9	GND	-		GND	-	
M13	GND	-		GND	-	
M15	GND	-		GND	-	
M18	GND	-		GND	-	
M20	GND	-		GND	-	
M27	GND	-		GND	-	
M7	GND	-		GND	-	
N12	GND	-		GND	-	
N14	GND	-		GND	-	
N19	GND	-		GND	-	
N21	GND	-		GND	-	
N29	GND	-		GND	-	
N3	GND	-		GND	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y4	PR48B	3		PR63B	3	
W4	PR48A	3		PR63A	3	
W11	PR47D	3		PR60D	3	
V11	PR47C	3		PR60C	3	
W2	PR47B	3		PR60B	3	
V2	PR47A	3		PR60A	3	
W9	PR45D	3		PR57D	3	
V9	PR45C	3		PR57C	3	
V1	PR45B	3		PR57B	3	
U1	PR45A	3		PR57A	3	
W10	PR44D	3		PR56D	3	
V10	PR44C	3		PR56C	3	
U2	PR44B	3		PR56B	3	
T2	PR44A	3		PR56A	3	
Y8	PR43D	3		PR55D	3	
W8	PR43C	3	VREF1_3	PR55C	3	VREF1_3
W5	PR43B	3		PR55B	3	
V5	PR43A	3		PR55A	3	
V7	PR40D	3	PCLKC3_2	PR52D	3	PCLKC3_2
U7	PR40C	3	PCLKT3_2	PR52C	3	PCLKT3_2
T1	PR40B	3		PR52B	3	
R1	PR40A	3		PR52A	3	
V8	PR39D	3	PCLKC3_3	PR51D	3	PCLKC3_3
U8	PR39C	3	PCLKT3_3	PR51C	3	PCLKT3_3
U5	PR39B	3		PR51B	3	
T5	PR39A	3		PR51A	3	
V6	PR38D	3	PCLKC3_1	PR50D	3	PCLKC3_1
U6	PR38C	3	PCLKT3_1	PR50C	3	PCLKT3_1
T4	PR38B	3	PCLKC3_0	PR50B	3	PCLKC3_0
T3	PR38A	3	PCLKT3_0	PR50A	3	PCLKT3_0
U9	PR36D	2	PCLKC2_2	PR48D	2	PCLKC2_2
T9	PR36C	2	PCLKT2_2	PR48C	2	PCLKT2_2
R2	PR36B	2	PCLKC2_0	PR48B	2	PCLKC2_0
P2	PR36A	2	PCLKT2_0	PR48A	2	PCLKT2_0
T11	PR35D	2	PCLKC2_3	PR47D	2	PCLKC2_3
U11	PR35C	2	PCLKT2_3	PR47C	2	PCLKT2_3
R4	PR35B	2	PCLKC2_1	PR47B	2	PCLKC2_1
R3	PR35A	2	PCLKT2_1	PR47A	2	PCLKT2_1
T8	PR34D	2		PR46D	2	
R8	PR34C	2		PR46C	2	
P1	PR34B	2		PR46B	2	
N1	PR34A	2		PR46A	2	
R6	PR31D	2		PR43D	2	
P6	PR31C	2		PR43C	2	
M1	PR31B	2		PR43B	2	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J3	PR45A	2	
M8	PR43D	2	DIFFR_2
L8	PR43C	2	VREF1_2
K4	PR43B	2	
J4	PR43A	2	
M7	PR26D	2	
L7	PR26C	2	
J5	PR26B	2	
H5	PR26A	2	
N9	PR19D	2	
P9	PR19C	2	
G3	PR19B	2	
F3	PR19A	2	
J6	PR18D	2	VREF2_2
H6	PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
D2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
G4	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
F4	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
J7	PR15D	2	
H7	PR15C	2	
G5	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
F5	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
C2	VCCJ	-	
M9	TDO	-	TDO
L9	TMS	-	
D1	TCK	-	
C1	TDI	-	
J8	PROGRAMN	1	
K8	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
B2	CCLK	1	
H9	RESP_URC	-	
H10	VCC12	-	
H8	A_REFCLKN_R	-	
G8	A_REFCLKP_R	-	
C3	VCC12	-	
D3	A_VDDIB0_R	-	
A3	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B3	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E5	VCC12	-	
A4	A_HDOUPT0_R	-	PCS 3E0 CH 0 OUT P

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
K26	GND	-	
K28	GND	-	
K6	GND	-	
K9	GND	-	
L12	GND	-	
L32	GND	-	
L4	GND	-	
M10	GND	-	
M17	GND	-	
M24	GND	-	
N29	GND	-	
N7	GND	-	
P15	GND	-	
P20	GND	-	
P3	GND	-	
P31	GND	-	
R10	GND	-	
R14	GND	-	
R16	GND	-	
R19	GND	-	
R21	GND	-	
R26	GND	-	
T15	GND	-	
T17	GND	-	
T18	GND	-	
T20	GND	-	
T28	GND	-	
T6	GND	-	
U16	GND	-	
U19	GND	-	
U23	GND	-	
U32	GND	-	
U4	GND	-	
V12	GND	-	
V16	GND	-	
V19	GND	-	
V3	GND	-	
V31	GND	-	
W15	GND	-	
W17	GND	-	
W18	GND	-	
W20	GND	-	
W29	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD33	PL59D	6		PL73D	6	
AA38	PL60A	6		PL74A	6	
AB38	PL60B	6		PL74B	6	
AC29	PL60C	6		PL74C	6	
AD29	PL60D	6		PL74D	6	
AA41	PL61A	6		PL75A	6	
AB41	PL61B	6		PL75B	6	
AC34	PL61C	6		PL75C	6	
AD34	PL61D	6		PL75D	6	
AA42	PL63A	6		PL77A	6	
AB42	PL63B	6		PL77B	6	
AC37	PL63C	6		PL77C	6	
AD37	PL63D	6		PL77D	6	
AC38	PL64A	6		PL78A	6	
AD38	PL64B	6		PL78B	6	
AD36	PL64C	6		PL78C	6	
AE36	PL64D	6		PL78D	6	
AC39	PL65A	6		PL79A	6	
AD39	PL65B	6		PL79B	6	
AD35	PL65C	6		PL79C	6	
AE35	PL65D	6		PL79D	6	
AC40	PL67A	6		PL81A	6	
AD40	PL67B	6		PL81B	6	
AE37	PL67C	6		PL81C	6	
AF37	PL67D	6		PL81D	6	
AC41	PL68A	6		PL82A	6	
AD41	PL68B	6		PL82B	6	
AE34	PL68C	6		PL82C	6	
AF34	PL68D	6		PL82D	6	
AC42	PL69A	6		PL83A	6	
AD42	PL69B	6		PL83B	6	
AE33	PL69C	6		PL83C	6	
AF33	PL69D	6		PL83D	6	
AE38	PL72A	6		PL86A	6	
AF38	PL72B	6		PL86B	6	
AE32	PL72C	6		PL86C	6	
AF32	PL72D	6		PL86D	6	
AE41	PL73A	6		PL87A	6	
AF41	PL73B	6		PL87B	6	
AE31	PL73C	6		PL87C	6	
AF31	PL73D	6		PL87D	6	
AE42	PL74A	6		PL88A	6	
AF42	PL74B	6		PL88B	6	
AG37	PL74C	6		PL88C	6	
AH37	PL74D	6		PL88D	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCI/O Bank	Dual Function	Ball Function	VCCI/O Bank	Dual Function
AP1	PR90B	3		PR109B	3	
AN1	PR90A	3		PR109A	3	
AK10	PR89D	3	VREF2_3	PR107D	3	VREF2_3
AJ10	PR89C	3		PR107C	3	
AM5	PR89B	3		PR107B	3	
AL5	PR89A	3		PR107A	3	
AL7	PR86D	3		PR104D	3	
AK7	PR86C	3		PR104C	3	
AM1	PR86B	3		PR104B	3	
AL1	PR86A	3		PR104A	3	
AJ11	PR85D	3		PR103D	3	
AH11	PR85C	3		PR103C	3	
AK5	PR85B	3		PR103B	3	
AJ5	PR85A	3		PR103A	3	
AK9	PR84D	3		PR99D	3	
AJ9	PR84C	3		PR99C	3	
AK3	PR84B	3		PR99B	3	
AJ3	PR84A	3		PR99A	3	
AK6	PR82D	3		PR98D	3	
AJ6	PR82C	3		PR98C	3	
AK2	PR82B	3		PR98B	3	
AJ2	PR82A	3		PR98A	3	
AH10	PR81D	3		PR96D	3	
AG10	PR81C	3		PR96C	3	
AK1	PR81B	3		PR96B	3	
AJ1	PR81A	3		PR96A	3	
AH9	PR80D	3		PR94D	3	
AG9	PR80C	3		PR94C	3	
AH2	PR80B	3		PR94B	3	
AG2	PR80A	3		PR94A	3	
AH8	PR78D	3		PR92D	3	
AG8	PR78C	3		PR92C	3	
AG1	PR78B	3		PR92B	3	
AH1	PR78A	3		PR92A	3	
AG14	PR77D	3		PR91D	3	
AF14	PR77C	3		PR91C	3	
AG4	PR77B	3		PR91B	3	
AF4	PR77A	3		PR91A	3	
AH7	PR76D	3	DIFFR_3	PR90D	3	DIFFR_3
AG7	PR76C	3		PR90C	3	
AG3	PR76B	3		PR90B	3	
AF3	PR76A	3		PR90A	3	
AH6	PR74D	3		PR88D	3	
AG6	PR74C	3		PR88C	3	
AF1	PR74B	3		PR88B	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D1	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
F1	VCC12	-		VCC12	-	
A3	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
E1	A_VDDOB0_R	-		A_VDDOB0_R	-	
B3	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
C2	A_VDDOB1_R	-		A_VDDOB1_R	-	
A4	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
B2	VCC12	-		VCC12	-	
B4	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
E3	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
D3	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
M10	VCC12	-		VCC12	-	
E2	A_VDDIB1_R	-		A_VDDIB1_R	-	
J11	VCC12	-		VCC12	-	
M11	A_VDDIB2_R	-		A_VDDIB2_R	-	
D4	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
E4	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
K9	VCC12	-		VCC12	-	
A5	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
D2	A_VDDOB2_R	-		A_VDDOB2_R	-	
B5	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
L10	A_VDDOB3_R	-		A_VDDOB3_R	-	
B6	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
G6	VCC12	-		VCC12	-	
A6	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
E5	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
D5	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
K12	VCC12	-		VCC12	-	
L13	A_VDDIB3_R	-		A_VDDIB3_R	-	
N14	VCC12	-		VCC12	-	
F9	B_VDDIB0_R	-		B_VDDIB0_R	-	
D6	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
E6	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
J8	VCC12	-		VCC12	-	
B7	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
G4	B_VDDOB0_R	-		B_VDDOB0_R	-	
A7	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
K8	B_VDDOB1_R	-		B_VDDOB1_R	-	
A8	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L9	VCC12	-		VCC12	-	
B8	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
E7	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
D7	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
F10	VCC12	-		VCC12	-	
K13	B_VDDIB1_R	-		B_VDDIB1_R	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L8	VCCIO2	-		VCCIO2	-	
M3	VCCIO2	-		VCCIO2	-	
P7	VCCIO2	-		VCCIO2	-	
R4	VCCIO2	-		VCCIO2	-	
T12	VCCIO2	-		VCCIO2	-	
U8	VCCIO2	-		VCCIO2	-	
V3	VCCIO2	-		VCCIO2	-	
W11	VCCIO2	-		VCCIO2	-	
Y7	VCCIO2	-		VCCIO2	-	
AB3	VCCIO3	-		VCCIO3	-	
AC7	VCCIO3	-		VCCIO3	-	
AD11	VCCIO3	-		VCCIO3	-	
AE4	VCCIO3	-		VCCIO3	-	
AF8	VCCIO3	-		VCCIO3	-	
AG12	VCCIO3	-		VCCIO3	-	
AH3	VCCIO3	-		VCCIO3	-	
AJ7	VCCIO3	-		VCCIO3	-	
AK11	VCCIO3	-		VCCIO3	-	
AL4	VCCIO3	-		VCCIO3	-	
AM8	VCCIO3	-		VCCIO3	-	
AP3	VCCIO3	-		VCCIO3	-	
AR7	VCCIO3	-		VCCIO3	-	
AU4	VCCIO3	-		VCCIO3	-	
AL16	VCCIO4	-		VCCIO4	-	
AM13	VCCIO4	-		VCCIO4	-	
AM19	VCCIO4	-		VCCIO4	-	
AR11	VCCIO4	-		VCCIO4	-	
AR17	VCCIO4	-		VCCIO4	-	
AT14	VCCIO4	-		VCCIO4	-	
AT20	VCCIO4	-		VCCIO4	-	
AT8	VCCIO4	-		VCCIO4	-	
AW15	VCCIO4	-		VCCIO4	-	
AW21	VCCIO4	-		VCCIO4	-	
AW9	VCCIO4	-		VCCIO4	-	
AY12	VCCIO4	-		VCCIO4	-	
AY18	VCCIO4	-		VCCIO4	-	
AY6	VCCIO4	-		VCCIO4	-	
AL27	VCCIO5	-		VCCIO5	-	
AM24	VCCIO5	-		VCCIO5	-	
AM30	VCCIO5	-		VCCIO5	-	
AR26	VCCIO5	-		VCCIO5	-	
AR32	VCCIO5	-		VCCIO5	-	
AT23	VCCIO5	-		VCCIO5	-	
AT29	VCCIO5	-		VCCIO5	-	
AT35	VCCIO5	-		VCCIO5	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).