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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga40e-5ff1152i

Features

■ High Performance FPGA Fabric

- 15K to 115K four input Look-up Tables (LUT4s)
- 139 to 942 I/Os
- 700MHz global clock; 1GHz edge clocks

■ 4 to 32 High Speed SERDES and flexiPCS™ (per Device)

- Performance ranging from 600Mbps to 3.8Gbps
- Excellent Rx jitter tolerance (0.8UI at 3.125Gbps)
- Low Tx jitter (0.25UI typical at 3.125Gbps)
- Built-in Pre-emphasis and equalization
- Low power (typically 105mW per channel)
- Embedded Physical Coding Sublayer (PCS) provides pre-engineered implementation for the following standards:
 - GbE, XAUI, PCI Express, SONET, Serial RapidIO, 1G Fibre Channel, 2G Fibre Channel

■ 2Gbps High Performance PURESPEED™ I/O

- Supports the following performance bandwidths
 - Differential I/O up to 2Gbps DDR (1GHz Clock)
 - Single-ended memory interfaces up to 800Mbps
- 144 Tap programmable Input Delay (INDEL) block on every I/O dynamically aligns data to clock for robust performance
 - Dynamic bit Adaptive Input Logic (AIL) monitoring and control circuitry per pin that automatically ensures proper set-up and hold
 - Dynamic bus: uses control bus from DLL
 - Static per bit
- Electrical standards supported:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2, LVTTTL
 - SSTL 3/2/18 I, II; HSTL 18/15 I, II
 - PCI, PCI-X
 - LVDS, Mini-LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS
- Programmable On Die Termination (ODT)
 - Includes Thevenin Equivalent and low power V_{TT} termination options

■ Memory Intensive FPGA

- sysMEM™ embedded Block RAM

- 1 to 7.8 Mbits memory
- True Dual Port/Pseudo Dual Port/Single Port
- Dedicated FIFO logic for all block RAM
- 500MHz performance
- Additional 240K to 1.8Mbits distributed RAM

■ sysCLOCK™ Network

- Eight analog PLLs per device
 - Frequency range from 15MHz to 1GHz
 - Spread spectrum support
- 12 DLLs per device with direct control of I/O delay
 - Frequency range from 100MHz to 700MHz
- Extensive clocking network
 - 700MHz primary and 325 MHz secondary clocks
 - 1GHz I/O-connected edge clocks
- Precision Clock Divider
 - Phase matched x2 and x4 division of incoming clocks
- Dynamic Clock Select (DCS)
 - Glitch free clock MUX

■ Masked Array for Cost Optimization (MACO™) Blocks

- On-chip structured ASIC Blocks provide pre-engineered IP for low power, low cost system level integration

■ High Performance System Bus

- Ties FPGA elements together with a standard bus framework
 - Connects to peripheral user interfaces for run-time dynamic configuration

■ System Level Support

- IEEE standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer
- IEEE Standard 1532 in-system configuration
- 1.2V and 1.0V operation
- Onboard oscillator for initialization and general use
- Embedded PowerPC microprocessor interface
- Low cost wire-bond and high pin count flip-chip packaging
- Low cost SPI Flash RAM configuration

Power Supply Ramp Rates

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
t_{RAMP}	Power supply ramp rates for all power supplies	Over process, voltage, temperature	3.45	—	—	mV/ μ s
			—	—	75	ms

1. See the Power-up and Power-Down requirements section for more details on power sequencing.
2. From 0.5V to minimum operating voltage.

Hot Socketing Specifications¹

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Programmable and dedicated Input or I/O leakage current ^{2, 3, 4, 5, 6}	$0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	—	—	± 1500	μ A
I_{HDIN}	SERDES average input current when device powered down and inputs driven ⁷		—	—	4	mA

1. See Hot Socket power up/down information in Chapter 2 of this document.
2. Assumes monotonic rise/fall rates for all power supplies.
3. Sensitive to power supply sequencing as described in hot socketing section.
4. Assumes power supplies are between 0 and maximum recommended operations conditions.
5. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} .
6. Represents DC conditions. For the first 20ns after hot insertion, current specification is 8 mA.
7. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed VDDOB of 1.575V, 8b/10b data and internal AC coupling.

DC Electrical Characteristics⁵

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min. ³	Typ.	Max.	Units
$I_{\text{IL}}, I_{\text{IH}}^1$	Input or I/O Low leakage	$0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	—	—	10	μ A
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{\text{IN}} \leq 0.7 V_{\text{CCIO}}$	-30	—	-210	μ A
I_{PD}	I/O Active Pull-down Current	$V_{\text{IL}} (\text{MAX}) \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	30	—	210	μ A
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{\text{IN}} = V_{\text{IL}} (\text{MAX})$	30	—	—	μ A
I_{BHHS}	Bus Hold High Sustaining Current	$V_{\text{IN}} = 0.7 V_{\text{CCIO}}$	-30	—	—	μ A
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	—	—	210	μ A
I_{BHLH}	Bus Hold High Overdrive Current	$0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	—	—	-210	μ A
I_{CL}	PCI Low Clamp Current	$-3 < V_{\text{IN}} \leq -1$	$-25 + (V_{\text{IN}} + 1)/0.015$	—	—	mA
I_{CH}	PCI High Clamp Current	$V_{\text{CC}} + 4 > V_{\text{IN}} \geq V_{\text{CC}} + 1$	$25 + (V_{\text{IN}} - V_{\text{CC}} - 1)/0.015$	—	—	mA
V_{BHT}	Bus Hold trip Points	$0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$	$V_{\text{IL}} (\text{MAX})$	—	$V_{\text{IH}} (\text{MIN})$	V
C1	I/O Capacitance ²	$V_{\text{CCIO}} = 3.3\text{V}, 2.5\text{V}, 1.8\text{V}, 1.5\text{V}, 1.2\text{V},$ $V_{\text{CC}} = 1.2\text{V}, V_{\text{CCIP2}} = 1.2\text{V},$ $V_{\text{CCAUX}} = 2.5, V_{\text{IO}} = 0 \text{ to } V_{\text{IH}} (\text{MAX})$	—	8	—	pf
C3 ²	Dedicated Input Capacitance ²	$V_{\text{CCIO}} = 3.3\text{V}, 2.5\text{V}, 1.8\text{V}, 1.5\text{V}, 1.2\text{V},$ $V_{\text{CC}} = 1.2\text{V}, V_{\text{CCIP2}} = 1.2\text{V},$ $V_{\text{CCAUX}} = 2.5, V_{\text{IO}} = 0 \text{ to } V_{\text{IH}} (\text{MAX})$	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_{\text{A}} = 25^{\circ}\text{C}$, $f = 1.0\text{MHz}$
3. I_{PU} , I_{PD} , I_{BHLS} and I_{BHHS} have minimum values of 15 or -15 μ A if V_{CCIO} is set to 1.2V nominal.
4. This table does not apply to SERDES pins.
5. For programmable I/Os.

LatticeSC/M Internal Timing Parameters¹ (Continued)

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Symbol	Description	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
EBR Timing									
t _{CO_EBR}	CK_Q_DEL	Clock (Read) to output from Address or Data	—	1.900	—	2.116	—	2.335	ns
t _{COO_EBR}	CK_Q_DEL	Clock (Write) to output from EBR output Register	0.390	—	0.444	—	0.498	—	ns
t _{SUDATA_EBR}	D_CK_SET	Setup Data to EBR Memory (Write clk)	-0.173	—	-0.192	—	-0.210	—	ns
t _{HDATA_EBR}	D_CK_HLD	Hold Data to EBR Memory (Write clk)	0.276	—	0.305	—	0.335	—	ns
t _{SUADDR_EBR}	A_CK_SET	Setup Address to EBR Memory (Write clk)	-0.165	—	-0.182	—	-0.200	—	ns
t _{HADDR_EBR}	A_CK_HLD	Hold Address to EBR Memory (Write clk)	0.269	—	0.298	—	0.327	—	ns
t _{SUWREN_EBR}	CE_CK_SET	Setup Write/Read Enable to EBR Memory (Write/Read clk)	0.225	—	0.226	—	0.226	—	ns
t _{HWREN_EBR}	CE_CK_HLD	Hold Write/Read Enable to EBR Memory (write/read clk)	0.073	—	0.095	—	0.116	—	ns
t _{SUCE_EBR}	CS_CK_SET	Clock Enable Setup Time to EBR Output Register (Read clk)	0.261	—	0.269	—	0.276	—	ns
t _{HCE_EBR}	CS_CK_HLD	Clock Enable Hold Time to EBR Out-put Register (Read clk)	0.023	—	0.039	—	0.055	—	ns
t _{RSTO_EBR}	RESET_Q_DEL	Reset To Output Delay Time from EBR Output Register (asynchronous)	—	0.589	—	0.673	—	0.757	ns
Cycle Boosting Timing									
t _{DEL1}	DEL1	Cycle boosting delay 1 applies to PIO, PFU, EBR	—	0.480	—	0.524	—	0.570	ns
t _{DEL2}	DEL2	Cycle boosting delay 2 applies to PIO, PFU, EBR	—	0.922	—	1.005	—	1.090	ns
t _{DEL3}	DEL3	Cycle boosting delay 3 applies to PIO, PFU, EBR	—	1.366	—	1.488	—	1.612	ns

1. Complete timing parameters for a user design will be incorporated when running ispLEVER. This is a sampling of the key timing parameters.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
RESETN		Reset. (Also sent to general routing). During configuration it resets the configuration state machine. After configuration this pin can perform the global set/reset (GSR) functions or can be used as a general input pin.
CFGIRQN	O	MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins.
TSALLN	I	Tristates all I/O.
Configuration Pads (User I/O if not used. Used during sysCONFIG.)		
HDC/SI	O	High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete. For SPI modes, this pin is used to download the read command and initial read address into the Flash memory device on the falling edge of SCK. This pin will be connected to SI of the memory. If the SPI mode is used, the 8-bit instruction code 0x03 will be downloaded followed by a 24-bit starting address of 0x000000 or a non-zero stat address for partial reconfiguration. If the SPIX mode has been selected, the 8-bit instruction captured on D[7:0] at power-up will be shifted in and followed by a 32-bit starting address of 0x000000.
LDCN/SCS	O	Low During Configuration is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete. For SPI modes, this is an active low chip select for Flash memories. It will go active after INITN goes high but before SCK begins. During power up LDCN will be low. Once INITN goes high, LDCN will go high for 100ns-200ns after which time it will go back low and configuration can begin. During the 100ns-200ns period, the read instruction will be latched for SPIX mode.
DOUT	O	Serial data output that can drive the D0/DIN of daisy-chained slave devices. The data-stream from this output will propagate preamble bits of the bitstream to daisy-chained devices. Data out on DOUT changes on the rising edge of CCLK.
QOUT/CEON	O	During daisy-chaining configuration, QOUT is the serial data output that can drive the D0/DIN of daisy-chained slave devices that do not propagate preamble bits. Data out on QOUT changes on the rising edge of CCLK. During parallel-chaining configuration, active low CEON enables the cascaded slave device to receive bitstream data.
RDN	I	Used in the asynchronous peripheral configuration mode. A low on RDN changes D[7:3] into status outputs. WRN and RDN should not be used simultaneously. If they are, the write strobe overrides.
WRN	I	When the FPGA is selected, a low on the write strobe, WRN, loads the data on D[7:0] inputs into an internal data buffer.
CS0N CS1	I	Used in the asynchronous peripheral, slave parallel and MPI modes. The FPGA is selected when CS0N is low and CS1 is high. During configuration, a pull-up is enabled on both except with MPI DMA access control.
A[21:0]	I/O	In master parallel mode, A[21:0] is an output and will address the configuration EPROMs up to 4 MB space. For MPI configuration mode, A[17:0] will be the MPI address MPL_ADDR[31:14], A[19:18] will be the transfer size and A[21:20] will be the burst mode and burst in process.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
A29	RESP_URC	-		RESP_URC	-	
D26	VCC12	-		VCC12	-	
C30	A_REFCLKN_R	-		A_REFCLKN_R	-	
B30	A_REFCLKP_R	-		A_REFCLKP_R	-	
F24	A_VDDAX25_R	-		A_VDDAX25_R	-	
D25	VCC12	-		VCC12	-	
C28	A_VDDIB0_R	-		A_VDDIB0_R	-	
B28	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B27	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E25	VCC12	-		VCC12	-	
A28	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
C27	A_VDDOB0_R	-		A_VDDOB0_R	-	
A27	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
C26	A_VDDOB1_R	-		A_VDDOB1_R	-	
A26	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
D24	VCC12	-		VCC12	-	
A25	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
B26	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
B25	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
E24	VCC12	-		VCC12	-	
C25	A_VDDIB1_R	-		A_VDDIB1_R	-	
D23	VCC12	-		VCC12	-	
C24	A_VDDIB2_R	-		A_VDDIB2_R	-	
B24	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
B23	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
E23	VCC12	-		VCC12	-	
A24	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
C23	A_VDDOB2_R	-		A_VDDOB2_R	-	
A23	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
C22	A_VDDOB3_R	-		A_VDDOB3_R	-	
A22	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
D22	VCC12	-		VCC12	-	
A21	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
B22	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
B21	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
E22	VCC12	-		VCC12	-	
C21	A_VDDIB3_R	-		A_VDDIB3_R	-	
G22	PT43D	1	HDC/SI	PT49D	1	HDC/SI
F22	PT43C	1	LDCN/SCS	PT49C	1	LDCN/SCS
B20	PT41B	1	D8/MPI_DATA8	PT49B	1	D8/MPI_DATA8
B19	PT41A	1	CS1/MPI_CS1	PT49A	1	CS1/MPI_CS1
A20	PT40D	1	D9/MPI_DATA9	PT47D	1	D9/MPI_DATA9
A19	PT40C	1	D10/MPI_DATA10	PT47C	1	D10/MPI_DATA10
D19	PT39B	1	CS0N/MPI_CS0N	PT47B	1	CS0N/MPI_CS0N
D18	PT39A	1	RDN/MPI_STRB_N	PT47A	1	RDN/MPI_STRB_N

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
U18	GND	-		GND	-	
U19	GND	-		GND	-	
U20	GND	-		GND	-	
V11	GND	-		GND	-	
V12	GND	-		GND	-	
V13	GND	-		GND	-	
V14	GND	-		GND	-	
V15	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V18	GND	-		GND	-	
V19	GND	-		GND	-	
V20	GND	-		GND	-	
W11	GND	-		GND	-	
W12	GND	-		GND	-	
W13	GND	-		GND	-	
W14	GND	-		GND	-	
W15	GND	-		GND	-	
W16	GND	-		GND	-	
W17	GND	-		GND	-	
W18	GND	-		GND	-	
W19	GND	-		GND	-	
W20	GND	-		GND	-	
Y11	GND	-		GND	-	
Y12	GND	-		GND	-	
Y13	GND	-		GND	-	
Y14	GND	-		GND	-	
Y15	GND	-		GND	-	
Y16	GND	-		GND	-	
Y17	GND	-		GND	-	
Y18	GND	-		GND	-	
Y19	GND	-		GND	-	
Y20	GND	-		GND	-	
H2	VCCIO7	-		VCCIO7	-	
N4	VCCIO7	-		VCCIO7	-	
N6	VCCIO7	-		VCCIO7	-	
J2	VCCIO7	-		VCCIO7	-	
L2	VCCIO7	-		VCCIO7	-	
H4	VCCIO7	-		VCCIO7	-	
AB2	VCCIO6	-		VCCIO6	-	
AD1	VCCIO6	-		VCCIO6	-	
W4	VCCIO6	-		VCCIO6	-	
AA4	VCCIO6	-		VCCIO6	-	
AE7	VCCIO5	-		VCCIO5	-	
AH6	VCCIO5	-		VCCIO5	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ31	PB9A	5		PB9A	5	
AH30	PB9B	5		PB9B	5	
AM30	PB11A	5		PB11A	5	
AM29	PB11B	5		PB11B	5	
AH29	PB11C	5		PB11C	5	
AH28	PB11D	5		PB11D	5	
AJ27	PB12A	5		PB13A	5	
AK27	PB12B	5		PB13B	5	
AE22	PB12C	5		PB13C	5	
AF23	PB12D	5		PB13D	5	
AL28	PB13A	5		PB15A	5	
AL27	PB13B	5		PB15B	5	
AC21	PB13C	5		PB15C	5	
AD21	PB13D	5		PB15D	5	
AM28	PB15A	5		PB17A	5	
AM27	PB15B	5		PB17B	5	
AG23	PB15C	5		PB17C	5	
AF22	PB15D	5		PB17D	5	
AG26	PB16A	5		PB19A	5	
AG25	PB16B	5		PB19B	5	
AL26	PB17A	5		PB22A	5	
AM26	PB17B	5		PB22B	5	
AJ24	PB19A	5		PB25A	5	
AK24	PB19B	5		PB25B	5	
AE21	PB19C	5		PB25C	5	
AE20	PB19D	5		PB25D	5	
AJ22	PB20A	5	PCLKT5_3	PB30A	5	PCLKT5_3
AK22	PB20B	5	PCLKC5_3	PB30B	5	PCLKC5_3
AG22	PB20C	5	PCLKT5_4	PB30C	5	PCLKT5_4
AH22	PB20D	5	PCLKC5_4	PB30D	5	PCLKC5_4
AL23	PB21A	5	PCLKT5_5	PB31A	5	PCLKT5_5
AL22	PB21B	5	PCLKC5_5	PB31B	5	PCLKC5_5
AH23	PB21C	5		PB31C	5	
AH24	PB21D	5		PB31D	5	
AJ21	PB23A	5	PCLKT5_0	PB33A	5	PCLKT5_0
AK21	PB23B	5	PCLKC5_0	PB33B	5	PCLKC5_0
AE19	PB23C	5		PB33C	5	
AF19	PB23D	5	VREF2_5	PB33D	5	VREF2_5
AM23	PB24A	5	PCLKT5_1	PB34A	5	PCLKT5_1
AM22	PB24B	5	PCLKC5_1	PB34B	5	PCLKC5_1
AH25	PB24C	5	PCLKT5_6	PB34C	5	PCLKT5_6
AH26	PB24D	5	PCLKC5_6	PB34D	5	PCLKC5_6
AL21	PB25A	5	PCLKT5_2	PB35A	5	PCLKT5_2
AL20	PB25B	5	PCLKC5_2	PB35B	5	PCLKC5_2
AG20	PB25C	5	PCLKT5_7	PB35C	5	PCLKT5_7
AG19	PB25D	5	PCLKC5_7	PB35D	5	PCLKC5_7
AJ19	PB28A	5		PB37A	5	
AK19	PB28B	5		PB37B	5	
AD18	PB28C	5		PB37C	5	
AE18	PB28D	5		PB37D	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD29	PL60D	6		PL84D	6	
AE31	PL61A	6		PL85A	6	
AF31	PL61B	6		PL85B	6	
AF30	PL61C	6		PL85C	6	
AF29	PL61D	6		PL85D	6	
AH33	PL62A	6		PL86A	6	
AJ33	PL62B	6		PL86B	6	
AC28	PL62C	6		PL86C	6	
AD28	PL62D	6		PL86D	6	
AH32	PL65A	6		PL89A	6	
AJ32	PL65B	6		PL89B	6	
AD27	PL65C	6		PL89C	6	
AE27	PL65D	6	VREF2_6	PL89D	6	VREF2_6
AG34	PL66A	6		PL90A	6	
AH34	PL66B	6		PL90B	6	
AC26	PL66C	6		PL90C	6	
AB26	PL66D	6		PL90D	6	
AK33	PL67A	6		PL91A	6	
AL33	PL67B	6		PL91B	6	
AG30	PL67C	6		PL91C	6	
AH30	PL67D	6		PL91D	6	
AL34	PL69A	6		PL93A	6	
AM34	PL69B	6		PL93B	6	
AJ30	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL93C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL93D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL70A	6		PL94A	6	
AH31	PL70B	6		PL94B	6	
AD26	PL70C	6		PL94C	6	
AD25	PL70D	6		PL94D	6	
AL32	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL95A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL95B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL95C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL95D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-		XRES	-	
AF27	TEMP	6		TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AN33	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AH29	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AJ29	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AM32	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AM31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AG27	PB4C	5		PB4C	5	
AG26	PB4D	5		PB4D	5	
AL29	PB5A	5		PB5A	5	
AL28	PB5B	5		PB5B	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K20	GND	-		GND	-	
K23	GND	-		GND	-	
K26	GND	-		GND	-	
K28	GND	-		GND	-	
K6	GND	-		GND	-	
K9	GND	-		GND	-	
L12	GND	-		GND	-	
L32	GND	-		GND	-	
L4	GND	-		GND	-	
M10	GND	-		GND	-	
M17	GND	-		GND	-	
M24	GND	-		GND	-	
N29	GND	-		GND	-	
N7	GND	-		GND	-	
P15	GND	-		GND	-	
P20	GND	-		GND	-	
P3	GND	-		GND	-	
P31	GND	-		GND	-	
R10	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
T15	GND	-		GND	-	
T17	GND	-		GND	-	
T18	GND	-		GND	-	
T20	GND	-		GND	-	
T28	GND	-		GND	-	
T6	GND	-		GND	-	
U16	GND	-		GND	-	
U19	GND	-		GND	-	
U23	GND	-		GND	-	
U32	GND	-		GND	-	
U4	GND	-		GND	-	
V12	GND	-		GND	-	
V16	GND	-		GND	-	
V19	GND	-		GND	-	
V3	GND	-		GND	-	
V31	GND	-		GND	-	
W15	GND	-		GND	-	
W17	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W29	GND	-		GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN15	PB89A	4	PCLKT4_2
AN14	PB89B	4	PCLKC4_2
AE16	PB89C	4	PCLKT4_7
AD16	PB89D	4	PCLKC4_7
AK15	PB90A	4	PCLKT4_1
AK14	PB90B	4	PCLKC4_1
AG15	PB90C	4	PCLKT4_6
AG14	PB90D	4	PCLKC4_6
AM13	PB91A	4	PCLKT4_0
AM12	PB91B	4	PCLKC4_0
AJ12	PB91C	4	VREF2_4
AJ11	PB91D	4	
AL13	PB93A	4	PCLKT4_5
AL12	PB93B	4	PCLKC4_5
AH12	PB93C	4	
AH11	PB93D	4	
AN13	PB94A	4	PCLKT4_3
AN12	PB94B	4	PCLKC4_3
AD14	PB94C	4	PCLKT4_4
AD15	PB94D	4	PCLKC4_4
AP13	PB87A	4	
AP12	PB87B	4	
AK13	PB87C	4	
AK12	PB87D	4	
AP11	PB97A	4	
AP10	PB97B	4	
AN11	PB113A	4	
AN10	PB113B	4	
AF14	PB113C	4	
AF13	PB113D	4	
AM10	PB115A	4	
AM9	PB115B	4	
AE14	PB115C	4	
AE13	PB115D	4	
AP9	PB118A	4	
AP8	PB118B	4	
AK11	PB118C	4	
AK10	PB118D	4	
AL10	PB121A	4	
AL9	PB121B	4	
AF12	PB121C	4	
AF11	PB121D	4	
AN9	PB123A	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AD5	PR94C	3	
AE2	PR94B	3	
AD2	PR94A	3	
AC5	PR92D	3	
AB5	PR92C	3	
AF1	PR92B	3	
AE1	PR92A	3	
AA11	PR91D	3	
Y11	PR91C	3	
AC4	PR91B	3	
AB4	PR91A	3	
AA8	PR90D	3	DIFFR_3
AA9	PR90C	3	
AC3	PR90B	3	
AB3	PR90A	3	
AA7	PR79D	3	
Y7	PR79C	3	
AA2	PR79B	3	
Y2	PR79A	3	
AA6	PR77D	3	
Y6	PR77C	3	
Y4	PR77B	3	
W4	PR77A	3	
W11	PR74D	3	
V11	PR74C	3	
W2	PR74B	3	
V2	PR74A	3	
W9	PR71D	3	
V9	PR71C	3	
V1	PR71B	3	
U1	PR71A	3	
W10	PR70D	3	
V10	PR70C	3	
U2	PR70B	3	
T2	PR70A	3	
Y8	PR69D	3	
W8	PR69C	3	VREF1_3
W5	PR69B	3	
V5	PR69A	3	
V7	PR66D	3	PCLKC3_2
U7	PR66C	3	PCLKT3_2
T1	PR66B	3	
R1	PR66A	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
K26	GND	-	
K28	GND	-	
K6	GND	-	
K9	GND	-	
L12	GND	-	
L32	GND	-	
L4	GND	-	
M10	GND	-	
M17	GND	-	
M24	GND	-	
N29	GND	-	
N7	GND	-	
P15	GND	-	
P20	GND	-	
P3	GND	-	
P31	GND	-	
R10	GND	-	
R14	GND	-	
R16	GND	-	
R19	GND	-	
R21	GND	-	
R26	GND	-	
T15	GND	-	
T17	GND	-	
T18	GND	-	
T20	GND	-	
T28	GND	-	
T6	GND	-	
U16	GND	-	
U19	GND	-	
U23	GND	-	
U32	GND	-	
U4	GND	-	
V12	GND	-	
V16	GND	-	
V19	GND	-	
V3	GND	-	
V31	GND	-	
W15	GND	-	
W17	GND	-	
W18	GND	-	
W20	GND	-	
W29	GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
Y18	VCC	-	
Y20	VCC	-	
AB15	VCC12	-	
AB20	VCC12	-	
N15	VCC12	-	
N20	VCC12	-	
R13	VCC12	-	
R22	VCC12	-	
Y13	VCC12	-	
Y22	VCC12	-	
AA12	VCCAUX	-	
AA23	VCCAUX	-	
AB12	VCCAUX	-	
AB16	VCCAUX	-	
AB17	VCCAUX	-	
AB18	VCCAUX	-	
AB19	VCCAUX	-	
AB23	VCCAUX	-	
AC12	VCCAUX	-	
AC13	VCCAUX	-	
Y19	GND	-	
AC14	VCCAUX	-	
AC17	VCCAUX	-	
AC21	VCCAUX	-	
AC22	VCCAUX	-	
AC23	VCCAUX	-	
M13	VCCAUX	-	
M14	VCCAUX	-	
M18	VCCAUX	-	
M21	VCCAUX	-	
M22	VCCAUX	-	
N12	VCCAUX	-	
N16	VCCAUX	-	
N17	VCCAUX	-	
N18	VCCAUX	-	
N19	VCCAUX	-	
N23	VCCAUX	-	
P12	VCCAUX	-	
P23	VCCAUX	-	
T13	VCCAUX	-	
T22	VCCAUX	-	
U12	VCCAUX	-	
U13	VCCAUX	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCI/O Bank	Dual Function	Ball Function	VCCI/O Bank	Dual Function
AE1	PR74A	3		PR88A	3	
AF12	PR73D	3		PR87D	3	
AE12	PR73C	3		PR87C	3	
AF2	PR73B	3		PR87B	3	
AE2	PR73A	3		PR87A	3	
AF11	PR72D	3		PR86D	3	
AE11	PR72C	3		PR86C	3	
AF5	PR72B	3		PR86B	3	
AE5	PR72A	3		PR86A	3	
AF10	PR69D	3		PR83D	3	
AE10	PR69C	3		PR83C	3	
AD1	PR69B	3		PR83B	3	
AC1	PR69A	3		PR83A	3	
AF9	PR68D	3		PR82D	3	
AE9	PR68C	3		PR82C	3	
AD2	PR68B	3		PR82B	3	
AC2	PR68A	3		PR82A	3	
AF6	PR67D	3		PR81D	3	
AE6	PR67C	3		PR81C	3	
AD3	PR67B	3		PR81B	3	
AC3	PR67A	3		PR81A	3	
AE8	PR65D	3		PR79D	3	
AD8	PR65C	3		PR79C	3	
AD4	PR65B	3		PR79B	3	
AC4	PR65A	3		PR79A	3	
AE7	PR64D	3		PR78D	3	
AD7	PR64C	3		PR78C	3	
AD5	PR64B	3		PR78B	3	
AC5	PR64A	3		PR78A	3	
AD6	PR63D	3		PR77D	3	
AC6	PR63C	3		PR77C	3	
AB1	PR63B	3		PR77B	3	
AA1	PR63A	3		PR77A	3	
AD9	PR61D	3		PR75D	3	
AC9	PR61C	3		PR75C	3	
AB2	PR61B	3		PR75B	3	
AA2	PR61A	3		PR75A	3	
AD14	PR60D	3		PR74D	3	
AC14	PR60C	3		PR74C	3	
AB5	PR60B	3		PR74B	3	
AA5	PR60A	3		PR74A	3	
AD10	PR59D	3		PR73D	3	
AC10	PR59C	3		PR73C	3	
Y1	PR59B	3		PR73B	3	
W1	PR59A	3		PR73A	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D1	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
F1	VCC12	-		VCC12	-	
A3	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
E1	A_VDDOB0_R	-		A_VDDOB0_R	-	
B3	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
C2	A_VDDOB1_R	-		A_VDDOB1_R	-	
A4	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
B2	VCC12	-		VCC12	-	
B4	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
E3	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
D3	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
M10	VCC12	-		VCC12	-	
E2	A_VDDIB1_R	-		A_VDDIB1_R	-	
J11	VCC12	-		VCC12	-	
M11	A_VDDIB2_R	-		A_VDDIB2_R	-	
D4	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
E4	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
K9	VCC12	-		VCC12	-	
A5	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
D2	A_VDDOB2_R	-		A_VDDOB2_R	-	
B5	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
L10	A_VDDOB3_R	-		A_VDDOB3_R	-	
B6	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
G6	VCC12	-		VCC12	-	
A6	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
E5	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
D5	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
K12	VCC12	-		VCC12	-	
L13	A_VDDIB3_R	-		A_VDDIB3_R	-	
N14	VCC12	-		VCC12	-	
F9	B_VDDIB0_R	-		B_VDDIB0_R	-	
D6	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
E6	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
J8	VCC12	-		VCC12	-	
B7	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
G4	B_VDDOB0_R	-		B_VDDOB0_R	-	
A7	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
K8	B_VDDOB1_R	-		B_VDDOB1_R	-	
A8	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L9	VCC12	-		VCC12	-	
B8	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
E7	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
D7	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
F10	VCC12	-		VCC12	-	
K13	B_VDDIB1_R	-		B_VDDIB1_R	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K14	VCC12	-		VCC12	-	
H11	B_VDDIB2_R	-		B_VDDIB2_R	-	
D8	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
E8	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
G5	VCC12	-		VCC12	-	
B9	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
L12	B_VDDOB2_R	-		B_VDDOB2_R	-	
A9	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
C5	B_VDDOB3_R	-		B_VDDOB3_R	-	
A10	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
H5	VCC12	-		VCC12	-	
B10	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
E9	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
D9	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
J13	VCC12	-		VCC12	-	
H12	B_VDDIB3_R	-		B_VDDIB3_R	-	
J12	VCC12	-		VCC12	-	
M14	B_REFCLKN_R	-		B_REFCLKN_R	-	
L14	B_REFCLKP_R	-		B_REFCLKP_R	-	
J14	VCC12	-		VCC12	-	
G12	C_VDDIB0_R	-		C_VDDIB0_R	-	
D10	C_HDINP0_R	-	PCS 3E2 CH 0 IN P	C_HDINP0_R	-	PCS 3E2 CH 0 IN P
E10	C_HDINN0_R	-	PCS 3E2 CH 0 IN N	C_HDINN0_R	-	PCS 3E2 CH 0 IN N
H6	VCC12	-		VCC12	-	
B11	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P
M12	C_VDDOB0_R	-		C_VDDOB0_R	-	
A11	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N
L11	C_VDDOB1_R	-		C_VDDOB1_R	-	
A12	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N
K11	VCC12	-		VCC12	-	
B12	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P
E11	C_HDINN1_R	-	PCS 3E2 CH 1 IN N	C_HDINN1_R	-	PCS 3E2 CH 1 IN N
D11	C_HDINP1_R	-	PCS 3E2 CH 1 IN P	C_HDINP1_R	-	PCS 3E2 CH 1 IN P
H13	VCC12	-		VCC12	-	
C6	C_VDDIB1_R	-		C_VDDIB1_R	-	
H15	VCC12	-		VCC12	-	
G13	C_VDDIB2_R	-		C_VDDIB2_R	-	
D12	C_HDINP2_R	-	PCS 3E2 CH 2 IN P	C_HDINP2_R	-	PCS 3E2 CH 2 IN P
E12	C_HDINN2_R	-	PCS 3E2 CH 2 IN N	C_HDINN2_R	-	PCS 3E2 CH 2 IN N
J9	VCC12	-		VCC12	-	
B13	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P
K10	C_VDDOB2_R	-		C_VDDOB2_R	-	
A13	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N
J10	C_VDDOB3_R	-		C_VDDOB3_R	-	
A14	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H18	PT77C	1	LDCN/SCS	PT93C	1	LDCN/SCS
F18	PT77B	1	D8/MPI_DATA8	PT93B	1	D8/MPI_DATA8
E18	PT77A	1	CS1/MPI_CS1	PT93A	1	CS1/MPI_CS1
H19	PT75D	1	D9/MPI_DATA9	PT90D	1	D9/MPI_DATA9
G19	PT75C	1	D10/MPI_DATA10	PT90C	1	D10/MPI_DATA10
D19	PT75B	1	CS0N/MPI_CS0N	PT90B	1	CS0N/MPI_CS0N
D18	PT75A	1	RDN/MPI_STRB_N	PT90A	1	RDN/MPI_STRB_N
J20	PT74D	1	WRN/MPI_WR_N	PT89D	1	WRN/MPI_WR_N
K20	PT74C	1	D7/MPI_DATA7	PT89C	1	D7/MPI_DATA7
E19	PT74B	1	D6/MPI_DATA6	PT89B	1	D6/MPI_DATA6
F19	PT74A	1	D5/MPI_DATA5	PT89A	1	D5/MPI_DATA5
K18	PT73D	1	D4/MPI_DATA4	PT87D	1	D4/MPI_DATA4
J18	PT73C	1	D3/MPI_DATA3	PT87C	1	D3/MPI_DATA3
A19	PT73B	1	D2/MPI_DATA2	PT87B	1	D2/MPI_DATA2
B19	PT73A	1	D1/MPI_DATA1	PT87A	1	D1/MPI_DATA1
H17	PT71D	1	D16/PCLKC1_3/MPI_DATA16	PT86D	1	D16/PCLKC1_3/MPI_DATA16
J17	PT71C	1	D17/PCLKT1_3/MPI_DATA17	PT86C	1	D17/PCLKT1_3/MPI_DATA17
B20	PT71B	1	D0/MPI_DATA0	PT86B	1	D0/MPI_DATA0
C20	PT71A	1	QOUT/CEON	PT86A	1	QOUT/CEON
M20	PT70D	1	VREF2_1	PT83D	1	VREF2_1
L20	PT70C	1	D18/MPI_DATA18	PT83C	1	D18/MPI_DATA18
F20	PT70B	1	DOUT	PT83B	1	DOUT
G20	PT70A	1	MCA_DONE_IN	PT83A	1	MCA_DONE_IN
K19	PT69D	1	D19/PCLKC1_2/MPI_DATA19	PT81D	1	D19/PCLKC1_2/MPI_DATA19
J19	PT69C	1	D20/PCLKT1_2/MPI_DATA20	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D20	PT69B	1	MCA_CLK_P1_OUT	PT81B	1	MCA_CLK_P1_OUT
E20	PT69A	1	MCA_CLK_P1_IN	PT81A	1	MCA_CLK_P1_IN
H21	PT67D	1	D21/PCLKC1_1/MPI_DATA21	PT78D	1	D21/PCLKC1_1/MPI_DATA21
G21	PT67C	1	D22/PCLKT1_1/MPI_DATA22	PT78C	1	D22/PCLKT1_1/MPI_DATA22
B21	PT67B	1	MCA_CLK_P2_OUT	PT78B	1	MCA_CLK_P2_OUT
C21	PT67A	1	MCA_CLK_P2_IN	PT78A	1	MCA_CLK_P2_IN
M21	PT66D	1	MCA_DONE_OUT	PT75D	1	MCA_DONE_OUT
L21	PT66C	1	BUSYN/RCLK/SCK	PT75C	1	BUSYN/RCLK/SCK
A21	PT66B	1	DP0/MPI_PAR0	PT75B	1	DP0/MPI_PAR0
A20	PT66A	1	MPI_TA	PT75A	1	MPI_TA
J21	PT65D	1	D23/MPI_DATA23	PT73D	1	D23/MPI_DATA23
K21	PT65C	1	DP2/MPI_PAR2	PT73C	1	DP2/MPI_PAR2
E21	PT65B	1	PCLKC1_0	PT73B	1	PCLKC1_0
F21	PT65A	1	PCLKT1_0/MPI_CLK	PT73A	1	PCLKT1_0/MPI_CLK
G22	PT63D	1	DP3/PCLKC1_4/MPI_PAR3	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H22	PT63C	1	D24/PCLKT1_4/MPI_DATA24	PT71C	1	D24/PCLKT1_4/MPI_DATA24
A23	PT63B	1	MPI_RETRY	PT71B	1	MPI_RETRY
A22	PT63A	1	A0/MPI_ADDR14	PT71A	1	A0/MPI_ADDR14
L22	PT61D	1	A1/MPI_ADDR15	PT69D	1	A1/MPI_ADDR15
M22	PT61C	1	A2/MPI_ADDR16	PT69C	1	A2/MPI_ADDR16

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG38	NC	-		PL95A	6	
AH38	NC	-		PL95B	6	
AJ39	NC	-		PL100A	6	
AK39	NC	-		PL100B	6	
AL41	NC	-		PL105A	6	
AM41	NC	-		PL105B	6	
AN40	NC	-		PL108A	6	
AM40	NC	-		PL108B	6	
AM39	NC	-		PL111A	6	
AN39	NC	-		PL111B	6	
AR42	NC	-		PL113A	6	
AT42	NC	-		PL113B	6	
AT1	NC	-		PR113B	3	
AR1	NC	-		PR113A	3	
AN4	NC	-		PR111B	3	
AM4	NC	-		PR111A	3	
AM3	NC	-		PR108B	3	
AN3	NC	-		PR108A	3	
AM2	NC	-		PR105B	3	
AL2	NC	-		PR105A	3	
AK4	NC	-		PR100B	3	
AJ4	NC	-		PR100A	3	
AH5	NC	-		PR95B	3	
AG5	NC	-		PR95A	3	
P6	NC	-		PR39B	2	
N6	NC	-		PR39A	2	
L3	NC	-		PR36B	2	
K3	NC	-		PR36A	2	
M5	NC	-		PR35A	2	
L4	NC	-		PR32B	2	
K4	NC	-		PR32A	2	
A2	GND	-		GND	-	
A41	GND	-		GND	-	
AA20	GND	-		GND	-	
AA23	GND	-		GND	-	
AA3	GND	-		GND	-	
AA39	GND	-		GND	-	
AB20	GND	-		GND	-	
AB23	GND	-		GND	-	
AB4	GND	-		GND	-	
AB40	GND	-		GND	-	
AC17	GND	-		GND	-	
AC19	GND	-		GND	-	
AC21	GND	-		GND	-	
AC22	GND	-		GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM27	GND	-		GND	-	
AM36	GND	-		GND	-	
AM7	GND	-		GND	-	
AP4	GND	-		GND	-	
AP40	GND	-		GND	-	
AR14	GND	-		GND	-	
AR20	GND	-		GND	-	
AR23	GND	-		GND	-	
AR29	GND	-		GND	-	
AR35	GND	-		GND	-	
AR8	GND	-		GND	-	
AT11	GND	-		GND	-	
AT17	GND	-		GND	-	
AT26	GND	-		GND	-	
AT32	GND	-		GND	-	
AU3	GND	-		GND	-	
AU39	GND	-		GND	-	
AW12	GND	-		GND	-	
AW18	GND	-		GND	-	
AW22	GND	-		GND	-	
AW28	GND	-		GND	-	
AW34	GND	-		GND	-	
AW6	GND	-		GND	-	
AY15	GND	-		GND	-	
AY21	GND	-		GND	-	
AY25	GND	-		GND	-	
AY31	GND	-		GND	-	
AY37	GND	-		GND	-	
AY9	GND	-		GND	-	
B1	GND	-		GND	-	
B42	GND	-		GND	-	
BA1	GND	-		GND	-	
BA42	GND	-		GND	-	
BB2	GND	-		GND	-	
BB41	GND	-		GND	-	
C10	GND	-		GND	-	
C12	GND	-		GND	-	
C13	GND	-		GND	-	
C16	GND	-		GND	-	
C18	GND	-		GND	-	
C19	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C27	GND	-		GND	-	
C28	GND	-		GND	-	