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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga40e-5ffn1152c

Table 1-1. LatticeSC Family Selection Guide¹

Device	SC15	SC25	SC40	SC80	SC115
LUT4s (K)	15	25	40	80	115
sysMEM Blocks (18Kb)	56	104	216	308	424
Embedded Memory (Mbits)	1.03	1.92	3.98	5.68	7.8
Max. Distributed Memory (Mbits)	0.24	0.41	0.65	1.28	1.84
Number of 3.8Gbps SERDES (Max.)	8	16	16	32	32
DLLs	12	12	12	12	12
Analog PLLs	8	8	8	8	8
MACO Blocks	4	6	10	10	12
Package I/O/SERDES Combinations (1mm ball pitch)					
256-ball fpBGA (17 x 17mm)	139/4				
900-ball fpBGA (31 x 31mm)	300/8	378/8			
1020-ball fcBGA (33 x 33mm) ²		476/16	562/16		
1152-ball fcBGA (35 x 35mm) ³			604/16	660/16	660/16
1704-ball fcBGA (42.5 x 42.5mm) ³				904/32	942/32

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per [PCN #02A-10](#).
3. Ceramic fcBGA converted to organic fcBGA per [PCN #01A-10](#).

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

Table 1-2. LatticeSCM Family

Device	SCM15	SCM25	SCM40	SCM80	SCM115
flexiMAC Blocks • 1GbE Mode • 10GbE Mode • PCI Express Mode	1	2	2	2	4
SPI4.2 Blocks	1	2	2	2	2
Memory Controller Blocks • DDR/DDR2 DRAM Mode • QDR II/II+ SRAM Mode • RLDRAM I • RLDRAM II CIO/SIO	1	2	2	2	2
Low-Speed CDR Blocks	0	0	2	2	2
PCI Express LTSSM (PHY) Blocks	1	0	2	2	2

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SPR 16x2 DPR 16x2	ROM 16x2

Logic Mode

In this mode, the LUTs in each Slice are configured as combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices in the PFU.

Ripple Mode

Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Up counter 2-bit
- Down counter 2-bit
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the Slice. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

ROM Mode

The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

- 8-bit SERDES Only
- 10-bit SERDES Only
- SONET (STS-12/STS-48)
- Gigabit Ethernet
- Fibre Channel
- XAUI
- Serial RapidIO
- PCI-Express
- Generic 8b10b

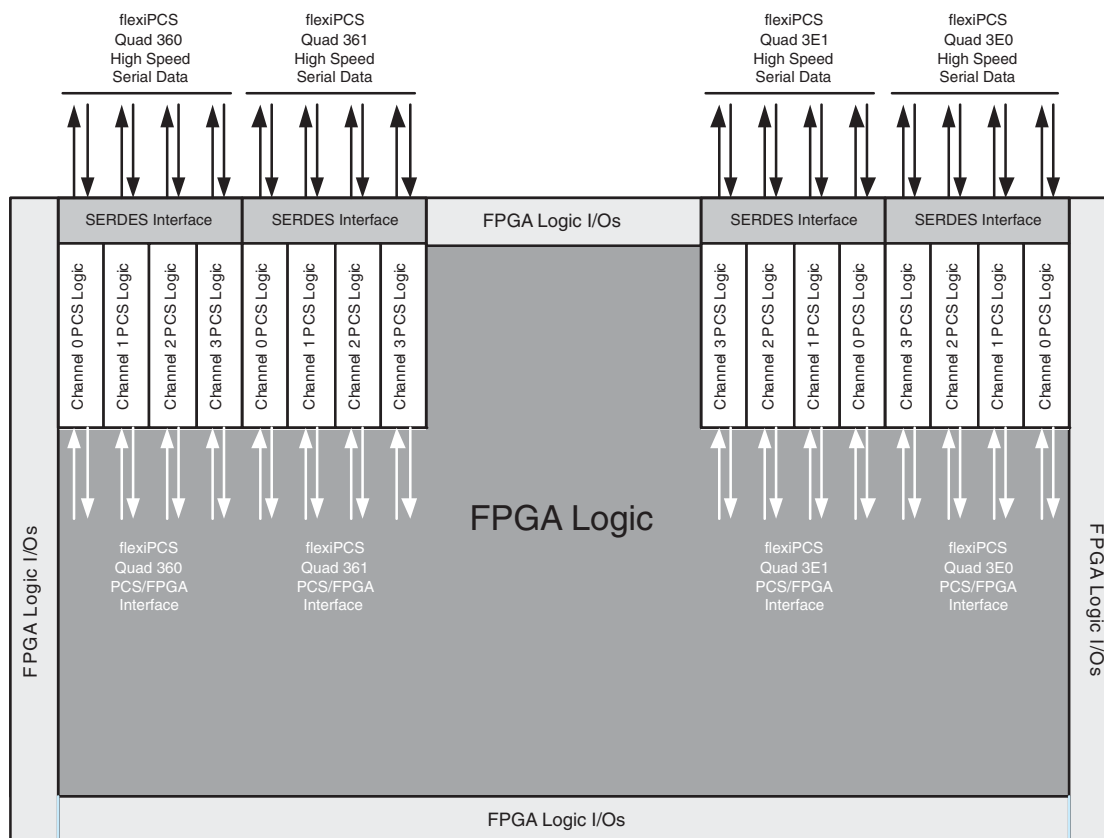
flexiPCS Quad

The flexiPCS logic is arranged in quads containing logic for four independent full-duplex data channels. Each device in the LatticeSC family has up to eight quads of flexiPCS logic. The LatticeSC Family Selection Guide table on the first page of this data sheet contains the number of flexiPCS channels present on the chip. Note that in some packages (particularly lower pin count packages), not all channels from all quads on a given device may be bonded to package pins.

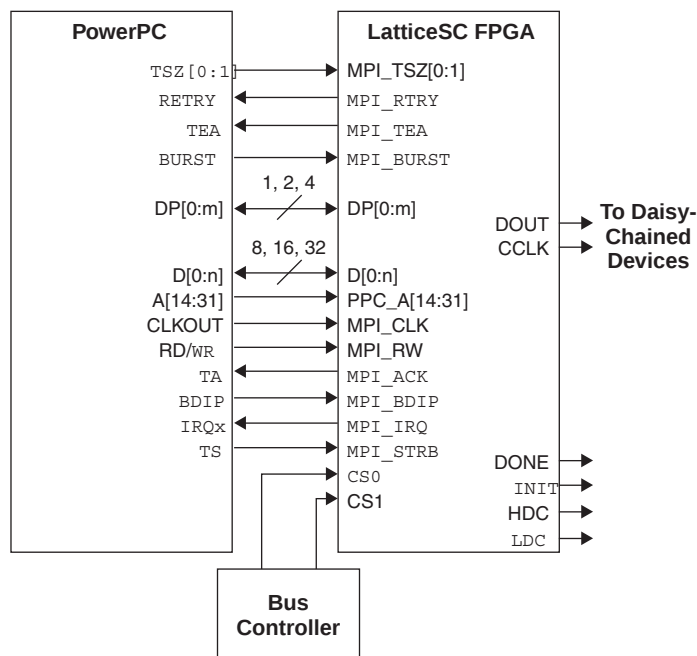
Each quad supports up to four channels of full-duplex data and can be programmed into any one of several protocol based modes. Each quad requires its own reference clock which can be sourced externally or from the FPGA logic. The user can utilize between one and four channels in a quad, depending on the application.

Figure 2-30 shows an example of four flexiPCS quads in a LatticeSC device. Quads are labeled according to the address of their software controlled registers.

Figure 2-30. LatticeSC flexiPCS



Since each quad has its own reference clock, different quads can support different standards on the same chip. This feature makes the LatticeSC family of devices ideal for bridging between different standards.

Figure 2-32. PowerPCI and MPI Schematic

Configuration and Testing

The following section describes the configuration and testing features of the LatticeSC family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeSC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS33, 25 and 18 standards. For additional detail refer to technical information at the end of the data sheet.

Device Configuration

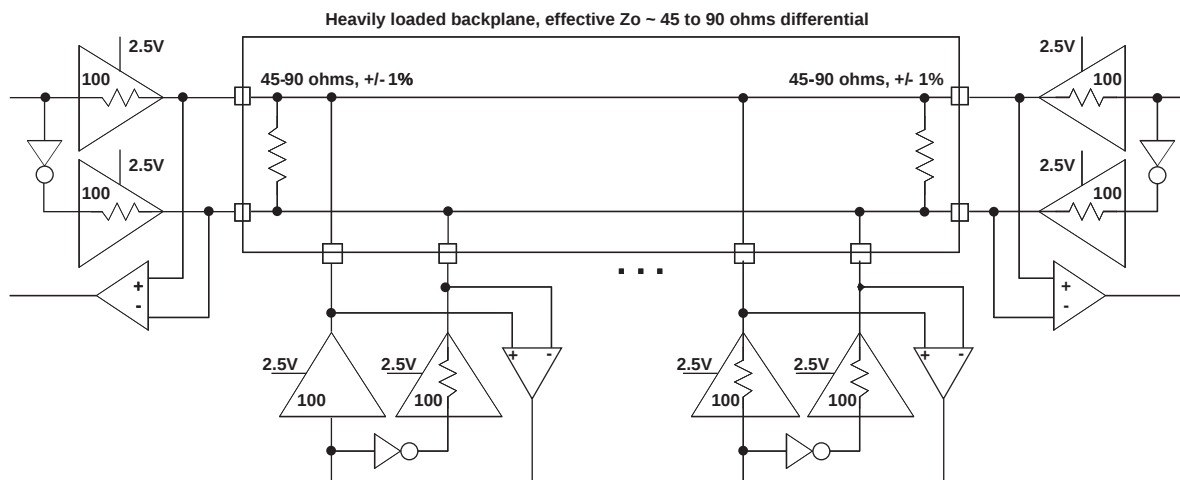
All LatticeSC devices contain three possible ports that can be used for device configuration. The serial port, which supports bit-wide configuration, and the sysCONFIG port that supports both byte-wide and serial configuration. The MPI port supports 8-bit, 16-bit or 32-bit configuration.

The serial port supports both the IEEE Std. 1149.1 Boundary Scan specification and the IEEE Std. 1532 In-System Configuration specification. The sysCONFIG port is a 20-pin interface with six of the I/Os used as dedicated pins and the rest being dual-use pins. When sysCONFIG mode is not used, these dual-use pins are available for general purpose I/O. All I/Os for the sysCONFIG and MPI ports are in I/O bank #1.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port. Once a configuration port is selected, that port is locked and another configuration port cannot be activated until the next re-initialization sequence. For additional detail refer to technical information at the end of the data sheet.

BLVDS

The LatticeSC devices support BLVDS standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example**Table 3-2. BLVDS DC Conditions¹****Over Recommended Operating Conditions**

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z _{OUT}	Output impedance	100	100	ohm
R _{TLEFT}	Left end termination	45	90	ohm
R _{TRIGHT}	Right end termination	45	90	ohm
V _{OH}	Output high voltage	1.375	1.48	V
V _{OL}	Output low voltage	1.125	1.02	V
V _{OD}	Output differential voltage	0.25	0.46	V
V _{CM}	Output common mode voltage	1.25	1.25	V
I _{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LatticeSC/M Family Timing Adders

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Input Adjusters								
LVDS	LVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
RSDS	RSDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
BLVDS25	BLVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
MLVDS25	MLVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
LVPECL33	LVPECL	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
HSTL18_I	HSTL_18 class I	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL18_II	HSTL_18 class II	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL18_III	HSTL_18 class III	-0.016	-0.018	0.008	0.003	0.032	0.023	ns
HSTL18_IV	HSTL_18 class IV	-0.016	-0.018	0.008	0.003	0.032	0.023	ns
HSTL18D_I	Differential HSTL 18 class I	0.006	0.001	0.029	0.024	0.052	0.046	ns
HSTL18D_II	Differential HSTL 18 class II	0.006	0.001	0.029	0.024	0.052	0.046	ns
HSTL15_I	HSTL_15 class I	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
HSTL15_II	HSTL_15 class II	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
HSTL15_III	HSTL_15 class III	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL15_IV	HSTL_15 class IV	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL15D_I	Differential HSTL 15 class I	-0.021	-0.022	0.001	-0.009	0.022	0.003	ns
HSTL15D_II	Differential HSTL 15 class II	-0.021	-0.022	0.001	-0.009	0.022	0.003	ns
SSTL33_I	SSTL_3 class I	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns
SSTL33_II	SSTL_3 class II	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns
SSTL33D_I	Differential SSTL_3 class I	0.012	0.012	0.034	0.028	0.055	0.043	ns
SSTL33D_II	Differential SSTL_3 class II	0.012	0.012	0.034	0.028	0.055	0.043	ns
SSTL25_I	SSTL_2 class I	0.003	-0.008	0.03	0.011	0.058	0.03	ns
SSTL25_II	SSTL_2 class II	0.003	-0.008	0.03	0.011	0.058	0.03	ns
SSTL25D_I	Differential SSTL_2 class I	0.006	0	0.031	0.023	0.056	0.046	ns
SSTL25D_II	Differential SSTL_2 class II	0.006	0	0.031	0.023	0.056	0.046	ns
SSTL18_I	SSTL_18 class I	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
SSTL18_II	SSTL_18 class II	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
SSTL18D_I	Differential SSTL_18 class I	0.006	0.001	0.029	0.024	0.052	0.046	ns
SSTL18D_II	Differential SSTL_18 class II	0.006	0.001	0.029	0.024	0.052	0.046	ns
LVTTTL33	LVTTTL	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
LVC MOS33	LVC MOS 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
LVC MOS25	LVC MOS 2.5	0	0	0	0	0	0	ns
LVC MOS18	LVC MOS 1.8	-0.068	-0.068	-0.087	-0.087	-0.105	-0.105	ns
LVC MOS15	LVC MOS 1.5	-0.131	-0.131	-0.186	-0.186	-0.241	-0.241	ns
LVC MOS12	LVC MOS 1.2	-0.238	-0.238	-0.364	-0.364	-0.49	-0.49	ns
PCI33	PCI	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
PCIX33	PCI-X 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
PCIX15	PCI-X 1.5	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
AGP1X33	AGP-1X 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
AGP2X33	AGP-2X	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.024	-0.106	0.019	-0.004	0.016	0.099	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.074	-0.134	0.08	-0.022	0.088	0.089	ns
LVC MOS18_OD	LVC MOS 1.8 open drain	0.002	-0.206	0	-0.196	-0.002	-0.221	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	-0.344	-0.164	-0.379	-0.186	-0.412	-0.209	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	-0.125	-0.137	-0.145	-0.157	-0.164	-0.176	ns
LVC MOS15_12mA	LVC MOS 1.5 12mA drive	-0.027	-0.166	-0.043	-0.07	-0.059	0.026	ns
LVC MOS15_16mA	LVC MOS 1.5 16mA drive	0.025	-0.195	0.013	-0.089	0.003	0.017	ns
LVC MOS15_OD	LVC MOS 1.5 open drain	-0.047	-0.267	-0.067	-0.267	-0.087	-0.299	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	-0.473	-0.293	-0.505	-0.317	-0.537	-0.34	ns
LVC MOS12_4mA	LVC MOS 1.2 4mA drive	-0.218	-0.239	-0.25	-0.271	-0.28	-0.303	ns
LVC MOS12_8mA	LVC MOS 1.2 8mA drive	-0.109	-0.269	-0.143	-0.181	-0.176	-0.093	ns
LVC MOS12_12mA	LVC MOS 1.2 12mA drive	-0.054	-0.3	-0.085	-0.203	-0.114	-0.106	ns
LVC MOS12_OD	LVC MOS 1.2 open drain	-0.126	-0.371	-0.166	-0.398	-0.204	-0.43	ns
PCI33	PCI	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX33	PCI-X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX15	PCI-X 1.5	0.208	0.227	0.233	0.312	0.259	0.398	ns
AGP1X33	AGP-1X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
AGP2X33	AGP-2X	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		2	—	1000	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		1.5625	—	1000	MHz
f_{VCO}	PLL VCO Frequency		100	—	1000	MHz
f_{PFD}	Phase Detector Input Frequency		2	—	700	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected (at 50% levels)	45	—	55	%
t_{OPJIT}^1	Output Clock Period Jitter	$2\text{ MHz} \leq f_{PFD} \leq 10\text{ MHz}$	—	—	200	ps
		$f_{PFD} > 10\text{ MHz}$	—	—	100	ps
t_{CPJIT}^1	Output Clock Cycle-to-Cycle Jitter		—	—	100	ps
t_{SKEW}	Output Clock-to-Clock Skew (Between Two Outputs with the Same Phase Setting)		—	—	20	ps
t_{LOCK}	PLL Lock-in Time		—	—	1	ms
t_{IPJIT}	Input Clock Period Jitter		—	—	± 250	ps
t_{HI}	Input Clock High Time	At 80% level	350	—	—	ps
t_{LO}	Input Clock Low Time	At 20% level	350	—	—	ps
t_{RSWA}	Analog Reset Signal Pulse Width		100	—	—	ns
t_{RSWD}	Digital Reset Signal Pulse Width		3	—	—	ns
t_{DEL}	Timeshift Delay Step Size		40	80	120	ps
t_{RANGE}	Timeshift Delay Range		—	± 560	—	ps
f_{SS}	Spread Spectrum Modulation Frequency		30	—	500	KHz
% Spread	Percentage Downspread for SS Mode		0.5	—	1.5	%
	VCO Clock Phase Adjustment Accuracy		-5	—	5	°

1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps

Switching Test Conditions

Figure 3-15 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-4.

Figure 3-15. Output Test Load, LVTTTL and LVCMOS Standards

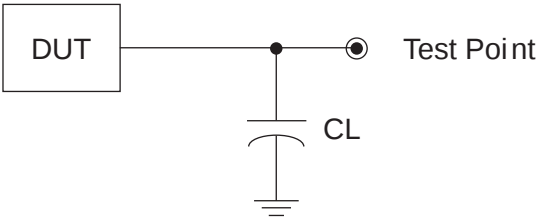


Table 3-4. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L -> H, H -> L)	30pF	LVCMOS 3.3 = 1.5V	—
		LVCMOS 2.5 = V _{CCIO} /2	—
		LVCMOS 1.8 = V _{CCIO} /2	—
		LVCMOS 1.5 = V _{CCIO} /2	—
		LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z -> H)	30pF	V _{CCIO} /2	V _{OL}
LVCMOS 2.5 I/O (Z -> L)		V _{CCIO} /2	V _{OH}
LVCMOS 2.5 I/O (H -> Z)		V _{OH} - 0.15	V _{OL}
LVCMOS 2.5 I/O (L -> Z)		V _{OL} + 0.15	V _{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E19	NC	-		NC	-	
G21	NC	-		NC	-	
G20	NC	-		NC	-	
G19	NC	-		NC	-	
F9	NC	-		NC	-	
A11	NC	-		NC	-	
G7	NC	-		NC	-	
AH9	NC	-		NC	-	
H8	VCC12	-		VCC12	-	
T8	VCC12	-		VCC12	-	
AB9	VCC12	-		VCC12	-	
AC8	VCC12	-		VCC12	-	
AB22	VCC12	-		VCC12	-	
AC23	VCC12	-		VCC12	-	
R23	VCC12	-		VCC12	-	
H23	VCC12	-		VCC12	-	
H15	VCC12	-		VCC12	-	
L24	VTT_2	2		VTT_2	2	
T23	VTT_2	2		VTT_2	2	
AC24	VTT_3	3		VTT_3	3	
T25	VTT_3	3		VTT_3	3	
W25	VTT_3	3		VTT_3	3	
AD24	VTT_4	4		VTT_4	4	
AE17	VTT_4	4		VTT_4	4	
AE18	VTT_4	4		VTT_4	4	
AC15	VTT_5	5		VTT_5	5	
AD16	VTT_5	5		VTT_5	5	
AE9	VTT_5	5		VTT_5	5	
AA6	VTT_6	6		VTT_6	6	
T7	VTT_6	6		VTT_6	6	
W6	VTT_6	6		VTT_6	6	
L7	VTT_7	7		VTT_7	7	
P7	VTT_7	7		VTT_7	7	
AA10	VCC	-		VCC	-	
AA11	VCC	-		VCC	-	
AA12	VCC	-		VCC	-	
AA13	VCC	-		VCC	-	
AA14	VCC	-		VCC	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA20	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AA22	VCC	-		VCC	-	
AA9	VCC	-		VCC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y24	PL48C	6		PL61C	6	
Y23	PL48D	6		PL61D	6	
AD29	PL49A	6		PL62A	6	
AD30	PL49B	6		PL62B	6	
AF28	PL49C	6		PL62C	6	
AE28	PL49D	6		PL62D	6	
AC28	PL51A	6		PL65A	6	
AD28	PL51B	6		PL65B	6	
AB26	PL51C	6		PL65C	6	
AC26	PL51D	6	VREF2_6	PL65D	6	VREF2_6
AC32	PL52A	6		PL66A	6	
AD32	PL52B	6		PL66B	6	
AA24	PL52C	6		PL66C	6	
AA23	PL52D	6		PL66D	6	
AE30	PL53A	6		PL67A	6	
AE29	PL53B	6		PL67B	6	
AC25	PL53C	6		PL67C	6	
AB25	PL53D	6		PL67D	6	
AE31	PL55A	6		PL69A	6	
AE32	PL55B	6		PL69B	6	
AE26	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AE27	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF32	PL56A	6		PL70A	6	
AF31	PL56B	6		PL70B	6	
AC24	PL56C	6		PL70C	6	
AD25	PL56D	6		PL70D	6	
AG32	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG31	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC23	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AD24	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AH32	XRES	-		XRES	-	
AH31	TEMP	6		TEMP	6	
AJ32	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AK32	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AF27	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AG28	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AK31	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AL31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AE25	PB4C	5		PB4C	5	
AE24	PB4D	5		PB4D	5	
AK30	PB5A	5		PB5A	5	
AL30	PB5B	5		PB5B	5	
AD23	PB5C	5		PB5C	5	
AE23	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AK29	PB7A	5		PB7A	5	
AL29	PB7B	5		PB7B	5	
AF26	PB7C	5		PB7C	5	
AF25	PB7D	5		PB7D	5	
AJ28	PB8A	5		PB8A	5	
AK28	PB8B	5		PB8B	5	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E16	PT45C	1	D3/MPI_DATA3	PT54C	1	D3/MPI_DATA3
C13	PT45B	1	D2/MPI_DATA2	PT53B	1	D2/MPI_DATA2
C14	PT45A	1	D1/MPI_DATA1	PT53A	1	D1/MPI_DATA1
B14	PT43B	1	D0/MPI_DATA0	PT51B	1	D0/MPI_DATA0
B13	PT43A	1	QOUT/CEON	PT51A	1	QOUT/CEON
L13	PT42D	1	VREF2_1	PT50D	1	VREF2_1
C15	PT42B	1	DOUT	PT50B	1	DOUT
D15	PT42A	1	MCA_DONE_IN	PT50A	1	MCA_DONE_IN
J16	PT41B	1	MCA_CLK_P1_OUT	PT49B	1	MCA_CLK_P1_OUT
K16	PT41A	1	MCA_CLK_P1_IN	PT49A	1	MCA_CLK_P1_IN
H15	PT39D	1	D21/PCLKC1_1/MPI_DATA21	PT47D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT39C	1	D22/PCLKT1_1/MPI_DATA22	PT47C	1	D22/PCLKT1_1/MPI_DATA22
A14	PT39B	1	MCA_CLK_P2_OUT	PT47B	1	MCA_CLK_P2_OUT
A13	PT39A	1	MCA_CLK_P2_IN	PT47A	1	MCA_CLK_P2_IN
G16	PT38D	1	MCA_DONE_OUT	PT46D	1	MCA_DONE_OUT
F16	PT38C	1	BUSYN/RCLK/SCK	PT46C	1	BUSYN/RCLK/SCK
B16	PT38B	1	DP0/MPI_PAR0	PT46B	1	DP0/MPI_PAR0
B15	PT38A	1	MPI_TA	PT46A	1	MPI_TA
L16	PT37C	1	DP2/MPI_PAR2	PT45C	1	DP2/MPI_PAR2
A16	PT37B	1	PCLKC1_0	PT45B	1	PCLKC1_0
A15	PT37A	1	PCLKT1_0/MPI_CLK	PT45A	1	PCLKT1_0/MPI_CLK
L17	PT35C	1	D24/PCLKT1_4/MPI_DATA24	PT43C	1	D24/PCLKT1_4/MPI_DATA24
A17	PT35B	1	MPI_RETRY	PT43B	1	MPI_RETRY
A18	PT35A	1	A0/MPI_ADDR14	PT43A	1	A0/MPI_ADDR14
F17	PT33D	1	A1/MPI_ADDR15	PT42D	1	A1/MPI_ADDR15
G17	PT33C	1	A2/MPI_ADDR16	PT42C	1	A2/MPI_ADDR16
B17	PT33B	1	A3/MPI_ADDR17	PT42B	1	A3/MPI_ADDR17
B18	PT33A	1	A4/MPI_ADDR18	PT42A	1	A4/MPI_ADDR18
H17	PT32D	1	D25/PCLKC1_5/MPI_DATA25	PT41D	1	D25/PCLKC1_5/MPI_DATA25
H18	PT32C	1	D26/PCLKT1_5/MPI_DATA26	PT41C	1	D26/PCLKT1_5/MPI_DATA26
A19	PT32B	1	A5/MPI_ADDR19	PT41B	1	A5/MPI_ADDR19
A20	PT32A	1	A6/MPI_ADDR20	PT41A	1	A6/MPI_ADDR20
L20	PT31C	1	VREF1_1	PT39C	1	VREF1_1
J17	PT31B	1	A7/MPI_ADDR21	PT39B	1	A7/MPI_ADDR21
K17	PT31A	1	A8/MPI_ADDR22	PT39A	1	A8/MPI_ADDR22
C18	PT29B	1	A9/MPI_ADDR23	PT38B	1	A9/MPI_ADDR23
D18	PT29A	1	A10/MPI_ADDR24	PT38A	1	A10/MPI_ADDR24
B19	PT28B	1	A11/MPI_ADDR25	PT37B	1	A11/MPI_ADDR25
B20	PT28A	1	A12/MPI_ADDR26	PT37A	1	A12/MPI_ADDR26
E17	PT27D	1	D11/MPI_DATA11	PT35D	1	D11/MPI_DATA11
E18	PT27C	1	D12/MPI_DATA12	PT35C	1	D12/MPI_DATA12
C20	PT27B	1	A13/MPI_ADDR27	PT35B	1	A13/MPI_ADDR27
C19	PT27A	1	A14/MPI_ADDR28	PT35A	1	A14/MPI_ADDR28
H19	PT25D	1	A16/MPI_ADDR30	PT33D	1	A16/MPI_ADDR30
G19	PT25C	1	D13/MPI_DATA13	PT33C	1	D13/MPI_DATA13
D20	PT25B	1	A15/MPI_ADDR29	PT33B	1	A15/MPI_ADDR29
D19	PT25A	1	A17/MPI_ADDR31	PT33A	1	A17/MPI_ADDR31
H20	PT24D	1	A19/MPI_TSI21	PT30D	1	A19/MPI_TSI21
G20	PT24C	1	A20/MPI_BDIP	PT30C	1	A20/MPI_BDIP
E19	PT24B	1	A18/MPI_TSI20	PT30B	1	A18/MPI_TSI20

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ9	PB78C	4		PB117C	4	
AJ8	PB78D	4		PB117D	4	
AP3	PB79A	4		PB119A	4	
AN3	PB79B	4		PB119B	4	
AF10	PB79C	4		PB119C	4	
AE10	PB79D	4		PB119D	4	
AL7	PB81A	4		PB121A	4	
AL6	PB81B	4		PB121B	4	
AK7	PB81C	4		PB121C	4	
AK6	PB81D	4		PB121D	4	
AN5	PB82A	4		PB123A	4	
AN4	PB82B	4		PB123B	4	
AH9	PB82C	4	VREF1_4	PB123C	4	VREF1_4
AH8	PB82D	4		PB123D	4	
AM3	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB124A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB124B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB83C	4		PB124C	4	
AG8	PB83D	4		PB124D	4	
AN2	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB125A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB125B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB125C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB125D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-		PROBE_VCC	-	
AF8	PROBE_GND	-		PROBE_GND	-	
AG7	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR95D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR95C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AL4	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR95B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR95A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR70D	3		PR94D	3	
AD9	PR70C	3		PR94C	3	
AH4	PR70B	3		PR94B	3	
AJ4	PR70A	3		PR94A	3	
AK5	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR93D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR93C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR69B	3		PR93B	3	
AL1	PR69A	3		PR93A	3	
AH5	PR67D	3		PR91D	3	
AG5	PR67C	3		PR91C	3	
AL2	PR67B	3		PR91B	3	
AK2	PR67A	3		PR91A	3	
AB9	PR66D	3		PR90D	3	
AC9	PR66C	3		PR90C	3	
AH1	PR66B	3		PR90B	3	
AG1	PR66A	3		PR90A	3	
AE8	PR65D	3	VREF2_3	PR89D	3	VREF2_3

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
W30	PL69B	6	VREF1_6
W27	PL69C	6	
Y27	PL69D	6	
T33	PL70A	6	
U33	PL70B	6	
V25	PL70C	6	
W25	PL70D	6	
U34	PL71A	6	
V34	PL71B	6	
V26	PL71C	6	
W26	PL71D	6	
V33	PL74A	6	
W33	PL74B	6	
V24	PL74C	6	
W24	PL74D	6	
W31	PL77A	6	
Y31	PL77B	6	
Y29	PL77C	6	
AA29	PL77D	6	
Y33	PL79A	6	
AA33	PL79B	6	
Y28	PL79C	6	
AA28	PL79D	6	
AB32	PL90A	6	
AC32	PL90B	6	
AA26	PL90C	6	
AA27	PL90D	6	
AB31	PL91A	6	DIFFR_6
AC31	PL91B	6	
Y24	PL91C	6	
AA24	PL91D	6	
AE34	PL92A	6	
AF34	PL92B	6	
AB30	PL92C	6	
AC30	PL92D	6	
AD33	PL94A	6	
AE33	PL94B	6	
AD30	PL94C	6	
AE30	PL94D	6	
AE32	PL96A	6	
AF32	PL96B	6	
AA25	PL96C	6	
AB25	PL96D	6	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
U22	VCCAUX	-	
V13	VCCAUX	-	
V22	VCCAUX	-	
V23	VCCAUX	-	
W13	VCCAUX	-	
W22	VCCAUX	-	
Y21	GND	-	
Y25	GND	-	
C18	VCCIO1	-	
D17	VCCIO1	-	
F16	VCCIO1	-	
G19	VCCIO1	-	
J20	VCCIO1	-	
K12	VCCIO1	-	
K15	VCCIO1	-	
L23	VCCIO1	-	
Y9	GND	-	
J9	VCCIO1	-	
E3	VCCIO2	-	
G6	VCCIO2	-	
H4	VCCIO2	-	
K7	VCCIO2	-	
L3	VCCIO2	-	
M11	VCCIO2	-	
N6	VCCIO2	-	
P4	VCCIO2	-	
R9	VCCIO2	-	
AA3	VCCIO3	-	
AB7	VCCIO3	-	
AC10	VCCIO3	-	
AD4	VCCIO3	-	
AE6	VCCIO3	-	
AG3	VCCIO3	-	
AK4	VCCIO3	-	
T7	VCCIO3	-	
U3	VCCIO3	-	
V4	VCCIO3	-	
W6	VCCIO3	-	
Y10	VCCIO3	-	
AD12	VCCIO4	-	
AF15	VCCIO4	-	
AF9	VCCIO4	-	
AH10	VCCIO4	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AY41	PB12A	5		PB13A	5	
BA41	PB12B	5		PB13B	5	
AT39	PB12C	5		PB13C	5	
AT38	PB12D	5		PB13D	5	
AV37	PB13A	5		PB15A	5	
AV36	PB13B	5		PB15B	5	
AM31	PB13C	5		PB15C	5	
AM32	PB13D	5		PB15D	5	
BA40	PB15A	5		PB16A	5	
BB40	PB15B	5		PB16B	5	
AM29	PB15C	5		PB16C	5	
AL29	PB15D	5		PB16D	5	
AY39	PB16A	5		PB17A	5	
AY38	PB16B	5		PB17B	5	
AN33	PB16C	5		PB17C	5	
AN32	PB16D	5		PB17D	5	
BA39	PB17A	5		PB19A	5	
BA38	PB17B	5		PB19B	5	
AT37	PB17C	5		PB19C	5	
AT36	PB17D	5		PB19D	5	
AW36	PB19A	5		PB20A	5	
AW35	PB19B	5		PB20B	5	
AM28	PB19C	5		PB20C	5	
AL28	PB19D	5		PB20D	5	
BB38	PB20A	5		PB21A	5	
BB39	PB20B	5		PB21B	5	
AR34	PB20C	5		PB21C	5	
AR33	PB20D	5		PB21D	5	
AV35	PB21A	5		PB23A	5	
AV34	PB21B	5		PB23B	5	
AT33	PB21C	5		PB23C	5	
AT34	PB21D	5		PB23D	5	
BA37	PB23A	5		PB25A	5	
BA36	PB23B	5		PB25B	5	
AP33	PB23C	5		PB25C	5	
AP32	PB23D	5		PB25D	5	
AY36	PB24A	5		PB26A	5	
AY35	PB24B	5		PB26B	5	
AN31	PB24C	5		PB26C	5	
AN30	PB24D	5		PB26D	5	
BB37	PB25A	5		PB27A	5	
BB36	PB25B	5		PB27B	5	
AP31	PB25C	5		PB27C	5	
AP30	PB25D	5		PB27D	5	
AV33	PB27A	5		PB29A	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
A26	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N
C34	D_VDDOB2_L	-		D_VDDOB2_L	-	
B26	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P
C32	VCC12	-		VCC12	-	
E27	D_HDINN2_L	-	PCS 363 CH 2 IN N	D_HDINN2_L	-	PCS 363 CH 2 IN N
D27	D_HDINP2_L	-	PCS 363 CH 2 IN P	D_HDINP2_L	-	PCS 363 CH 2 IN P
G25	D_VDDIB2_L	-		D_VDDIB2_L	-	
F29	VCC12	-		VCC12	-	
H26	D_VDDIB1_L	-		D_VDDIB1_L	-	
F30	VCC12	-		VCC12	-	
D28	D_HDINP1_L	-	PCS 363 CH 1 IN P	D_HDINP1_L	-	PCS 363 CH 1 IN P
E28	D_HDINN1_L	-	PCS 363 CH 1 IN N	D_HDINN1_L	-	PCS 363 CH 1 IN N
B27	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P
F36	VCC12	-		VCC12	-	
A27	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N
F35	D_VDDOB1_L	-		D_VDDOB1_L	-	
A28	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N
M30	D_VDDOB0_L	-		D_VDDOB0_L	-	
B28	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P
F37	VCC12	-		VCC12	-	
E29	D_HDINN0_L	-	PCS 363 CH 0 IN N	D_HDINN0_L	-	PCS 363 CH 0 IN N
D29	D_HDINP0_L	-	PCS 363 CH 0 IN P	D_HDINP0_L	-	PCS 363 CH 0 IN P
H27	D_VDDIB0_L	-		D_VDDIB0_L	-	
G28	VCC12	-		VCC12	-	
J28	C_REFCLKP_L	-		C_REFCLKP_L	-	
K28	C_REFCLKN_L	-		C_REFCLKN_L	-	
F32	VCC12	-		VCC12	-	
G29	C_VDDIB3_L	-		C_VDDIB3_L	-	
C31	VCC12	-		VCC12	-	
D30	C_HDINP3_L	-	PCS 362 CH 3 IN P	C_HDINP3_L	-	PCS 362 CH 3 IN P
E30	C_HDINN3_L	-	PCS 362 CH 3 IN N	C_HDINN3_L	-	PCS 362 CH 3 IN N
B29	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P
F38	VCC12	-		VCC12	-	
A29	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N
J33	C_VDDOB3_L	-		C_VDDOB3_L	-	
A30	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N
K33	C_VDDOB2_L	-		C_VDDOB2_L	-	
B30	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P
J34	VCC12	-		VCC12	-	
F31	C_HDINN2_L	-	PCS 362 CH 2 IN N	C_HDINN2_L	-	PCS 362 CH 2 IN N
E31	C_HDINP2_L	-	PCS 362 CH 2 IN P	C_HDINP2_L	-	PCS 362 CH 2 IN P
G30	C_VDDIB2_L	-		C_VDDIB2_L	-	
H28	VCC12	-		VCC12	-	
C37	C_VDDIB1_L	-		C_VDDIB1_L	-	
H30	VCC12	-		VCC12	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-7FFN1020C ¹	-7	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-6FFN1020C ¹	-6	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-5FFN1020C ¹	-5	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-7FCN1152C ²	-7	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-6FCN1152C ²	-6	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-5FCN1152C ²	-5	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	40.4
LFSC3GA40E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	40.4
LFSC3GA40E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-7FFN1020C ¹	-7	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-6FFN1020C ¹	-6	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-5FFN1020C ¹	-5	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-7FFAN1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-6FFAN1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-5FFAN1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-7FCN1152C ²	-7	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FCN1152C ²	-6	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FCN1152C ²	-5	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-7FFN1152C	-7	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FFN1152C	-6	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FFN1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Date	Version	Section	Change Summary
August 2006 (cont.)	01.3 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Family Timing Adders with ispLEVER 6.0 SP1 results
			Updated PLL Timing Parameters based on PDE testing results
			Removed RDDATA parameter from sysCONFIG readback timing table
		Multiple	Changed TDO/RDDATA to TDO
		Pinout Information	Removed all MPI signals from SC15 256 pin package Dual Function Column
			Added note to SC15, SC25 900 pin package that the package supports a 16 bit MPI
			Added note that pin D3 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note that pin D28 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note to SC25 1020 pin package that the package supports a 16 bit MPI
			Added note to SC80 1152 pin package that the package supports a 32 bit MPI
			Added note to SC80 1704 pin package that the package supports a 32 bit MPI
		Ordering Information	Changed "fcBGA" for the 1020 packages to "ffBGA"
November 2006	01.4	Introduction	LatticeSC Family Selection Guide table – I/O count for SC80 device, 1704 fcBGA package changed to 904/32. I/O count for SC115 device, 1704 fcBGA package changed to 942/32.
		DC and Switching Characteristics	DC Electrical Characteristics table – Updated the initialization and standby supply current values.
			DC Electrical Characteristics table – Updated the sysCONFIG Master Parallel mode RCLK low and RCLK high time specifications.
			DC Electrical Characteristics table – Updated VCCIO values for LVPECL33 I/Os.
		Pin Information	Pin Information Summary table - Changed number of single ended user I/Os from 906 to 904 for 1704 fcBGA.
			Removed the single-ended only output restriction on pins D3 and D28 in an SC15 and SC25 900 pin package.
		Ordering Information	Ordering Information tables - Changed number of I/Os from 906 to 904 for 1704 fcBGA.
			Added ordering part numbers for LatticeSC/SCM 40K and 115K LUT devices.
			Added lead-free ordering part numbers.
		Multiple	Changed number of available SC80 I/O from 906 to 904. Changed number of available SC115 I/O from 944 to 942.
January 2007	01.4a	Architecture	Added EBR Asynchronous Reset section.
February 2007	01.4b	Architecture	Updated EBR Asynchronous Reset section.
March 2007	01.5	Architecture	Added EBR asynchronous reset clarification
			Clarified that differential drivers are not supported in banks 1, 4 and 5
		DC and Switching Characteristics	Added clarification for the description of the junction temperature specification in the Absolute Maximum Ratings section.
			Updated Initialization and Standby Current table. Updated LatticeSC External Switching Characteristics with ispLEVER 6.1 SP1 results.

Date	Version	Section	Change Summary
December 2011	02.4	DC and Switching Characteristics	Updated JTAG Port Timing Specifications table.