Lattice Semiconductor Corporation - LFSC3GA40E-5FFN1152I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

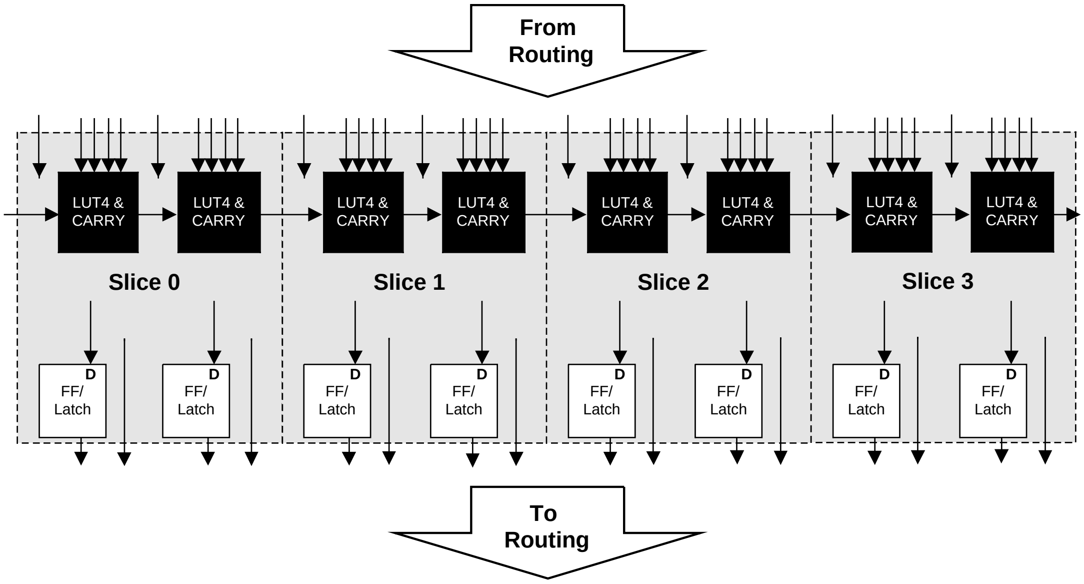
Details	
Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga40e-5ffn1152i

PFU Blocks

The core of the LatticeSC devices consists of PFU blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-2. PFU Diagram

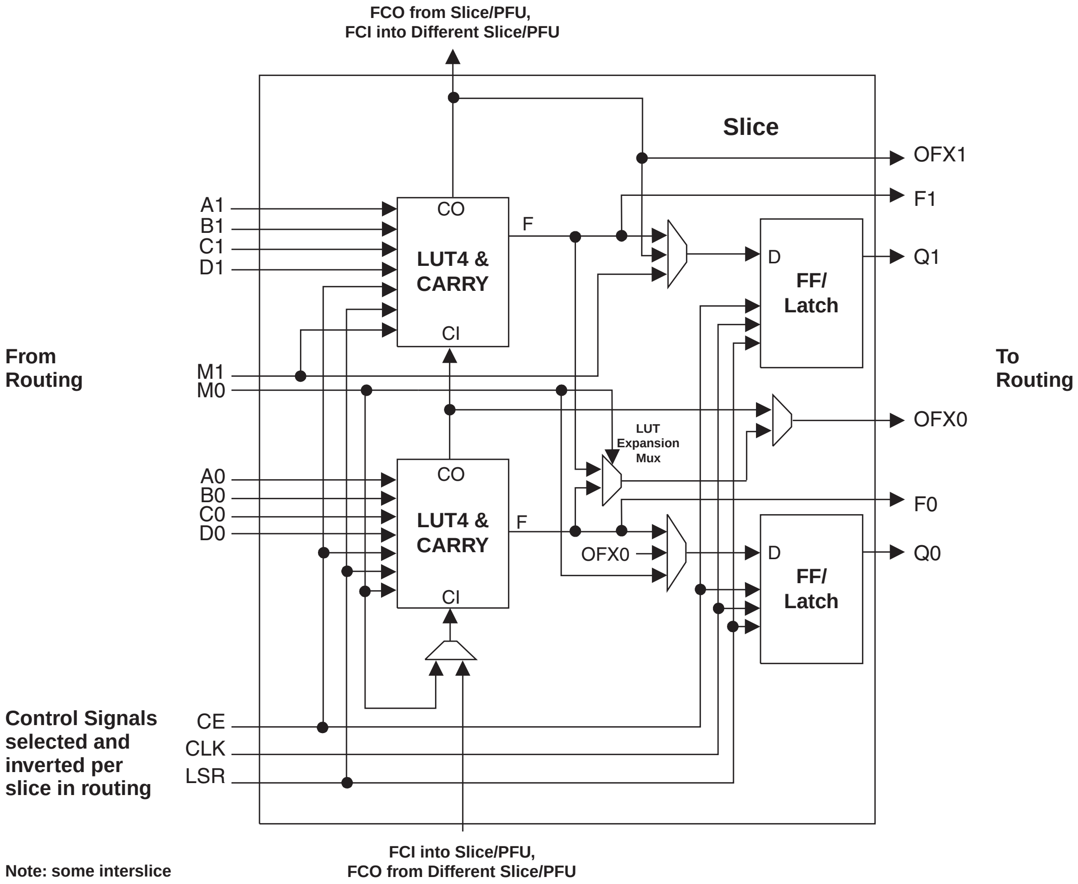


Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to implement 5, 6, 7 and 8 Input LUTs (LUT5, LUT6, LUT7 and LUT8). There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-3. Slice Diagram



Note: some interslice signals not shown.

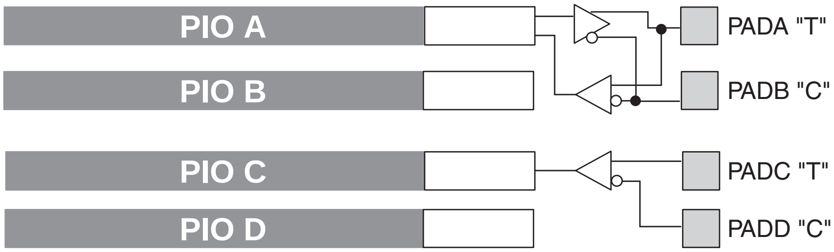
Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[2]

1. See Figure 2-2 for connection details.
2. Requires two PFUs.

high-speed interfaces in the LatticeSC devices. Figure 2-18 shows how differential receivers and drivers are arranged between PIOs.

Figure 2-18. Differential Drivers and Receivers



*Differential Driver only available on right and left of the device.

PIO

The PIO contains five blocks: an input register block, output register block, tristate register block, update block, and a control logic block. These blocks contain registers for both single data rate (SDR), double data rate (DDR), and shift register operation along with the necessary clock and selection logic.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 show the diagram of the input register block. The signal from the PURE-SPEED I/O buffer (DI) enters the input register block and can be used for three purposes, as a source for the combinatorial (INDD) and clock outputs (INCK), the input into the SDR register/latch block and the input to the delay block. The output of the delay block can be used as combinatorial (INDD) and clock (INCK) outputs, an input to the DDR/Shift Register Block or an input into the SDR register block.

Input SDR Register/Latch Block

The SDR register/latch block has a latch and a register/latch that can be used in a variety of combinations to provide a registered or latched output (INFF). The latch operates off high-speed input clocks and latches data on the positive going edge. The register/latch operates off the low-speed input clock and registers/latches data on the positive going edge. Both the latch and the register/latch have a clock enable input that is driven by the input clock enable. In addition both have a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register and latch LSR inputs are driven from LSRI, which is generated from the PIO control MUX. The GSR inputs are driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Input Delay Block

The delay block uses 144 tapped delay lines to obtain coarse and fine delay resolution. These delays can be adjusted during configuration or automatically via DLL or AIL blocks. The Adaptive Input Logic (AIL) uses this delay block to adjust automatically the delay in the data path to ensure that it has sufficient setup and hold time.

The delay line in this block matches the delay line that is used in the 12 on-chip DLLs. The delay line can be set via configuration bits or driven from a calibration bus that allows the setting to be controlled either from one of the on-chip DLLs or user logic. Controlling the delay from one of the on-chip DLLs allow the delay to be calibrated to the DLL clock and hence compensated for the variations in process, voltage and temperature.

Table 2-9. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)	On-chip Termination
Single Ended Interfaces			
LVTTL33[3]	—	3.3	None
LVCMOS 33, 25, 18, 15, 12[3]	—	3.3/2.5/1.8/1.5/1.2	None
PCI33, PCIX33, AGP1X33[3]	—	3.3	None
PCIX15	0.75	1.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
AGP2X33	1.32	—	None
HSTL18_I, II	0.9	1.8[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL18_III, IV	1.08	1.8[2]	None / V_{CCIO}: 50
HSTL15_I, II	0.75	1.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL15_III, IV	0.9	1.5[2]	None / V_{CCIO}: 50
SSTL33_I, II	1.5	3.3	None
SSTL25_I, II	1.25	2.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL18_I, II	0.9	1.8[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
GTL+, GTL	1.0 / 0.8	1.5 / 1.2[2]	None / V_{CCIO}: 50
Differential Interfaces			
SSTL18D_I, II	—	1.8[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL25D_I, II	—	2.5[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL33D_I, II	—	3.3	None
HSTL15D_I, II	—	1.5[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL18D_I, II	—	1.8[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
LVDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240
Mini-LVDS	—	—	None / Diff: 120, 150 / Diff to V_{CMT}: 120, 150
BLVDS25	—	—	None
MLVDS25	—	—	None
RSDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240
LVPECL33	—	≤ 2.5	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.
2. V_{CCIO} needed for on-chip termination to $V_{CCIO}/2$ or V_{CCIO} only. V_{CCIO} is not specified for off-chip termination or V_{TT} termination.
3. All ratioed input buffers and dedicated pin input buffers include hysteresis with a typical value of 50mV.

PURESPEED I/O Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input voltage		0	—	2.4	V
V_{THD}	Differential input threshold ($Q-\overline{Q}$)		+/-100	—	—	mV
V_{CM}	Input common mode voltage		0.05	1.2	2.35	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{SAB}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	12	mA
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	500	ps	T_R, T_F

Notes:

1. Data is for 3.5mA differential current drive. Other differential driver current options are available.
2. If the low power mode of the input buffer is used, the minimum V_{CM} is 600 mV.

Mini-LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	ohms
R_T	Differential termination resistance	60	100	150	ohms
V_{OD}	Output voltage, differential, $\|V_{OP} - V_{OM}\|$	300	—	600	mV
V_{OS}	Output voltage, common mode, $\|V_{OP} + V_{OM}\|/2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD}, between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS}, between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $\|V_{INP} - V_{INM}\|$	200	—	600	mV
V_{CM}	Input voltage, common mode, $\|V_{INP} + V_{INM}\|/2$	0.3+(V_{THD}/2)	—	2.1-(V_{THD}/2)	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	500	ps
T_{ODUTY}	Output clock duty cycle	45	—	55	%
T_{IDUTY}	Input clock duty cycle	40	—	60	%

Note: Data is for 6mA differential current drive. Other differential driver current options are available.

LatticeSC/M Internal Timing Parameters[1] (Continued)

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Symbol	Description	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
EBR Timing									
t_{CO_EBR}	CK_Q_DEL	Clock (Read) to output from Address or Data	—	1.900	—	2.116	—	2.335	ns
t_{COO_EBR}	CK_Q_DEL	Clock (Write) to output from EBR output Register	0.390	—	0.444	—	0.498	—	ns
t_{SUDATA_EBR}	D_CK_SET	Setup Data to EBR Memory (Write clk)	-0.173	—	-0.192	—	-0.210	—	ns
t_{HDATA_EBR}	D_CK_HLD	Hold Data to EBR Memory (Write clk)	0.276	—	0.305	—	0.335	—	ns
t_{SUADDR_EBR}	A_CK_SET	Setup Address to EBR Memory (Write clk)	-0.165	—	-0.182	—	-0.200	—	ns
t_{HADDR_EBR}	A_CK_HLD	Hold Address to EBR Memory (Write clk)	0.269	—	0.298	—	0.327	—	ns
t_{SUWREN_EBR}	CE_CK_SET	Setup Write/Read Enable to EBR Memory (Write/Read clk)	0.225	—	0.226	—	0.226	—	ns
t_{HWREN_EBR}	CE_CK_HLD	Hold Write/Read Enable to EBR Memory (write/read clk)	0.073	—	0.095	—	0.116	—	ns
t_{SUCE_EBR}	CS_CK_SET	Clock Enable Setup Time to EBR Output Register (Read clk)	0.261	—	0.269	—	0.276	—	ns
t_{HCE_EBR}	CS_CK_HLD	Clock Enable Hold Time to EBR Output Register (Read clk)	0.023	—	0.039	—	0.055	—	ns
t_{RSTO_EBR}	RESET_Q_DEL	Reset To Output Delay Time from EBR Output Register (asynchronous)	—	0.589	—	0.673	—	0.757	ns
Cycle Boosting Timing									
t_{DEL1}	DEL1	Cycle boosting delay 1 applies to PIO, PFU, EBR	—	0.480	—	0.524	—	0.570	ns
t_{DEL2}	DEL2	Cycle boosting delay 2 applies to PIO, PFU, EBR	—	0.922	—	1.005	—	1.090	ns
t_{DEL3}	DEL3	Cycle boosting delay 3 applies to PIO, PFU, EBR	—	1.366	—	1.488	—	1.612	ns

1. Complete timing parameters for a user design will be incorporated when running ispLEVER. This is a sampling of the key timing parameters.

Figure 3-8. Read Mode with Input and Output Registers

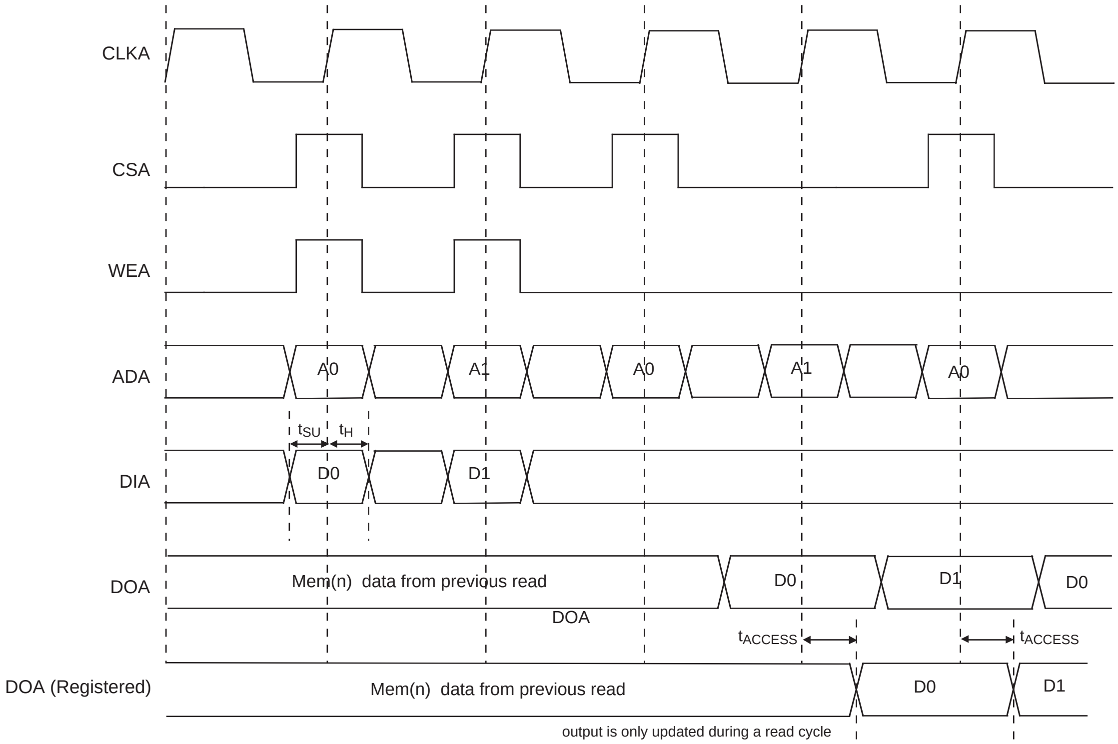
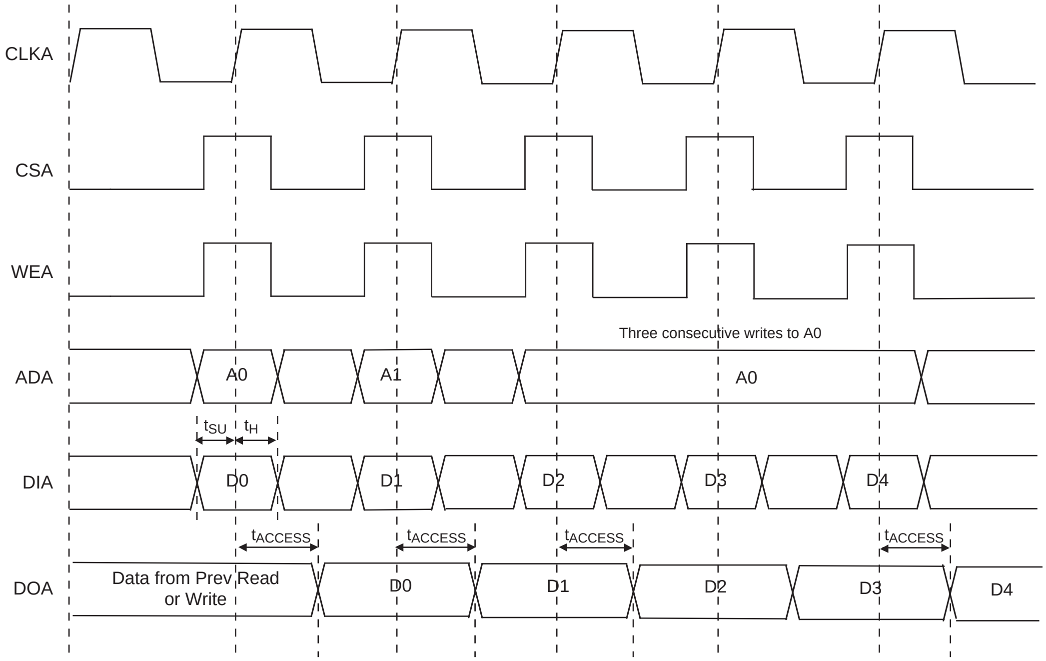


Figure 3-9. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-12. Waveforms First Read after Full Flag

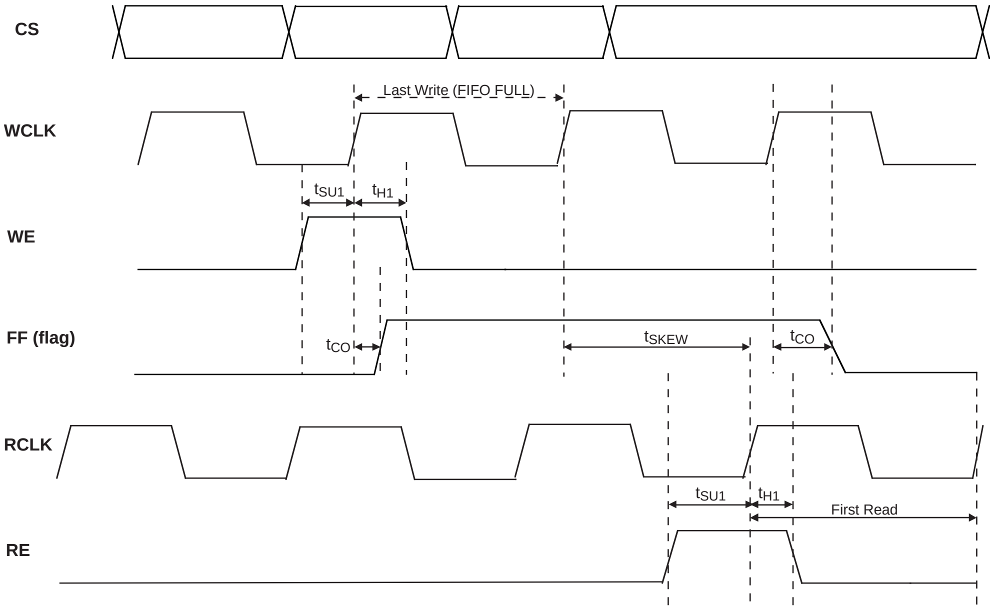
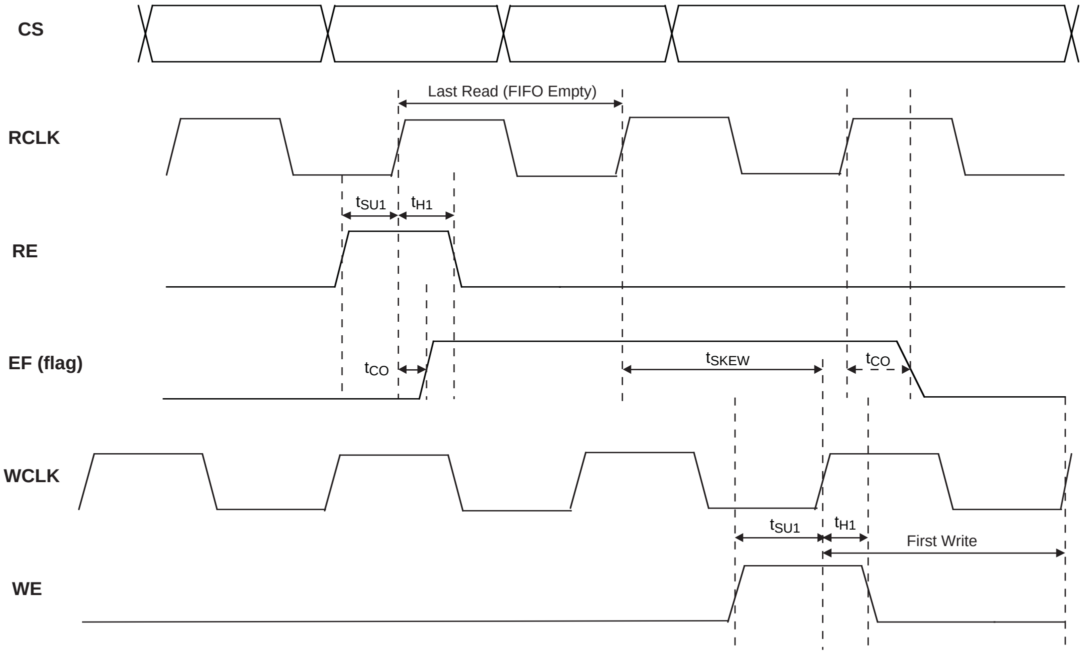


Figure 3-13. Waveform First Write after Empty Flag



LatticeSC/M sysCONFIG Port Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
General Configuration Timing				
t_{SMODE}	M[3:0] Setup Time to INITN High	0	—	ns
t_{HMODE}	M[3:0] Hold Time from INITN High	600	—	ns
t_{RW}	RESETN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
t_{PGW}	PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
$f_{ESB\_CLK\_FRQ}$	System Bus ESB_CLK Frequency (No Wait States)	—	133	MHz
sysCONFIG Master Parallel Configuration Mode				
t_{SMB}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMB}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMB}	RCLK Low Time (Non-compressed Bitstreams)	0.5	0.5	CCLK periods
	RCLK Low Time (Compressed Bitstreams)	0.5	7.5	CCLK periods
t_{CHMB}	RCLK High Time	0.5	0.5	CCLK periods
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CSCK Low	—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low	0	2	µs
t_{SCK}	CSCK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CSCK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN Low to CSCK high Setup Time	—	15	ns
f_{MAXSPI}	Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0)	—	50	MHz
t_{SUSPI}	SOSPI/D0 Data Setup Time Before CSCK	7	—	ns
t_{HSPI}	SOSPI/D0 Data Hold Time After CSCK	2	—	ns
	Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
	Duty Cycle	40	60	%
sysCONFIG Master Serial Configuration Mode				
t_{SMS}	DIN Setup Time	4.4	—	ns
t_{HMS}	DIN Hold Time	0	—	ns
f_{CMS}	CCLK Frequency (No Divider)	90	190	MHz
f_{C_DIV}	CCLK Frequency (Div 128)	0.70	1.48	MHz
t_{D}	CCLK to DOUT Delay	—	7.5	ns
sysCONFIG Master Parallel Configuration Mode				
t_{AVMP}	RCLK to Address Valid	—	10	ns
t_{SMP}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMP}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMP}	RCLK Low Time (Non-compressed Bitstream)	7.5	7.5	CCLK periods
	RCLK Low Time (Compressed Bitstream)	0.5	63.5	
t_{CHMP}	RCLK High Time	0.5	0.5	CCLK periods
t_{DMP}	CCLK to DOUT	—	7.5	ns

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
J9	VCC	-	
K8	VCC	-	
F6	VCC12	-	
F11	VCC12	-	
L11	VCC12	-	
L6	VCC12	-	
K7	VCC12	-	
K10	VCC12	-	
F10	VCCAUX	-	
F7	VCCAUX	-	
T1	GND	-	
G11	VCCAUX	-	
K11	VCCAUX	-	
L10	VCCAUX	-	
L9	VCCAUX	-	
L7	VCCAUX	-	
L8	VCCAUX	-	
T16	GND	-	
G6	VCCAUX	-	
K6	VCCAUX	-	
B13	VCCIO1	-	
D11	VCCIO1	-	
D14	VCCIO1	-	
F12	VCCIO2	-	
G15	VCCIO2	-	
K14	VCCIO3	-	
N15	VCCIO3	-	
M11	VCCIO4	-	
P13	VCCIO4	-	
R10	VCCIO4	-	
N6	VCCIO5	-	
P7	VCCIO5	-	
R4	VCCIO5	-	
K2	VCCIO6	-	
N3	VCCIO6	-	
F4	VCCIO7	-	
G3	VCCIO7	-	
D4	VCC12	-	
D7	VCC12	-	
D5	VCC12	-	
D6	VCC12	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M15 in a 256-pin package does not support an MPI interface.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G1	NC	-		PL20B	7	
M4	NC	-		NC	-	
J3	NC	-		NC	-	
P5	NC	-		NC	-	
W5	NC	-		PL48C	6	
T6	NC	-		PL35C	6	
U3	NC	-		PL36A	6	
V3	NC	-		PL36B	6	
T5	NC	-		PL39A	6	
T4	NC	-		PL39B	6	
V5	NC	-		PL43C	6	
U6	NC	-		PL42C	6	
U4	NC	-		PL40A	6	
U5	NC	-		PL40B	6	
V4	NC	-		PL43D	6	
Y2	NC	-		PL47A	6	
AA2	NC	-		PL47B	6	
W3	NC	-		PL47D	6	
Y3	NC	-		PL47C	6	
AB3	NC	-		NC	-	
AC4	NC	-		PL53A	6	
AD4	NC	-		PL53B	6	
AE3	NC	-		PL56A	6	
AF3	NC	-		PL56B	6	
AF7	NC	-		PB7A	5	
AF6	NC	-		PB7B	5	
AH4	NC	-		PB8A	5	
AG5	NC	-		PB8B	5	
AF8	NC	-		PB9A	5	
AG8	NC	-		PB9B	5	
AG7	NC	-		NC	-	
AG10	NC	-		NC	-	
AF12	NC	-		NC	-	
AH7	NC	-		PB15A	5	
AE13	NC	-		PB15D	5	
AG13	NC	-		PB23C	5	
AH8	NC	-		PB15B	5	
AJ5	NC	-		PB17A	5	
AJ6	NC	-		PB17B	5	
AF15	NC	-		PB21D	5	
AJ7	NC	-		PB19A	5	
AJ8	NC	-		PB19B	5	
AE12	NC	-		PB15C	5	
AF16	NC	-		PB38D	4	
AF19	NC	-		PB49D	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	**VCCIO Bank**	**Dual Function**
W30	PL69B	6	
W27	PL69C	6	VREF1_6
Y27	PL69D	6	
T33	PL70A	6	
U33	PL70B	6	
V25	PL70C	6	
W25	PL70D	6	
U34	PL71A	6	
V34	PL71B	6	
V26	PL71C	6	
W26	PL71D	6	
V33	PL74A	6	
W33	PL74B	6	
V24	PL74C	6	
W24	PL74D	6	
W31	PL77A	6	
Y31	PL77B	6	
Y29	PL77C	6	
AA29	PL77D	6	
Y33	PL79A	6	
AA33	PL79B	6	
Y28	PL79C	6	
AA28	PL79D	6	
AB32	PL90A	6	
AC32	PL90B	6	
AA26	PL90C	6	
AA27	PL90D	6	DIFFR_6
AB31	PL91A	6	
AC31	PL91B	6	
Y24	PL91C	6	
AA24	PL91D	6	
AE34	PL92A	6	
AF34	PL92B	6	
AB30	PL92C	6	
AC30	PL92D	6	
AD33	PL94A	6	
AE33	PL94B	6	
AD30	PL94C	6	
AE30	PL94D	6	
AE32	PL96A	6	
AF32	PL96B	6	
AA25	PL96C	6	
AB25	PL96D	6	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

	LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function
W7	GND	-	
AA14	VCC	-	
AA16	VCC	-	
AA17	VCC	-	
AA18	VCC	-	
AA19	VCC	-	
AA21	VCC	-	
AB13	VCC	-	
AB22	VCC	-	
N13	VCC	-	
N22	VCC	-	
P14	VCC	-	
P16	VCC	-	
P17	VCC	-	
P18	VCC	-	
P19	VCC	-	
P21	VCC	-	
R15	VCC	-	
R17	VCC	-	
R18	VCC	-	
R20	VCC	-	
T14	VCC	-	
T16	VCC	-	
T19	VCC	-	
T21	VCC	-	
U14	VCC	-	
U15	VCC	-	
U17	VCC	-	
U18	VCC	-	
U20	VCC	-	
U21	VCC	-	
V14	VCC	-	
V15	VCC	-	
V17	VCC	-	
V18	VCC	-	
V20	VCC	-	
V21	VCC	-	
W14	VCC	-	
W16	VCC	-	
W19	VCC	-	
W21	VCC	-	
Y15	VCC	-	
Y17	VCC	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP8	PB117D	4		PB131D	4	
AY3	PB119A	4		PB133A	4	
AW3	PB119B	4		PB133B	4	
AR6	PB119C	4		PB133C	4	
AR5	PB119D	4		PB133D	4	
AU5	PB120A	4		PB134A	4	
AV5	PB120B	4		PB134B	4	
AL12	PB120C	4		PB134C	4	
AL11	PB120D	4		PB134D	4	
AV3	PB121A	4		PB135A	4	
AV4	PB121B	4		PB135B	4	
AN9	PB121C	4		PB135C	4	
AN8	PB121D	4		PB135D	4	
AW1	PB123A	4		PB138A	4	
AY1	PB123B	4		PB138B	4	
AK14	PB123C	4	VREF1_4	PB138C	4	VREF1_4
AK13	PB123D	4		PB138D	4	
AV2	PB124A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB139A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AW2	PB124B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB139B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AM10	PB124C	4		PB139C	4	
AM9	PB124D	4		PB139D	4	
AV1	PB125A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB141A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AU1	PB125B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB141B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AL10	PB125C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB141C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AL9	PB125D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB141D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AT3	PROBE_VCC	-		PROBE_VCC	-	
AU2	PROBE_GND	-		PROBE_GND	-	
AP7	PR95D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR117D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AN7	PR95C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR117C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AR3	PR95B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR117B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AR4	PR95A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR117A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AP6	PR94D	3		PR116D	3	
AN6	PR94C	3		PR116C	3	
AT2	PR94B	3		PR116B	3	
AR2	PR94A	3		PR116A	3	
AM6	PR93D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR115D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AL6	PR93C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR115C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AP5	PR93B	3		PR115B	3	
AN5	PR93A	3		PR115A	3	
AL8	PR91D	3		PR112D	3	
AK8	PR91C	3		PR112C	3	
AP2	PR91B	3		PR112B	3	
AN2	PR91A	3		PR112A	3	
AJ12	PR90D	3		PR109D	3	
AH12	PR90C	3		PR109C	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB6	PR57D	3		PR71D	3	
AA6	PR57C	3		PR71C	3	
Y2	PR57B	3		PR71B	3	
W2	PR57A	3		PR71A	3	
AB7	PR56D	3		PR70D	3	
AA7	PR56C	3		PR70C	3	
Y3	PR56B	3		PR70B	3	
W3	PR56A	3		PR70A	3	
AC11	PR55D	3		PR69D	3	
AB11	PR55C	3	VREF1_3	PR69C	3	VREF1_3
Y4	PR55B	3		PR69B	3	
W4	PR55A	3		PR69A	3	
AB8	PR52D	3	PCLKC3_2	PR66D	3	PCLKC3_2
AA8	PR52C	3	PCLKT3_2	PR66C	3	PCLKT3_2
Y5	PR52B	3		PR66B	3	
W5	PR52A	3		PR66A	3	
AC12	PR51D	3	PCLKC3_3	PR65D	3	PCLKC3_3
AB12	PR51C	3	PCLKT3_3	PR65C	3	PCLKT3_3
V1	PR51B	3		PR65B	3	
U1	PR51A	3		PR65A	3	
W7	PR50D	3	PCLKC3_1	PR64D	3	PCLKC3_1
V7	PR50C	3	PCLKT3_1	PR64C	3	PCLKT3_1
V2	PR50B	3	PCLKC3_0	PR64B	3	PCLKC3_0
U2	PR50A	3	PCLKT3_0	PR64A	3	PCLKT3_0
AB9	PR48D	2	PCLKC2_2	PR62D	2	PCLKC2_2
AA9	PR48C	2	PCLKT2_2	PR62C	2	PCLKT2_2
T1	PR48B	2	PCLKC2_0	PR62B	2	PCLKC2_0
R1	PR48A	2	PCLKT2_0	PR62A	2	PCLKT2_0
AB10	PR47D	2	PCLKC2_3	PR61D	2	PCLKC2_3
AA10	PR47C	2	PCLKT2_3	PR61C	2	PCLKT2_3
U3	PR47B	2	PCLKC2_1	PR61B	2	PCLKC2_1
T3	PR47A	2	PCLKT2_1	PR61A	2	PCLKT2_1
Y9	PR46D	2		PR60D	2	
W9	PR46C	2		PR60C	2	
V5	PR46B	2		PR60B	2	
U5	PR46A	2		PR60A	2	
AA11	PR43D	2		PR57D	2	
Y11	PR43C	2		PR57C	2	
Y6	PR43B	2		PR57B	2	
W6	PR43A	2		PR57A	2	
Y10	PR42D	2		PR56D	2	
W10	PR42C	2		PR56C	2	
T2	PR42B	2		PR56B	2	
R2	PR42A	2		PR56A	2	
W8	PR41D	2		PR55D	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D32	C_HDINP1_L	-	PCS 362 CH 1 IN P	C_HDINP1_L	-	PCS 362 CH 1 IN P
E32	C_HDINN1_L	-	PCS 362 CH 1 IN N	C_HDINN1_L	-	PCS 362 CH 1 IN N
B31	C_HDOUTP1_L	-	PCS 362 CH 1 OUT P	C_HDOUTP1_L	-	PCS 362 CH 1 OUT P
K32	VCC12	-		VCC12	-	
A31	C_HDOUTN1_L	-	PCS 362 CH 1 OUT N	C_HDOUTN1_L	-	PCS 362 CH 1 OUT N
L32	C_VDDOB1_L	-		C_VDDOB1_L	-	
A32	C_HDOUTN0_L	-	PCS 362 CH 0 OUT N	C_HDOUTN0_L	-	PCS 362 CH 0 OUT N
M31	C_VDDOB0_L	-		C_VDDOB0_L	-	
B32	C_HDOUTP0_L	-	PCS 362 CH 0 OUT P	C_HDOUTP0_L	-	PCS 362 CH 0 OUT P
H37	VCC12	-		VCC12	-	
E33	C_HDINN0_L	-	PCS 362 CH 0 IN N	C_HDINN0_L	-	PCS 362 CH 0 IN N
D33	C_HDINP0_L	-	PCS 362 CH 0 IN P	C_HDINP0_L	-	PCS 362 CH 0 IN P
G31	C_VDDIB0_L	-		C_VDDIB0_L	-	
J29	VCC12	-		VCC12	-	
L29	B_REFCLKP_L	-		B_REFCLKP_L	-	
M29	B_REFCLKN_L	-		B_REFCLKN_L	-	
J31	VCC12	-		VCC12	-	
H31	B_VDDIB3_L	-		B_VDDIB3_L	-	
J30	VCC12	-		VCC12	-	
D34	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
E34	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
B33	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
H38	VCC12	-		VCC12	-	
A33	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
C38	B_VDDOB3_L	-		B_VDDOB3_L	-	
A34	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
L31	B_VDDOB2_L	-		B_VDDOB2_L	-	
B34	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G38	VCC12	-		VCC12	-	
E35	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
D35	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H32	B_VDDIB2_L	-		B_VDDIB2_L	-	
K29	VCC12	-		VCC12	-	
K30	B_VDDIB1_L	-		B_VDDIB1_L	-	
F33	VCC12	-		VCC12	-	
D36	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
E36	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
B35	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L34	VCC12	-		VCC12	-	
A35	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
K35	B_VDDOB1_L	-		B_VDDOB1_L	-	
A36	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
G39	B_VDDOB0_L	-		B_VDDOB0_L	-	
B36	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
J35	VCC12	-		VCC12	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-7FF1020C[1]	-7	Organic fcBGA	1020	COM	40.4
LFSC3GA40E-6FF1020C[1]	-6	Organic fcBGA	1020	COM	40.4
LFSC3GA40E-5FF1020C[1]	-5	Organic fcBGA	1020	COM	40.4
LFSC3GA40E-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-7FC1152C[2]	-7	Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-6FC1152C[2]	-6	Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-5FC1152C[2]	-5	Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-7FF1152C	-7	Organic fcBGA	1152	COM	40.4
LFSC3GA40E-6FF1152C	-6	Organic fcBGA	1152	COM	40.4
LFSC3GA40E-5FF1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-7FF1020C[1]	-7	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-6FF1020C[1]	-6	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-5FF1020C[1]	-5	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-7FC1152C[2]	-7	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FC1152C[2]	-6	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FC1152C[2]	-5	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-7FF1152C	-7	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FF1152C	-6	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FF1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-7FCN1152C[2]	-7	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-6FCN1152C[2]	-6	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-5FCN1152C[2]	-5	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	40.4
LFSC3GA40E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	40.4
LFSC3GA40E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-7FFN1020C[1]	-7	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-6FFN1020C[1]	-6	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-5FFN1020C[1]	-5	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-7FFAN1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-6FFAN1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-5FFAN1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-7FCN1152C[2]	-7	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FCN1152C[2]	-6	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FCN1152C[2]	-5	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-7FFN1152C	-7	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FFN1152C	-6	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FFN1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C[1]	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C[1]	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C[1]	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C[1]	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Date	Version	Section	Change Summary
December 2011	02.4	DC and Switching Characteristics	Updated JTAG Port Timing Specifications table.