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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

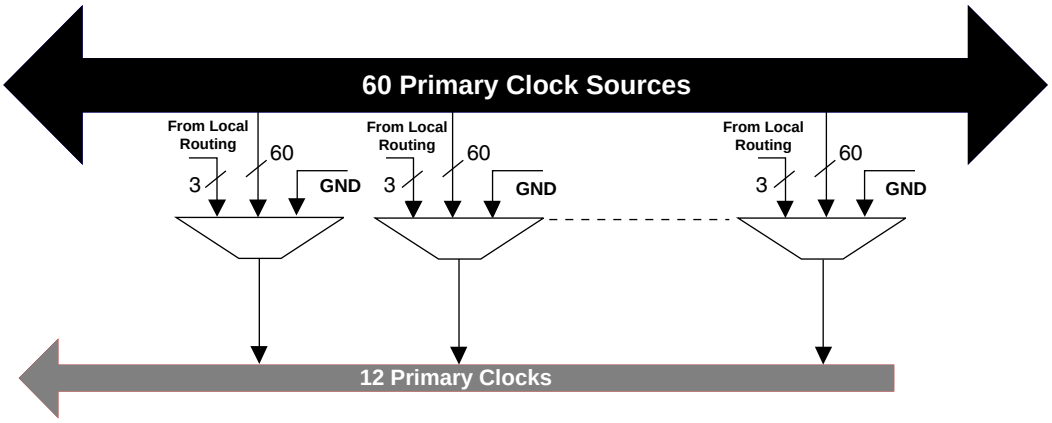
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 10000 |
| Number of Logic Elements/Cells | 40000 |
| Total RAM Bits | 4075520 |
| Number of I/O | 604 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga40e-6fcn1152c |

*Figure 2-6. Per Quadrant Clock Selection*




Note: GND is available to switch off the network.

## Secondary Clocks

In addition to the primary clock network and edge clocks the LatticeSC devices also contain a secondary clock network. Built of X6 style routing elements this secondary clock network is ideal for routing slower speed clock and control signals throughout the device preserving high-speed clock networks for the most timing critical signals.

## Edge Clocks

LatticeSC devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per bank for the top and bottom of the device. The left and right sides have eight edge clocks per side for both banks located on that side. Figure 2-7 shows the arrangement of edge clocks.

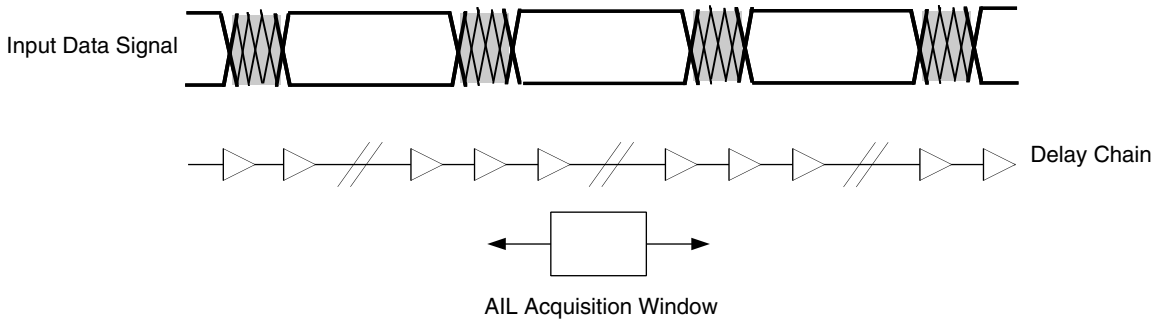
Edge clock resources can be driven from a variety of sources. Edge clock resources can be driven from:

- Edge clock PIOs in the same bank
- Primary clock PIOs in the same bank
- Routing
- Adjacent PLLs and DLLs
- ELSR output from the clock divider

**Adaptive Input Logic (AIL) Overview**

The Adaptive Input Logic (AIL) provides the ability of the input logic to dynamically find a solution by monitoring multiple samples of the input data. The input data signal from the input buffer is run through a delay chain. Data, transitions, jitter, noise are all contained inside of the delay chain. The AIL will then search the delay chain for a clean sampling point for data. Once found the AIL will monitor and walk with the data dynamically. This novel approach of using a delay chain to create multiple copies of the data provides a lower power solution than oversampling data with a higher speed clock. Figure 2-19 provides a high level view of the AIL methodology.

***Figure 2-19. LatticeSC AIL Delay of Input Data Waveform***




The AIL slides the acquisition window through the delay chain searching for stable data based solely on data transitions. A specific training pattern is not required to perform this bit alignment, simply data transitions. The size of the acquisition window is user-selectable allowing the AIL to operate over the full range of the PURESPEED I/O range. Based on dynamic user control the AIL can either continuously adjust the window location based on data edge detection or it can be locked to a specific delay.

The AIL operates on single data and double data rate interfaces and is available on most FPGA input pins on the LatticeSC device and all buffer types. The AIL block is low power using only 0.003 mW/MHz typical (6 mW @ 2 Gbps) for PRBS $2^7$ data. Multiple AIL inputs can be used to create a bus with a FPGA circuit to realign the bus to a common clock cycle. The FPGA circuit to realign the bus is required and is provided by Lattice as a reference design.

For more information on the LatticeSC AIL please refer to TN1158 LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide.

**Input DDR/Shift Block**

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer to the low-speed clock domain. It functions as a gearbox allowing high-speed incoming data to be passed into the FPGA fabric. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. The PIOs A and C on the left, right and bottom of the device also contain an optional Adaptive Input Logic (AIL) element. This logic automatically aligns incoming data with the clock allowing for easy design of high-speed interfaces. Figure 2-21 shows a simplified block diagram of the shift register block. The shift block in conjunction with the update and clock divider blocks automatically handles the hand off between the low-speed and high-speed clock domains.

3. **Bottom Side (Banks 4 and 5)**
   These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but true HLVDS and RSDS differential drivers are not available. Adaptive input logic is available on PIOs A or C.

Table 2-8 lists the standards supported by each side.

***Table 2-8. I/O Standards Supported by Different Banks***

| Description | Top Side Banks 1 | Right Side Banks 2-3 | Bottom Side Banks 4-5 | Left Side Banks 6-7 |
|---|---|---|---|---|
| I/O Buffer Type | Single-ended, Differential Receiver | Single-ended, Differential Receiver and Driver | Single-ended, Differential Receiver | Single-ended, Differential Receiver and Driver |
| Output Standards Supported | LVTTL<br>LVCMOS33<br>LVCMOS25<br>LVCMOS18<br>LVCMOS15<br>LVCMOS12<br>SSTL18_I, II<br>SSTL25_ I, II<br>SSTL33_ I, II<br>HSTL15_I, II, III[1], IV[1]<br>HSTL18_I, II,III[1], IV[1]<br>SSTL18D_I, II<br>SSTL25D_I, II<br>SSTL33D_I, II<br>HSTL15D_I, II<br>HSTL18D_I, II<br>PCI33<br>PCIX15<br>PCIX33<br>AGP1X33<br>AGP2X33<br>MLVDS/BLVDS<br>GTL[2], GTL+[2] | LVCMOS25<br>LVCMOS18<br>LVCMOS15<br>LVCMOS12<br>SSTL18_I, II<br>SSTL25_ I, II<br>HSTL15_I,III<br>HSTL18_I,II,III<br>PCIX15<br>SSTL18D_I, II<br>SSTL25D_I, II<br>HSTL15D_I, II<br>HSTL18D_I, II<br>LVDS/RSDS<br>Mini-LVDS<br>MLVDS/BLVDS<br>GTL[2], GTL+[2] | LVTTL<br>LVCMOS33<br>LVCMOS25<br>LVCMOS18<br>LVCMOS15<br>LVCMOS12<br>SSTL18_I, II<br>SSTL25_ I, II<br>SSTL33_ I, II<br>HSTL15_I, II, III[1], IV[1]<br>HSTL18_I, II,III[1], IV[1]<br>SSTL18D_I, II<br>SSTL25D_I, II<br>SSTL33D_I, II<br>HSTL15D_I, II<br>HSTL18D_I, II<br>PCI33<br>PCIX15<br>PCIX33<br>AGP1X33<br>AGP2X33<br>MLVDS/BLVDS<br>GTL[2], GTL+[2] | LVCMOS25<br>LVCMOS18<br>LVCMOS15<br>LVCMOS12<br>SSTL18_I, II<br>SSTL25_ I, II<br>HSTL15_I,III<br>HSTL18_I,II,III<br>PCIX15<br>SSTL18D_I, II<br>SSTL25D_I, II<br>HSTL15D_I, II<br>HSTL18D_I, II<br>LVDS/RSDS<br>Mini-LVDS<br>MLVDS/BLVDS<br>GTL[2], GTL+[2] |
| Input Standards Supported | Single-ended, Differential | Single-ended, Differential | Single-ended, Differential | Single-ended, Differential |
| Clock Inputs | Single-ended, Differential | Single-ended, Differential | Single-ended, Differential | Single-ended, Differential |
| Differential Output Support via Emulation | LVDS/MLVDS/BLVDS/ LVPECL | MLVDS/BLVDS/ LVPECL | LVDS/MLVDS/BLVDS/ LVPECL | MLVDS/BLVDS/ LVPECL |
| AIL Support | No | Yes | Yes | Yes |

1. Input only.
2. Input only. Outputs supported by bussing multiple outputs together.

## Supported Standards

The LatticeSC PURESPEED I/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 12, 15, 18, 25 and 33 standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, termination resistance, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL, HSTL, GTL (input only), GTL+ (input only), PCI33, PCIX33, PCIX15, AGP-1X33 and AGP-2X33. Differential standards supported include LVDS, RSDS, BLVDS, MLVDS, LVPECL, differential SSTL and differential HSTL. Tables 12 and 13 show the I/O standards (together with their supply and reference voltages) supported by the LatticeSC devices. The tables also provide the available internal termination schemes. For further information on utilizing the PURESPEED I/O buffer to support a variety of standards please see details of additional technical documentation at the end of this data sheet.

# LatticeSC/M Family Data Sheet DC and Switching Characteristics

**December 2011** **Data Sheet DS1004**

## Absolute Maximum Ratings

Supply Voltage $V_{CC}$, $V_{CC12}$, $V_{DDIB}$, $V_{DDOB}$ . . . . . -0.5 to 1.6V

Supply Voltage $V_{CCAUX}$, $V_{DDAX25}$, $V_{TT}$ . . . . . -0.5 to 2.75V

Supply Voltage $V_{CCJ}$ . . . . . -0.5 to 3.6V

Supply Voltage $V_{CCIO}$ (Banks 1, 4, 5) . . . . . -0.5 to 3.6V

Supply Voltage $V_{CCIO}$ (Banks 2, 3, 6, 7) . . . . . -0.5 to 2.75V

Input or I/O Tristate Voltage Applied (Banks 1, 4, 5) . . . . . -0.5 to 3.6V

Input or I/O Tristate Voltage Applied (Banks 2, 3, 6, 7) . . . . . -0.5 to 2.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temperature Under Bias (Tj) . . . . . +125°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot and overshoot of -2V to (VIHMAX +2) volts is permitted for a duration of <20ns.

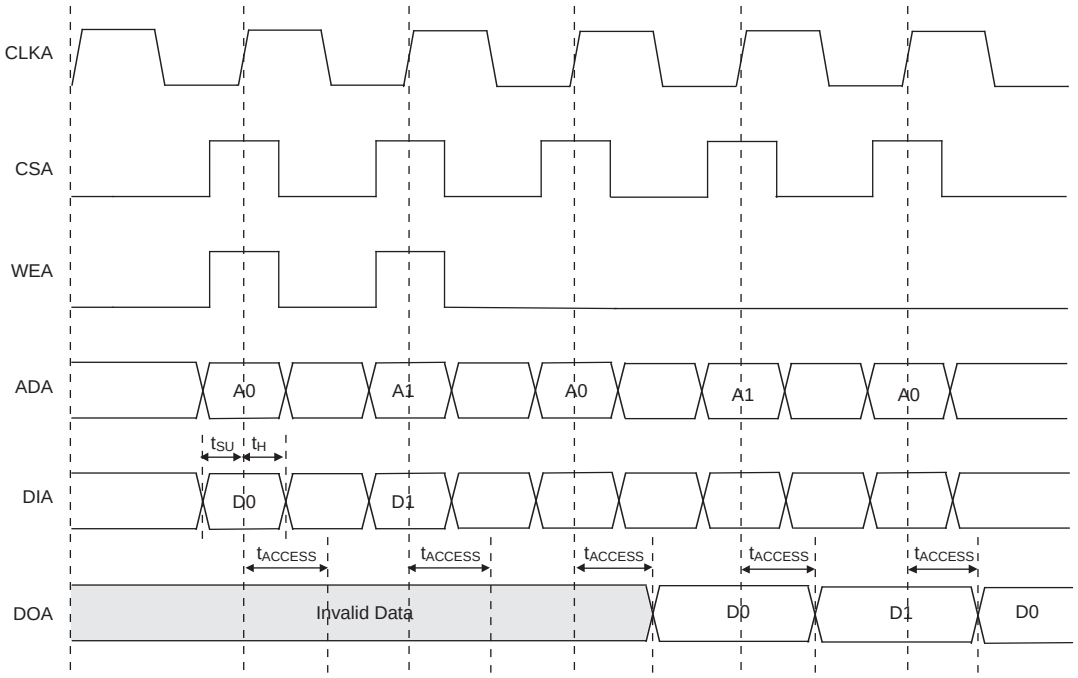
## Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$[5] | Core Supply Voltage (Nominal 1.2V Operation) | 0.95 | 1.26 | V |
| $V_{CCAUX}$[6] | Programmable I/O Auxiliary Supply Voltage | 2.375 | 2.625 | V |
| $V_{CCIO}$[1, 2, 5, 6] | Programmable I/O Driver Supply Voltage (Banks 1, 4, 5) | 1.14 | 3.45 | V |
| $V_{CCIO}$[1, 2, 5, 6] | Programmable I/O Driver Supply Voltage (Banks 2, 3, 6, 7) | 1.14 | 2.625 | V |
| $V_{CC12}$[4, 5] | Internal 1.2V Power Supply Voltage for Configuration Logic and FPGA PLL, SERDES PLL Power Supply Voltage and SERDES Analog Supply Voltage | 1.14 | 1.26 | V |
| $V_{DDIB}$ | SERDES Input Buffer Supply Voltage | 1.14 | 1.575 | V |
| $V_{DDOB}$ | SERDES Output Buffer Supply Voltage | 1.14 | 1.575 | V |
| $V_{DDAX25}$ | SERDES Termination Auxiliary Supply Voltage | 2.375 | 2.625 | V |
| $V_{CCJ}$[1, 5] | Supply Voltage for IEEE 1149.1 Test Access Port | 1.71 | 3.45 | V |
| $V_{TT}$[2, 3] | Programmable I/O Termination Power Supply | 0.5 | $V_{CCAUX}$ - 0.5 | V |
| $t_{JCOM}$ | Junction Temperature, Commercial Operation | 0 | +85 | C |
| $t_{JIND}$ | Junction Temperature, Industrial Operation | -40 | 105 | C |

1. If $V_{CCIO}$ or $V_{CCJ}$ is set to 2.5V, they must be connected to the same power supply as $V_{CCAUX}$.
2. See recommended voltages by I/O standard in subsequent table.
3. When $V_{TT}$ termination is not required, or used to provide the common mode termination voltage ($V_{CMT}$), these pins can be left unconnected on the device.
4. $V_{CC12}$ cannot be lower than $V_{CC}$ at any time. For 1.2V operation, it is recommended that the $V_{CC}$ and $V_{CC12}$ supplies be tied together with proper noise decoupling between the digital VCC and analog VCC12 supplies.
5. $V_{CC}$, $V_{CCIO}$ (all banks), $V_{CC12}$ and $V_{CCJ}$ must reach their minimum values before configuration will proceed.
6. If $V_{CCIO}$ for a bank is nominally 1.2V/1.5V/1.8V, then $V_{CCAUX}$ must always be higher than $V_{CCIO}$ during power up.

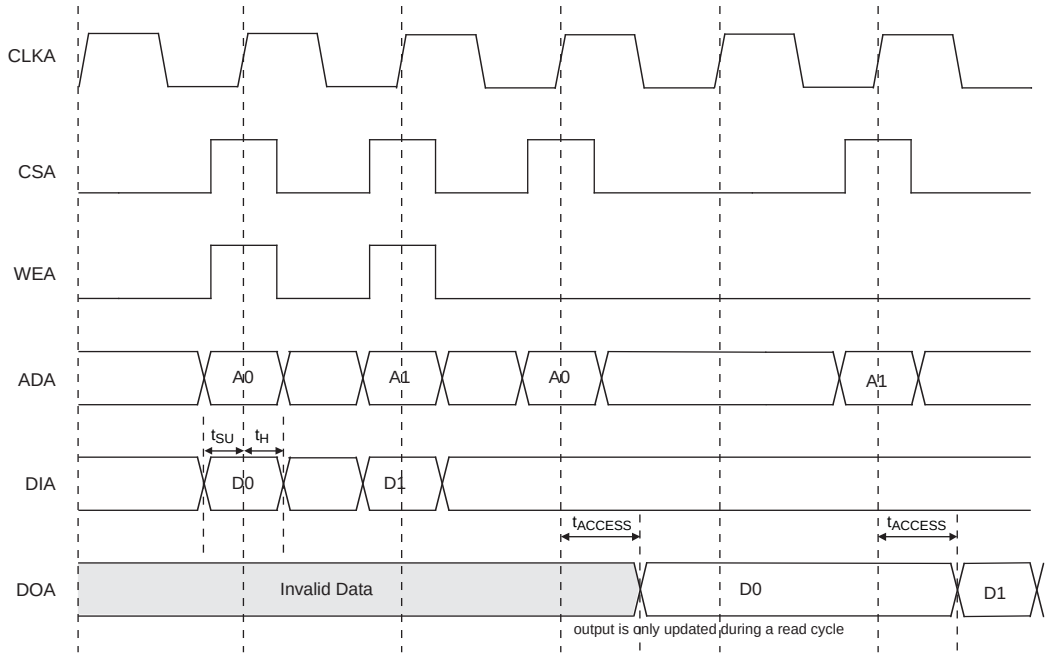
# EBR Memory Timing Diagrams

***Figure 3-6. Read Mode***




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

***Figure 3-7. Read Mode with Input Registers Only***



# LatticeSC/M sysCONFIG Port Timing

**Over Recommended Operating Conditions**

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| **General Configuration Timing** | | | | |
| $t_{SMODE}$ | M[3:0] Setup Time to INITN High | 0 | — | ns |
| $t_{HMODE}$ | M[3:0] Hold Time from INITN High | 600 | — | ns |
| $t_{RW}$ | RESETN Pulse Width Low to Start Reconfiguration (1.2 V) | 50 (or 100 at 0.95V) | — | ns |
| $t_{PGW}$ | PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V) | 50 (or 100 at 0.95V) | — | ns |
| $f_{ESB\_CLK\_FRQ}$ | System Bus ESB_CLK Frequency (No Wait States) | — | 133 | MHz |
| **sysCONFIG Master Parallel Configuration Mode** | | | | |
| $t_{SMB}$ | D[7:0] Setup Time to RCLK High | 6 | — | ns |
| $t_{HMB}$ | D[7:0] Hold Time to RCLK High | 0 | — | ns |
| $t_{CLMB}$ | RCLK Low Time (Non-compressed Bitstreams) | 0.5 | 0.5 | CCLK periods |
| | RCLK Low Time (Compressed Bitstreams) | 0.5 | 7.5 | CCLK periods |
| $t_{CHMB}$ | RCLK High Time | 0.5 | 0.5 | CCLK periods |
| **sysCONFIG SPI Port** | | | | |
| $t_{CFGX}$ | INITN High to CSCK Low | — | 80 | ns |
| $t_{CSSPI}$ | INITN High to CSSPIN Low | 0 | 2 | µs |
| $t_{SCK}$ | CSCK Low before CSSPIN Low | 0 | — | ns |
| $t_{SOCDO}$ | CSCK Low to Output Valid | — | 15 | ns |
| $t_{CSPID}$ | CSSPIN Low to CSCK high Setup Time | — | 15 | ns |
| $f_{MAXSPI}$ | Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0) | — | 50 | MHz |
| $t_{SUSPI}$ | SOSPI/D0 Data Setup Time Before CSCK | 7 | — | ns |
| $t_{HSPI}$ | SOSPI/D0 Data Hold Time After CSCK | 2 | — | ns |
| | Master Clock Frequency | Selected value - 30% | Selected value + 30% | MHz |
| | Duty Cycle | 40 | 60 | % |
| **sysCONFIG Master Serial Configuration Mode** | | | | |
| $t_{SMS}$ | DIN Setup Time | 4.4 | — | ns |
| $t_{HMS}$ | DIN Hold Time | 0 | — | ns |
| $f_{CMS}$ | CCLK Frequency (No Divider) | 90 | 190 | MHz |
| $f_{C\_DIV}$ | CCLK Frequency (Div 128) | 0.70 | 1.48 | MHz |
| $t_{D}$ | CCLK to DOUT Delay | — | 7.5 | ns |
| **sysCONFIG Master Parallel Configuration Mode** | | | | |
| $t_{AVMP}$ | RCLK to Address Valid | — | 10 | ns |
| $t_{SMP}$ | D[7:0] Setup Time to RCLK High | 6 | — | ns |
| $t_{HMP}$ | D[7:0] Hold Time to RCLK High | 0 | — | ns |
| $t_{CLMP}$ | RCLK Low Time (Non-compressed Bitstream) | 7.5 | 7.5 | CCLK periods |
| | RCLK Low Time (Compressed Bitstream) | 0.5 | 63.5 | |
| $t_{CHMP}$ | RCLK High Time | 0.5 | 0.5 | CCLK periods |
| $t_{DMP}$ | CCLK to DOUT | — | 7.5 | ns |

## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| D[n:0] | I/O | In parallel configuration modes, D[7:0] receives configuration data, and each pin is pull-up enabled. For slave serial mode, D0 is the data input.<br><br>D[7:3] is the output internal status for peripheral mode when RDN is low.<br><br>D[7:0] is also the first byte of MPI data pins.<br><br>In MPI configuration mode, MPI selectable data bus width from 8 and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction. |
| DP[m:0] | I/O | MPI selectable parity data bus width from 1, 2, and 3-bit DP[0] for D[7:0], DP[1] for D[15:8], and DP[2] for D[23:16]. |
| BUSYN/RCLK/SCK | O | During configuration in peripheral mode, high on BUSYN indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D[7] in asynchronous peripheral mode.<br><br>During configuration in slave parallel mode, low on BUSYN inhibits the external host from sending new data. The output is used by slave parallel and master serial modes only for decompression.<br><br>During configuration in master parallel and master byte modes, RCLK is a read clock output signal to an external memory. The RCLK frequency is the same as CCLK when used with uncompressed bitstreams. RCLK will be 1/8 the frequency of CCLK when the bitstream is compressed.<br><br>During configuration in SPI modes, SCK is generated by the device and connected to the CLK input of the FLASH memory. |
| **MPI Interface (Dedicated pin)** | | |
| MPI_IRQ_N | O | MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins. |
| **MPI Interface (User I/O if MPI is not used.)** | | |
| MPI_CS0N MPI_CS1 | I | MPI chip select pins, active low on MPI_CS0N while active high on MPI_CS1. Both have to be active during the whole transfer data phase. During transfer address phase, both can be inactive so that the decoding for them from address can be slow. If they are active during address phase, one cycle can be saved for sync read. |
| MPI_CLK | I | This is the PowerPC bus clock. It can be a source of the clock for embedded system bus. If MPI_CLK is used as system bus clock, MPI will be set into sync mode by default. All of the operation on PowerPC side of MPI are synchronized to the rising edge of this clock. |
| MPI_TSIZ[1:0] | I | Driven by a bus master to indicate the data transfer size for the transaction. 01 for byte, 10 for half-word, and 00 for word. |
| MPI_WR_N | I | Driven high indicates that a read access is in progress. Driven low indicates that a write access is in process. |
| MPI_BURST | I | Driven active low indicates that a burst transfer is in progress. Driven high indicates that the current transfer is not a burst. |
| MPI_BDIP | I | Active low “Burst Data in Process” is driven by a PowerPC processor. Asserted indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase. |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| N3 | PL27A | 6 | | PL30A | 6 | |
| P3 | PL27B | 6 | | PL30B | 6 | |
| P4 | PL27C | 6 | PCLKT6_3 | PL30C | 6 | PCLKT6_3 |
| P2 | PL28A | 6 | | PL31A | 6 | |
| R2 | PL28B | 6 | | PL31B | 6 | |
| T3 | PL28C | 6 | PCLKT6_2 | PL31C | 6 | PCLKT6_2 |
| R3 | PL28D | 6 | PCLKC6_2 | PL31D | 6 | PCLKC6_2 |
| P1 | PL31A | 6 | | PL34A | 6 | |
| R1 | PL31B | 6 | | PL34B | 6 | |
| R5 | PL31C | 6 | VREF1_6 | PL34C | 6 | VREF1_6 |
| R4 | PL31D | 6 | | PL34D | 6 | |
| T2 | PL32A | 6 | | PL35A | 6 | |
| U2 | PL32B | 6 | | PL35B | 6 | |
| T1 | PL33A | 6 | | PL38A | 6 | |
| U1 | PL33B | 6 | | PL38B | 6 | |
| V1 | PL35A | 6 | | PL42A | 6 | |
| W1 | PL35B | 6 | | PL42B | 6 | |
| V6 | PL35D | 6 | DIFFR_6 | PL42D | 6 | DIFFR_6 |
| V2 | PL36A | 6 | | PL43A | 6 | |
| W2 | PL36B | 6 | | PL43B | 6 | |
| Y1 | PL37A | 6 | | PL44A | 6 | |
| AA1 | PL37B | 6 | | PL44B | 6 | |
| AB1 | PL39A | 6 | | PL48A | 6 | |
| AC1 | PL39B | 6 | | PL48B | 6 | |
| Y5 | PL40A | 6 | | PL49A | 6 | |
| Y6 | PL40B | 6 | | PL49B | 6 | |
| AD2 | PL41A | 6 | | PL51A | 6 | |
| AE2 | PL41B | 6 | | PL51B | 6 | |
| AB5 | PL41D | 6 | VREF2_6 | PL51D | 6 | VREF2_6 |
| AC3 | PL43A | 6 | | PL52A | 6 | |
| AD3 | PL43B | 6 | | PL52B | 6 | |
| AF1 | PL44A | 6 | | PL55A | 6 | |
| AG1 | PL44B | 6 | | PL55B | 6 | |
| AB6 | PL44C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F | PL55C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F |
| AC5 | PL44D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F | PL55D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F |
| AF2 | PL45A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E | PL57A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E |
| AG2 | PL45B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E | PL57B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E |
| AC6 | PL45C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A | PL57C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A |
| AC7 | PL45D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A | PL57D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A |
| AE4 | XRES | - | | XRES | - | |
| AG4 | VCC12 | - | | VCC12 | - | |
| AD5 | TEMP | 6 | | TEMP | 6 | |
| AF5 | VCC12 | - | | VCC12 | - | |
| AH1 | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B |
| AJ1 | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AH20 | NC | - | | PB51D | 4 | |
| AK27 | NC | - | | NC | - | |
| AJ24 | NC | - | | NC | - | |
| AF17 | NC | - | | PB42C | 4 | |
| AH27 | NC | - | | PB61B | 4 | |
| AD23 | NC | - | | PB57A | 4 | |
| AE23 | NC | - | | PB57B | 4 | |
| AH24 | NC | - | | PB59A | 4 | |
| AH25 | NC | - | | PB59B | 4 | |
| AH26 | NC | - | | PB61A | 4 | |
| AF24 | NC | - | | PB63A | 4 | |
| AG24 | NC | - | | PB63B | 4 | |
| AG25 | NC | - | | PB64A | 4 | |
| AF25 | NC | - | | PB64B | 4 | |
| AG26 | NC | - | | PB65A | 4 | |
| AF27 | NC | - | | PB65B | 4 | |
| AD28 | NC | - | | PR56B | 3 | |
| AC27 | NC | - | | PR56A | 3 | |
| AE29 | NC | - | | PR53B | 3 | |
| AD29 | NC | - | | PR53A | 3 | |
| AB30 | NC | - | | NC | - | |
| AA28 | NC | - | | NC | - | |
| Y27 | NC | - | | PR47C | 3 | |
| W27 | NC | - | | PR47D | 3 | |
| V30 | NC | - | | PR47A | 3 | |
| W30 | NC | - | | PR47B | 3 | |
| W26 | NC | - | | PR43D | 3 | |
| V26 | NC | - | | PR43C | 3 | |
| U25 | NC | - | | PR42C | 3 | |
| T27 | NC | - | | PR40B | 3 | |
| R27 | NC | - | | PR40A | 3 | |
| V27 | NC | - | | PR39B | 3 | |
| U27 | NC | - | | PR39A | 3 | |
| U29 | NC | - | | PR36B | 3 | |
| T29 | NC | - | | PR36A | 3 | |
| T24 | NC | - | | PR35C | 3 | |
| Y25 | NC | - | | PR48C | 3 | |
| P24 | NC | - | | NC | - | |
| K28 | NC | - | | NC | - | |
| P23 | NC | - | | NC | - | |
| L28 | NC | - | | NC | - | |
| M27 | NC | - | | PR21B | 2 | |
| L27 | NC | - | | PR21A | 2 | |
| H27 | NC | - | | PR20B | 2 | |
| G27 | NC | - | | PR20A | 2 | |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| U18 | GND | - | | GND | - | |
| U19 | GND | - | | GND | - | |
| U20 | GND | - | | GND | - | |
| V11 | GND | - | | GND | - | |
| V12 | GND | - | | GND | - | |
| V13 | GND | - | | GND | - | |
| V14 | GND | - | | GND | - | |
| V15 | GND | - | | GND | - | |
| V16 | GND | - | | GND | - | |
| V17 | GND | - | | GND | - | |
| V18 | GND | - | | GND | - | |
| V19 | GND | - | | GND | - | |
| V20 | GND | - | | GND | - | |
| W11 | GND | - | | GND | - | |
| W12 | GND | - | | GND | - | |
| W13 | GND | - | | GND | - | |
| W14 | GND | - | | GND | - | |
| W15 | GND | - | | GND | - | |
| W16 | GND | - | | GND | - | |
| W17 | GND | - | | GND | - | |
| W18 | GND | - | | GND | - | |
| W19 | GND | - | | GND | - | |
| W20 | GND | - | | GND | - | |
| Y11 | GND | - | | GND | - | |
| Y12 | GND | - | | GND | - | |
| Y13 | GND | - | | GND | - | |
| Y14 | GND | - | | GND | - | |
| Y15 | GND | - | | GND | - | |
| Y16 | GND | - | | GND | - | |
| Y17 | GND | - | | GND | - | |
| Y18 | GND | - | | GND | - | |
| Y19 | GND | - | | GND | - | |
| Y20 | GND | - | | GND | - | |
| H2 | VCCIO7 | - | | VCCIO7 | - | |
| N4 | VCCIO7 | - | | VCCIO7 | - | |
| N6 | VCCIO7 | - | | VCCIO7 | - | |
| J2 | VCCIO7 | - | | VCCIO7 | - | |
| L2 | VCCIO7 | - | | VCCIO7 | - | |
| H4 | VCCIO7 | - | | VCCIO7 | - | |
| AB2 | VCCIO6 | - | | VCCIO6 | - | |
| AD1 | VCCIO6 | - | | VCCIO6 | - | |
| W4 | VCCIO6 | - | | VCCIO6 | - | |
| AA4 | VCCIO6 | - | | VCCIO6 | - | |
| AE7 | VCCIO5 | - | | VCCIO5 | - | |
| AH6 | VCCIO5 | - | | VCCIO5 | - | |

## LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| B29 | NC | - | | NC | - | |

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M15 and LatticeSC/M25 in a 900-pin package supports a 16-bit MPI interface.

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AJ31 | PB9A | 5 | | PB9A | 5 | |
| AH30 | PB9B | 5 | | PB9B | 5 | |
| AM30 | PB11A | 5 | | PB11A | 5 | |
| AM29 | PB11B | 5 | | PB11B | 5 | |
| AH29 | PB11C | 5 | | PB11C | 5 | |
| AH28 | PB11D | 5 | | PB11D | 5 | |
| AJ27 | PB12A | 5 | | PB13A | 5 | |
| AK27 | PB12B | 5 | | PB13B | 5 | |
| AE22 | PB12C | 5 | | PB13C | 5 | |
| AF23 | PB12D | 5 | | PB13D | 5 | |
| AL28 | PB13A | 5 | | PB15A | 5 | |
| AL27 | PB13B | 5 | | PB15B | 5 | |
| AC21 | PB13C | 5 | | PB15C | 5 | |
| AD21 | PB13D | 5 | | PB15D | 5 | |
| AM28 | PB15A | 5 | | PB17A | 5 | |
| AM27 | PB15B | 5 | | PB17B | 5 | |
| AG23 | PB15C | 5 | | PB17C | 5 | |
| AF22 | PB15D | 5 | | PB17D | 5 | |
| AG26 | PB16A | 5 | | PB19A | 5 | |
| AG25 | PB16B | 5 | | PB19B | 5 | |
| AL26 | PB17A | 5 | | PB22A | 5 | |
| AM26 | PB17B | 5 | | PB22B | 5 | |
| AJ24 | PB19A | 5 | | PB25A | 5 | |
| AK24 | PB19B | 5 | | PB25B | 5 | |
| AE21 | PB19C | 5 | | PB25C | 5 | |
| AE20 | PB19D | 5 | | PB25D | 5 | |
| AJ22 | PB20A | 5 | PCLKT5_3 | PB30A | 5 | PCLKT5_3 |
| AK22 | PB20B | 5 | PCLKC5_3 | PB30B | 5 | PCLKC5_3 |
| AG22 | PB20C | 5 | PCLKT5_4 | PB30C | 5 | PCLKT5_4 |
| AH22 | PB20D | 5 | PCLKC5_4 | PB30D | 5 | PCLKC5_4 |
| AL23 | PB21A | 5 | PCLKT5_5 | PB31A | 5 | PCLKT5_5 |
| AL22 | PB21B | 5 | PCLKC5_5 | PB31B | 5 | PCLKC5_5 |
| AH23 | PB21C | 5 | | PB31C | 5 | |
| AH24 | PB21D | 5 | | PB31D | 5 | |
| AJ21 | PB23A | 5 | PCLKT5_0 | PB33A | 5 | PCLKT5_0 |
| AK21 | PB23B | 5 | PCLKC5_0 | PB33B | 5 | PCLKC5_0 |
| AE19 | PB23C | 5 | | PB33C | 5 | |
| AF19 | PB23D | 5 | VREF2_5 | PB33D | 5 | VREF2_5 |
| AM23 | PB24A | 5 | PCLKT5_1 | PB34A | 5 | PCLKT5_1 |
| AM22 | PB24B | 5 | PCLKC5_1 | PB34B | 5 | PCLKC5_1 |
| AH25 | PB24C | 5 | PCLKT5_6 | PB34C | 5 | PCLKT5_6 |
| AH26 | PB24D | 5 | PCLKC5_6 | PB34D | 5 | PCLKC5_6 |
| AL21 | PB25A | 5 | PCLKT5_2 | PB35A | 5 | PCLKT5_2 |
| AL20 | PB25B | 5 | PCLKC5_2 | PB35B | 5 | PCLKC5_2 |
| AG20 | PB25C | 5 | PCLKT5_7 | PB35C | 5 | PCLKT5_7 |
| AG19 | PB25D | 5 | PCLKC5_7 | PB35D | 5 | PCLKC5_7 |
| AJ19 | PB28A | 5 | | PB37A | 5 | |
| AK19 | PB28B | 5 | | PB37B | 5 | |
| AD18 | PB28C | 5 | | PB37C | 5 | |
| AE18 | PB28D | 5 | | PB37D | 5 | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AD8 | PR65C | 3 | | PR89C | 3 | |
| AJ3 | PR65B | 3 | | PR89B | 3 | |
| AH3 | PR65A | 3 | | PR89A | 3 | |
| AD7 | PR62D | 3 | | PR86D | 3 | |
| AC7 | PR62C | 3 | | PR86C | 3 | |
| AJ2 | PR62B | 3 | | PR86B | 3 | |
| AH2 | PR62A | 3 | | PR86A | 3 | |
| AF6 | PR61D | 3 | | PR85D | 3 | |
| AF5 | PR61C | 3 | | PR85C | 3 | |
| AF4 | PR61B | 3 | | PR85B | 3 | |
| AE4 | PR61A | 3 | | PR85A | 3 | |
| AD6 | PR60D | 3 | | PR84D | 3 | |
| AC6 | PR60C | 3 | | PR84C | 3 | |
| AG2 | PR60B | 3 | | PR84B | 3 | |
| AF2 | PR60A | 3 | | PR84A | 3 | |
| AC8 | PR58D | 3 | | PR82D | 3 | |
| AB8 | PR58C | 3 | | PR82C | 3 | |
| AK1 | PR58B | 3 | | PR82B | 3 | |
| AJ1 | PR58A | 3 | | PR82A | 3 | |
| AB10 | PR57D | 3 | | PR81D | 3 | |
| AA10 | PR57C | 3 | | PR81C | 3 | |
| AF3 | PR57B | 3 | | PR81B | 3 | |
| AE3 | PR57A | 3 | | PR81A | 3 | |
| AE5 | PR56D | 3 | | PR80D | 3 | |
| AD5 | PR56C | 3 | | PR80C | 3 | |
| AE2 | PR56B | 3 | | PR80B | 3 | |
| AD2 | PR56A | 3 | | PR80A | 3 | |
| AC5 | PR53D | 3 | | PR78D | 3 | |
| AB5 | PR53C | 3 | | PR78C | 3 | |
| AF1 | PR53B | 3 | | PR78B | 3 | |
| AE1 | PR53A | 3 | | PR78A | 3 | |
| AA11 | PR52D | 3 | | PR77D | 3 | |
| Y11 | PR52C | 3 | | PR77C | 3 | |
| AC4 | PR52B | 3 | | PR77B | 3 | |
| AB4 | PR52A | 3 | | PR77A | 3 | |
| AA8 | PR51D | 3 | DIFFR_3 | PR76D | 3 | DIFFR_3 |
| AA9 | PR51C | 3 | | PR76C | 3 | |
| AC3 | PR51B | 3 | | PR76B | 3 | |
| AB3 | PR51A | 3 | | PR76A | 3 | |
| AA7 | PR49D | 3 | | PR65D | 3 | |
| Y7 | PR49C | 3 | | PR65C | 3 | |
| AA2 | PR49B | 3 | | PR65B | 3 | |
| Y2 | PR49A | 3 | | PR65A | 3 | |
| AA6 | PR48D | 3 | | PR63D | 3 | |
| Y6 | PR48C | 3 | | PR63C | 3 | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| N27 | PL47C | 7 | |
| P27 | PL47D | 7 | |
| K33 | PL49A | 7 | |
| L33 | PL49B | 7 | |
| M30 | PL49C | 7 | |
| N30 | PL49D | 7 | |
| M31 | PL51A | 7 | |
| N31 | PL51B | 7 | |
| P24 | PL51C | 7 | |
| R24 | PL51D | 7 | |
| M33 | PL56A | 7 | |
| N33 | PL56B | 7 | |
| U25 | PL56C | 7 | |
| T25 | PL56D | 7 | |
| L34 | PL57A | 7 | |
| M34 | PL57B | 7 | |
| P29 | PL57C | 7 | |
| R29 | PL57D | 7 | |
| N34 | PL60A | 7 | |
| P34 | PL60B | 7 | |
| R27 | PL60C | 7 | |
| T27 | PL60D | 7 | |
| R32 | PL61A | 7 | PCLKT7_1 |
| R31 | PL61B | 7 | PCLKC7_1 |
| U24 | PL61C | 7 | PCLKT7_3 |
| T24 | PL61D | 7 | PCLKC7_3 |
| P33 | PL62A | 7 | PCLKT7_0 |
| R33 | PL62B | 7 | PCLKC7_0 |
| T26 | PL62C | 7 | PCLKT7_2 |
| U26 | PL62D | 7 | PCLKC7_2 |
| T32 | PL64A | 6 | PCLKT6_0 |
| T31 | PL64B | 6 | PCLKC6_0 |
| U29 | PL64C | 6 | PCLKT6_1 |
| V29 | PL64D | 6 | PCLKC6_1 |
| T30 | PL65A | 6 | |
| U30 | PL65B | 6 | |
| U27 | PL65C | 6 | PCLKT6_3 |
| V27 | PL65D | 6 | PCLKC6_3 |
| R34 | PL66A | 6 | |
| T34 | PL66B | 6 | |
| U28 | PL66C | 6 | PCLKT6_2 |
| V28 | PL66D | 6 | PCLKC6_2 |
| V30 | PL69A | 6 | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| V8 | PR65D | 3 | PCLKC3_3 |
| U8 | PR65C | 3 | PCLKT3_3 |
| U5 | PR65B | 3 | |
| T5 | PR65A | 3 | |
| V6 | PR64D | 3 | PCLKC3_1 |
| U6 | PR64C | 3 | PCLKT3_1 |
| T4 | PR64B | 3 | PCLKC3_0 |
| T3 | PR64A | 3 | PCLKT3_0 |
| U9 | PR62D | 2 | PCLKC2_2 |
| T9 | PR62C | 2 | PCLKT2_2 |
| R2 | PR62B | 2 | PCLKC2_0 |
| P2 | PR62A | 2 | PCLKT2_0 |
| T11 | PR61D | 2 | PCLKC2_3 |
| U11 | PR61C | 2 | PCLKT2_3 |
| R4 | PR61B | 2 | PCLKC2_1 |
| R3 | PR61A | 2 | PCLKT2_1 |
| T8 | PR60D | 2 | |
| R8 | PR60C | 2 | |
| P1 | PR60B | 2 | |
| N1 | PR60A | 2 | |
| R6 | PR57D | 2 | |
| P6 | PR57C | 2 | |
| M1 | PR57B | 2 | |
| L1 | PR57A | 2 | |
| T10 | PR56D | 2 | |
| U10 | PR56C | 2 | |
| N2 | PR56B | 2 | |
| M2 | PR56A | 2 | |
| R11 | PR51D | 2 | |
| P11 | PR51C | 2 | |
| N4 | PR51B | 2 | |
| M4 | PR51A | 2 | |
| N5 | PR49D | 2 | |
| M5 | PR49C | 2 | |
| L2 | PR49B | 2 | |
| K2 | PR49A | 2 | |
| P8 | PR47D | 2 | |
| N8 | PR47C | 2 | |
| J2 | PR47B | 2 | |
| H2 | PR47A | 2 | |
| M6 | PR45D | 2 | |
| L6 | PR45C | 2 | |
| K3 | PR45B | 2 | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| AL5 | GND | - | |
| AM14 | GND | - | |
| AM18 | GND | - | |
| AM24 | GND | - | |
| AM30 | GND | - | |
| AM8 | GND | - | |
| AN1 | GND | - | |
| AN34 | GND | - | |
| AP2 | GND | - | |
| AP33 | GND | - | |
| B1 | GND | - | |
| B34 | GND | - | |
| C11 | GND | - | |
| C12 | GND | - | |
| C13 | GND | - | |
| C14 | GND | - | |
| C17 | GND | - | |
| C21 | GND | - | |
| C22 | GND | - | |
| C23 | GND | - | |
| C24 | GND | - | |
| C26 | GND | - | |
| C27 | GND | - | |
| C30 | GND | - | |
| C31 | GND | - | |
| C4 | GND | - | |
| C5 | GND | - | |
| C8 | GND | - | |
| C9 | GND | - | |
| D18 | GND | - | |
| E32 | GND | - | |
| E4 | GND | - | |
| F19 | GND | - | |
| G16 | GND | - | |
| G29 | GND | - | |
| G7 | GND | - | |
| H3 | GND | - | |
| H31 | GND | - | |
| J10 | GND | - | |
| J15 | GND | - | |
| J26 | GND | - | |
| K20 | GND | - | |
| K23 | GND | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AF40 | PL76A | 6 | | PL90A | 6 | |
| AG40 | PL76B | 6 | | PL90B | 6 | |
| AG36 | PL76C | 6 | | PL90C | 6 | |
| AH36 | PL76D | 6 | DIFFR_6 | PL90D | 6 | DIFFR_6 |
| AF39 | PL77A | 6 | | PL91A | 6 | |
| AG39 | PL77B | 6 | | PL91B | 6 | |
| AF29 | PL77C | 6 | | PL91C | 6 | |
| AG29 | PL77D | 6 | | PL91D | 6 | |
| AH42 | PL78A | 6 | | PL92A | 6 | |
| AG42 | PL78B | 6 | | PL92B | 6 | |
| AG35 | PL78C | 6 | | PL92C | 6 | |
| AH35 | PL78D | 6 | | PL92D | 6 | |
| AG41 | PL80A | 6 | | PL94A | 6 | |
| AH41 | PL80B | 6 | | PL94B | 6 | |
| AG34 | PL80C | 6 | | PL94C | 6 | |
| AH34 | PL80D | 6 | | PL94D | 6 | |
| AJ42 | PL81A | 6 | | PL96A | 6 | |
| AK42 | PL81B | 6 | | PL96B | 6 | |
| AG33 | PL81C | 6 | | PL96C | 6 | |
| AH33 | PL81D | 6 | | PL96D | 6 | |
| AJ41 | PL82A | 6 | | PL98A | 6 | |
| AK41 | PL82B | 6 | | PL98B | 6 | |
| AJ37 | PL82C | 6 | | PL98C | 6 | |
| AK37 | PL82D | 6 | | PL98D | 6 | |
| AJ40 | PL84A | 6 | | PL99A | 6 | |
| AK40 | PL84B | 6 | | PL99B | 6 | |
| AJ34 | PL84C | 6 | | PL99C | 6 | |
| AK34 | PL84D | 6 | | PL99D | 6 | |
| AJ38 | PL85A | 6 | | PL103A | 6 | |
| AK38 | PL85B | 6 | | PL103B | 6 | |
| AH32 | PL85C | 6 | | PL103C | 6 | |
| AJ32 | PL85D | 6 | | PL103D | 6 | |
| AL42 | PL86A | 6 | | PL104A | 6 | |
| AM42 | PL86B | 6 | | PL104B | 6 | |
| AK36 | PL86C | 6 | | PL104C | 6 | |
| AL36 | PL86D | 6 | | PL104D | 6 | |
| AL38 | PL89A | 6 | | PL107A | 6 | |
| AM38 | PL89B | 6 | | PL107B | 6 | |
| AJ33 | PL89C | 6 | | PL107C | 6 | |
| AK33 | PL89D | 6 | VREF2_6 | PL107D | 6 | VREF2_6 |
| AN42 | PL90A | 6 | | PL109A | 6 | |
| AP42 | PL90B | 6 | | PL109B | 6 | |
| AH31 | PL90C | 6 | | PL109C | 6 | |
| AJ31 | PL90D | 6 | | PL109D | 6 | |
| AN41 | PL91A | 6 | | PL112A | 6 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| E37 | B_HDINN0_L | - | PCS 361 CH 0 IN N | B_HDINN0_L | - | PCS 361 CH 0 IN N |
| D37 | B_HDINP0_L | - | PCS 361 CH 0 IN P | B_HDINP0_L | - | PCS 361 CH 0 IN P |
| F34 | B_VDDIB0_L | - | | B_VDDIB0_L | - | |
| N29 | VCC12 | - | | VCC12 | - | |
| L30 | A_VDDIB3_L | - | | A_VDDIB3_L | - | |
| K31 | VCC12 | - | | VCC12 | - | |
| D38 | A_HDINP3_L | - | PCS 360 CH 3 IN P | A_HDINP3_L | - | PCS 360 CH 3 IN P |
| E38 | A_HDINN3_L | - | PCS 360 CH 3 IN N | A_HDINN3_L | - | PCS 360 CH 3 IN N |
| A37 | A_HDOUTP3_L | - | PCS 360 CH 3 OUT P | A_HDOUTP3_L | - | PCS 360 CH 3 OUT P |
| G37 | VCC12 | - | | VCC12 | - | |
| B37 | A_HDOUTN3_L | - | PCS 360 CH 3 OUT N | A_HDOUTN3_L | - | PCS 360 CH 3 OUT N |
| L33 | A_VDDOB3_L | - | | A_VDDOB3_L | - | |
| B38 | A_HDOUTN2_L | - | PCS 360 CH 2 OUT N | A_HDOUTN2_L | - | PCS 360 CH 2 OUT N |
| D41 | A_VDDOB2_L | - | | A_VDDOB2_L | - | |
| A38 | A_HDOUTP2_L | - | PCS 360 CH 2 OUT P | A_HDOUTP2_L | - | PCS 360 CH 2 OUT P |
| K34 | VCC12 | - | | VCC12 | - | |
| E39 | A_HDINN2_L | - | PCS 360 CH 2 IN N | A_HDINN2_L | - | PCS 360 CH 2 IN N |
| D39 | A_HDINP2_L | - | PCS 360 CH 2 IN P | A_HDINP2_L | - | PCS 360 CH 2 IN P |
| M32 | A_VDDIB2_L | - | | A_VDDIB2_L | - | |
| J32 | VCC12 | - | | VCC12 | - | |
| E41 | A_VDDIB1_L | - | | A_VDDIB1_L | - | |
| M33 | VCC12 | - | | VCC12 | - | |
| D40 | A_HDINP1_L | - | PCS 360 CH 1 IN P | A_HDINP1_L | - | PCS 360 CH 1 IN P |
| E40 | A_HDINN1_L | - | PCS 360 CH 1 IN N | A_HDINN1_L | - | PCS 360 CH 1 IN N |
| B39 | A_HDOUTP1_L | - | PCS 360 CH 1 OUT P | A_HDOUTP1_L | - | PCS 360 CH 1 OUT P |
| B41 | VCC12 | - | | VCC12 | - | |
| A39 | A_HDOUTN1_L | - | PCS 360 CH 1 OUT N | A_HDOUTN1_L | - | PCS 360 CH 1 OUT N |
| C41 | A_VDDOB1_L | - | | A_VDDOB1_L | - | |
| B40 | A_HDOUTN0_L | - | PCS 360 CH 0 OUT N | A_HDOUTN0_L | - | PCS 360 CH 0 OUT N |
| E42 | A_VDDOB0_L | - | | A_VDDOB0_L | - | |
| A40 | A_HDOUTP0_L | - | PCS 360 CH 0 OUT P | A_HDOUTP0_L | - | PCS 360 CH 0 OUT P |
| F42 | VCC12 | - | | VCC12 | - | |
| D42 | A_HDINN0_L | - | PCS 360 CH 0 IN N | A_HDINN0_L | - | PCS 360 CH 0 IN N |
| C42 | A_HDINP0_L | - | PCS 360 CH 0 IN P | A_HDINP0_L | - | PCS 360 CH 0 IN P |
| H39 | A_VDDIB0_L | - | | A_VDDIB0_L | - | |
| F41 | VCC12 | - | | VCC12 | - | |
| P16 | VDDAX25_R | - | | VDDAX25_R | - | |
| P27 | VDDAX25_L | - | | VDDAX25_L | - | |
| K39 | NC | - | | PL32A | 7 | |
| L39 | NC | - | | PL32B | 7 | |
| M38 | NC | - | | PL35A | 7 | |
| K40 | NC | - | | PL36A | 7 | |
| L40 | NC | - | | PL36B | 7 | |
| N37 | NC | - | | PL39A | 7 | |
| P37 | NC | - | | PL39B | 7 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AC24 | GND | - | | GND | - | |
| AC26 | GND | - | | GND | - | |
| AC35 | GND | - | | GND | - | |
| AC8 | GND | - | | GND | - | |
| AD12 | GND | - | | GND | - | |
| AD16 | GND | - | | GND | - | |
| AD18 | GND | - | | GND | - | |
| AD20 | GND | - | | GND | - | |
| AD23 | GND | - | | GND | - | |
| AD25 | GND | - | | GND | - | |
| AD27 | GND | - | | GND | - | |
| AD31 | GND | - | | GND | - | |
| AE17 | GND | - | | GND | - | |
| AE19 | GND | - | | GND | - | |
| AE24 | GND | - | | GND | - | |
| AE26 | GND | - | | GND | - | |
| AE3 | GND | - | | GND | - | |
| AE39 | GND | - | | GND | - | |
| AF18 | GND | - | | GND | - | |
| AF20 | GND | - | | GND | - | |
| AF23 | GND | - | | GND | - | |
| AF25 | GND | - | | GND | - | |
| AF36 | GND | - | | GND | - | |
| AF7 | GND | - | | GND | - | |
| AG11 | GND | - | | GND | - | |
| AG16 | GND | - | | GND | - | |
| AG19 | GND | - | | GND | - | |
| AG24 | GND | - | | GND | - | |
| AG27 | GND | - | | GND | - | |
| AG32 | GND | - | | GND | - | |
| AH15 | GND | - | | GND | - | |
| AH28 | GND | - | | GND | - | |
| AH4 | GND | - | | GND | - | |
| AH40 | GND | - | | GND | - | |
| AJ35 | GND | - | | GND | - | |
| AJ8 | GND | - | | GND | - | |
| AK12 | GND | - | | GND | - | |
| AK31 | GND | - | | GND | - | |
| AL13 | GND | - | | GND | - | |
| AL19 | GND | - | | GND | - | |
| AL24 | GND | - | | GND | - | |
| AL3 | GND | - | | GND | - | |
| AL30 | GND | - | | GND | - | |
| AL39 | GND | - | | GND | - | |
| AM16 | GND | - | | GND | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AW25 | VCCIO5 | - | | VCCIO5 | - | |
| AW31 | VCCIO5 | - | | VCCIO5 | - | |
| AW37 | VCCIO5 | - | | VCCIO5 | - | |
| AY22 | VCCIO5 | - | | VCCIO5 | - | |
| AY28 | VCCIO5 | - | | VCCIO5 | - | |
| AY34 | VCCIO5 | - | | VCCIO5 | - | |
| AB39 | VCCIO6 | - | | VCCIO6 | - | |
| AC36 | VCCIO6 | - | | VCCIO6 | - | |
| AD32 | VCCIO6 | - | | VCCIO6 | - | |
| AE40 | VCCIO6 | - | | VCCIO6 | - | |
| AF35 | VCCIO6 | - | | VCCIO6 | - | |
| AG31 | VCCIO6 | - | | VCCIO6 | - | |
| AH39 | VCCIO6 | - | | VCCIO6 | - | |
| AJ36 | VCCIO6 | - | | VCCIO6 | - | |
| AK32 | VCCIO6 | - | | VCCIO6 | - | |
| AL40 | VCCIO6 | - | | VCCIO6 | - | |
| AM35 | VCCIO6 | - | | VCCIO6 | - | |
| AP39 | VCCIO6 | - | | VCCIO6 | - | |
| AR36 | VCCIO6 | - | | VCCIO6 | - | |
| AU40 | VCCIO6 | - | | VCCIO6 | - | |
| AA40 | VCCIO7 | - | | VCCIO7 | - | |
| H36 | VCCIO7 | - | | VCCIO7 | - | |
| J40 | VCCIO7 | - | | VCCIO7 | - | |
| L35 | VCCIO7 | - | | VCCIO7 | - | |
| M39 | VCCIO7 | - | | VCCIO7 | - | |
| P36 | VCCIO7 | - | | VCCIO7 | - | |
| R40 | VCCIO7 | - | | VCCIO7 | - | |
| T31 | VCCIO7 | - | | VCCIO7 | - | |
| U35 | VCCIO7 | - | | VCCIO7 | - | |
| V39 | VCCIO7 | - | | VCCIO7 | - | |
| W32 | VCCIO7 | - | | VCCIO7 | - | |
| Y36 | VCCIO7 | - | | VCCIO7 | - | |
| AA14 | VTT_2 | 2 | | VTT_2 | 2 | |
| AA15 | VTT_2 | 2 | | VTT_2 | 2 | |
| R12 | VTT_2 | 2 | | VTT_2 | 2 | |
| V14 | VTT_2 | 2 | | VTT_2 | 2 | |
| AB14 | VTT_3 | 3 | | VTT_3 | 3 | |
| AB15 | VTT_3 | 3 | | VTT_3 | 3 | |
| AE14 | VTT_3 | 3 | | VTT_3 | 3 | |
| AJ13 | VTT_3 | 3 | | VTT_3 | 3 | |
| AH21 | VTT_4 | 4 | | VTT_4 | 4 | |
| AJ18 | VTT_4 | 4 | | VTT_4 | 4 | |
| AJ19 | VTT_4 | 4 | | VTT_4 | 4 | |
| AJ20 | VTT_4 | 4 | | VTT_4 | 4 | |
| AJ21 | VTT_4 | 4 | | VTT_4 | 4 | |