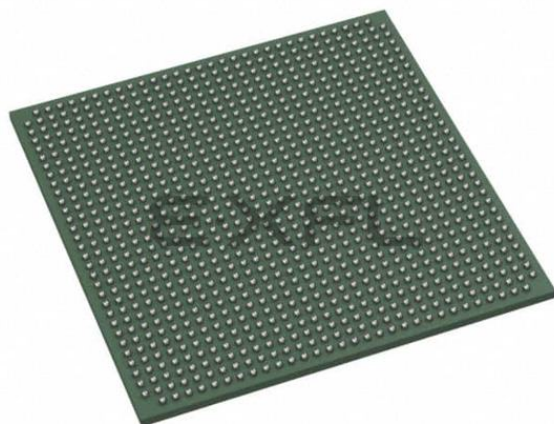




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	562
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga40e-6ff1020i

Features

■ High Performance FPGA Fabric

- 15K to 115K four input Look-up Tables (LUT4s)
- 139 to 942 I/Os
- 700MHz global clock; 1GHz edge clocks

■ 4 to 32 High Speed SERDES and flexiPCS™ (per Device)

- Performance ranging from 600Mbps to 3.8Gbps
- Excellent Rx jitter tolerance (0.8UI at 3.125Gbps)
- Low Tx jitter (0.25UI typical at 3.125Gbps)
- Built-in Pre-emphasis and equalization
- Low power (typically 105mW per channel)
- Embedded Physical Coding Sublayer (PCS) provides pre-engineered implementation for the following standards:
 - GbE, XAUI, PCI Express, SONET, Serial RapidIO, 1G Fibre Channel, 2G Fibre Channel

■ 2Gbps High Performance PURESPEED™ I/O

- Supports the following performance bandwidths
 - Differential I/O up to 2Gbps DDR (1GHz Clock)
 - Single-ended memory interfaces up to 800Mbps
- 144 Tap programmable Input Delay (INDEL) block on every I/O dynamically aligns data to clock for robust performance
 - Dynamic bit Adaptive Input Logic (AIL) monitoring and control circuitry per pin that automatically ensures proper set-up and hold
 - Dynamic bus: uses control bus from DLL
 - Static per bit
- Electrical standards supported:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2, LVTTTL
 - SSTL 3/2/18 I, II; HSTL 18/15 I, II
 - PCI, PCI-X
 - LVDS, Mini-LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS
- Programmable On Die Termination (ODT)
 - Includes Thevenin Equivalent and low power V_{TT} termination options

■ Memory Intensive FPGA

- sysMEM™ embedded Block RAM

- 1 to 7.8 Mbits memory
- True Dual Port/Pseudo Dual Port/Single Port
- Dedicated FIFO logic for all block RAM
- 500MHz performance
- Additional 240K to 1.8Mbits distributed RAM

■ sysCLOCK™ Network

- Eight analog PLLs per device
 - Frequency range from 15MHz to 1GHz
 - Spread spectrum support
- 12 DLLs per device with direct control of I/O delay
 - Frequency range from 100MHz to 700MHz
- Extensive clocking network
 - 700MHz primary and 325 MHz secondary clocks
 - 1GHz I/O-connected edge clocks
- Precision Clock Divider
 - Phase matched x2 and x4 division of incoming clocks
- Dynamic Clock Select (DCS)
 - Glitch free clock MUX

■ Masked Array for Cost Optimization (MACO™) Blocks

- On-chip structured ASIC Blocks provide pre-engineered IP for low power, low cost system level integration

■ High Performance System Bus

- Ties FPGA elements together with a standard bus framework
 - Connects to peripheral user interfaces for run-time dynamic configuration

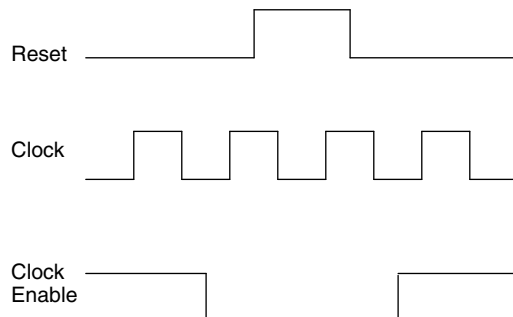
■ System Level Support

- IEEE standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer
- IEEE Standard 1532 in-system configuration
- 1.2V and 1.0V operation
- Onboard oscillator for initialization and general use
- Embedded PowerPC microprocessor interface
- Low cost wire-bond and high pin count flip-chip packaging
- Low cost SPI Flash RAM configuration

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset, as shown in Figure 2-16.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM, FIFO and shift register implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-16. The reset timing rules apply to the RPRreset input vs. the RE input and the RST input vs. the WE and RE inputs. Both RST and RPRreset are always asynchronous EBR inputs. For the EBR shift register mode, the GSR signal is always enabled and the local RESET pin is always asynchronous.

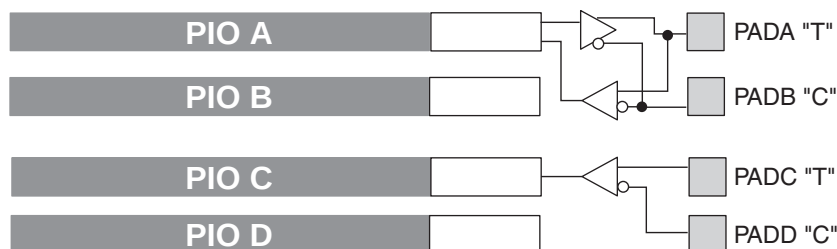
Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled. For more information about on-chip memory, see TN1094, [On-Chip Memory Usage Guide for LatticeSC Devices](#).

Programmable I/O Cells (PIC)

Each PIC contains four PIOs connected to their respective PURESPEED I/O Buffer which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to PURESPEED I/O buffer, and receives input (DI) from the buffer. The PIO contains advanced capabilities to allow the support of speeds up to 2Gbps. These include dedicated shift and DDR logic and adaptive input logic. The dedicated resources simplify the design of robust interfaces.

high-speed interfaces in the LatticeSC devices. Figure 2-18 shows how differential receivers and drivers are arranged between PIOs.

Figure 2-18. Differential Drivers and Receivers



*Differential Driver only available on right and left of the device.

PIO

The PIO contains five blocks: an input register block, output register block, tristate register block, update block, and a control logic block. These blocks contain registers for both single data rate (SDR), double data rate (DDR), and shift register operation along with the necessary clock and selection logic.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 show the diagram of the input register block. The signal from the PURE-SPEED I/O buffer (DI) enters the input register block and can be used for three purposes, as a source for the combinatorial (INDD) and clock outputs (INCK), the input into the SDR register/latch block and the input to the delay block. The output of the delay block can be used as combinatorial (INDD) and clock (INCK) outputs, an input to the DDR/Shift Register Block or an input into the SDR register block.

Input SDR Register/Latch Block

The SDR register/latch block has a latch and a register/latch that can be used in a variety of combinations to provide a registered or latched output (INFF). The latch operates off high-speed input clocks and latches data on the positive going edge. The register/latch operates off the low-speed input clock and registers/latches data on the positive going edge. Both the latch and the register/latch have a clock enable input that is driven by the input clock enable. In addition both have a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register and latch LSR inputs are driven from LSRI, which is generated from the PIO control MUX. The GSR inputs are driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Input Delay Block

The delay block uses 144 tapped delay lines to obtain coarse and fine delay resolution. These delays can be adjusted during configuration or automatically via DLL or AIL blocks. The Adaptive Input Logic (AIL) uses this delay block to adjust automatically the delay in the data path to ensure that it has sufficient setup and hold time.

The delay line in this block matches the delay line that is used in the 12 on-chip DLLs. The delay line can be set via configuration bits or driven from a calibration bus that allows the setting to be controlled either from one of the on-chip DLLs or user logic. Controlling the delay from one of the on-chip DLLs allow the delay to be calibrated to the DLL clock and hence compensated for the variations in process, voltage and temperature.

Figure 2-26. LatticeSC Banks

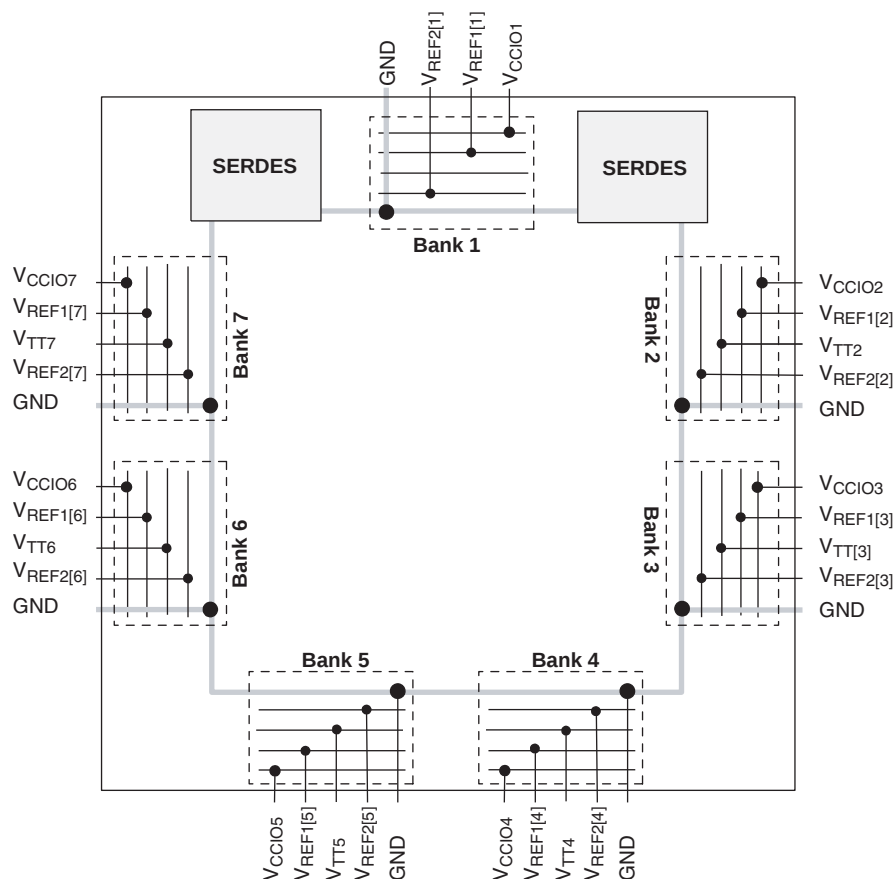


Table 2-7. Maximum Number of I/Os Per Bank in LatticeSC Family

Device	LFSC/M15	LFSC/M25	LFSC/M40	LFSC/M80	LFSC/M115
Bank1	104	80	136	80	136
Bank2	28	36	60	96	136
Bank3	60	84	96	132	156
Bank4	72	100	124	184	208
Bank5	72	100	124	184	208
Bank6	60	84	96	132	156
Bank7	28	36	60	96	136

Note: Not all the I/Os of the Banks are available in all the packages

The LatticeSC devices contain three types of PURESPEED I/O buffers:

1. **Left and Right Sides (Banks 2, 3, 6 and 7)**

These buffers can support LVCMOS standards up to 2.5V. A differential output driver (for LVDS and RSFS) is provided on all primary PIO pairs (A and B) and differential receivers are available on all pairs. Complimentary drivers are available. Adaptive input logic is available on PIOs A or C.

2. **Top Side (Bank 1)**

These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but differential drivers for LVDS and RSFS are not available. Adaptive input logic is not available on this side. Complimentary output drivers are available.

Density Shifting

The LatticeSC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
GTLPLUS15	GTLPLUS15	-0.013	-0.017	0.012	0.004	0.037	0.024	ns
GTL12	GTL12	-0.063	-0.071	-0.007	-0.048	0.056	-0.032	ns
Output Adjusters								
LVDS	LVDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
RSDS	RSDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
BLVDS25	BLVDS	-0.129	0.05	-0.136	0.069	-0.136	0.083	ns
MLVDS25	MLVDS	-0.059	0.059	-0.057	0.096	-0.054	0.133	ns
LVPECL33	LVPECL	-0.334	-0.181	-0.325	-1.389	-0.315	-2.598	ns
HSTL18_I	HSTL_18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18_II	HSTL_18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL18D_I	Differential HSTL 18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18D_II	Differential HSTL 18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL15_I	HSTL_15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15_II	HSTL_15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
HSTL15D_I	Differential HSTL 15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15D_II	Differential HSTL 15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
SSTL33_I	SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33_II	SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL33D_I	Differential SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33D_II	Differential SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL25_I	SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25_II	SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL25D_I	Differential SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25D_II	Differential SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL18_I	SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18_II	SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
SSTL18D_I	Differential SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18D_II	Differential SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
LVTTTL33_8mA	LVTTTL 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVTTTL33_16mA	LVTTTL 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVTTTL33_24mA	LVTTTL 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVC MOS33_24mA	LVC MOS 3.3 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive	-0.174	0.004	-0.195	0.002	-0.215	0	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive	0	0	0	0	0	0	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive	0.094	-0.025	0.107	0.096	0.12	0.216	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive	0.145	-0.054	0.162	0.063	0.181	0.179	ns
LVC MOS25_OD	LVC MOS 2.5 open drain	0.073	-0.125	0.081	-0.081	0.091	-0.09	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive	-0.278	-0.099	-0.312	-0.115	-0.345	-0.131	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive	-0.073	-0.078	-0.078	-0.084	-0.083	-0.089	ns

LatticeSC/M Internal Timing Parameters¹

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Symbol	Description	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
PFU Logic Mode Timing									
t _{LUT4_PFU}	CTOF_DEL	LUT4 delay (A to D inputs to F output)	—	0.045	—	0.050	—	0.054	ns
t _{LUT5_PFU}	MTOOFX_DEL	LUT5 delay (inputs to output)	—	0.152	—	0.172	—	0.192	ns
t _{LSR_PFU}	LSR_DEL	Set/Reset to output (asynchronous)	—	0.378	—	0.426	—	0.474	ns
t _{SUM_PFU}	M_SET	Clock to Mux (M0,M1) input setup time	0.113	—	0.131	—	0.148	—	ns
t _{HM_PFU}	M_HLD	Clock to Mux (M0,M1) input hold time	-0.041	—	-0.046	—	-0.052	—	ns
t _{SUD_PFU}	DIN_SET	Clock to D input setup time	0.072	—	0.083	—	0.094	—	ns
t _{HD_PFU}	DIN_HLD	Clock to D input hold time	-0.028	—	-0.032	—	-0.035	—	ns
t _{CK2Q_PFU}	REG_DEL	Clock to Q delay, D-type register configuration	—	0.224	—	0.252	—	0.279	ns
t _{LE2Q_PFU}	LTCH_DEL	Clock to Q delay latch configuration	—	0.294	—	0.331	—	0.367	ns
t _{LD2Q_PFU}	TLTCH_DEL	D to Q throughput delay when latch is enabled	—	0.300	—	0.338	—	0.376	ns
PFU Memory Mode Timing									
t _{CORAM_PFU}	CLKTOF_DEL	Clock to Output	—	0.575	—	0.649	—	0.724	ns
t _{SUDATA_PFU}	DIN_SET	Data Setup Time	-0.024	—	-0.026	—	-0.027	—	ns
t _{HDATA_PFU}	DIN_HLD	Data Hold Time	0.075	—	0.084	—	0.094	—	ns
t _{SUADDR_PFU}	WAD_SET	Address Setup Time	-0.176	—	-0.196	—	-0.215	—	ns
t _{HADDR_PFU}	WAD_HLD	Address Hold Time	0.110	—	0.124	—	0.138	—	ns
t _{SUWREN_PFU}	WE_SET	Write/Read Enable Setup Time	0.014	—	0.019	—	0.024	—	ns
t _{HWREN_PFU}	WE_HLD	Write/Read Enable Hold Time	0.078	—	0.086	—	0.094	—	ns
PIC Timing									
PIO Input/Output Buffer Timing									
t _{IN_PIO}	IN_DEL	Input Buffer Delay(LVCMOS25)	—	0.578	—	0.661	—	0.744	ns
t _{OUT_PIO}	DOPADI_DEL	Output Buffer Delay(LVCMOS25)	—	2.712	—	3.027	—	3.395	ns
t _{SUI_PIO}	DIN_SET	Input Register Setup Time (Data Before Clock)	0.277	—	0.312	—	0.348	—	ns
t _{HI_PIO}	DIN_HLD	Input Register Hold Time (Data after Clock)	-0.267	—	-0.306	—	-0.345	—	ns
t _{COO_PIO}	CK_DEL	Output Register Clock to Output Delay	—	0.513	—	0.571	—	0.639	ns
t _{SUCE_PIO}	CE_SET	Input Register Clock Enable Setup Time	—	0.000	—	0.000	—	0.000	ns
t _{HCE_PIO}	CE_HLD	Input Register Clock Enable Hold Time	—	0.129	—	0.145	—	0.161	ns
t _{SULSR_PIO}	LSR_SET	Set/Reset Setup Time	0.057	—	0.060	—	0.063	—	ns
t _{HLSR_PIO}	LSR_HLD	Set/Reset Hold Time	-0.151	—	-0.159	—	-0.169	—	ns
t _{LE2Q_PIO}	CK_DEL	Input Register Clock to Q delay latch configuration	—	0.335	—	0.372	—	0.410	ns
t _{LD2Q_PIO}	DIN_DEL	Input Register D to Q throughput delay when latch is enabled	—	0.578	—	0.647	—	0.717	ns

Input Delay Block/AIL Timing

Parameter	Description	Min.	Typ.	Max.	Units
t_{FDEL}	Fine delay time	35	45	80	ps
t_{CDEL}	Coarse delay time	1120	1440	2560	ps
j_{AIL}	AIL jitter tolerance	$1 - ((N + 1) * t_{FDEL}) / (\text{Clock Period})$			UI

1. N = number of fine delays used in a particular AIL setting

GSR Timing

Parameter	Description	VCC	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{SYNC_GSR_MAX}$	Maximum operating frequency for synchronous GSR	1.14V	—	438	—	417	—	398	MHz
		0.95V	—	378	—	355	—	337	MHz
$t_{ASYNC_GSR_MPW}$	Minimum pulse width of asynchronous input	—	—	—	—	—	3.3	—	ns

Note: Synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met.

Internal System Bus Timing

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HCLK}	Maximum operating frequency for internal system bus HCLK.	—	200	—	200	—	200	MHz

Note: There is no minimum frequency. If HCLK is sourced from the embedded oscillator, the minimum frequency limitation of the oscillator/divider is about 0.3 MHz. Refer to the oscillator data for missing configuration modes.

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y24	PL48C	6		PL61C	6	
Y23	PL48D	6		PL61D	6	
AD29	PL49A	6		PL62A	6	
AD30	PL49B	6		PL62B	6	
AF28	PL49C	6		PL62C	6	
AE28	PL49D	6		PL62D	6	
AC28	PL51A	6		PL65A	6	
AD28	PL51B	6		PL65B	6	
AB26	PL51C	6		PL65C	6	
AC26	PL51D	6	VREF2_6	PL65D	6	VREF2_6
AC32	PL52A	6		PL66A	6	
AD32	PL52B	6		PL66B	6	
AA24	PL52C	6		PL66C	6	
AA23	PL52D	6		PL66D	6	
AE30	PL53A	6		PL67A	6	
AE29	PL53B	6		PL67B	6	
AC25	PL53C	6		PL67C	6	
AB25	PL53D	6		PL67D	6	
AE31	PL55A	6		PL69A	6	
AE32	PL55B	6		PL69B	6	
AE26	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AE27	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF32	PL56A	6		PL70A	6	
AF31	PL56B	6		PL70B	6	
AC24	PL56C	6		PL70C	6	
AD25	PL56D	6		PL70D	6	
AG32	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG31	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC23	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AD24	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AH32	XRES	-		XRES	-	
AH31	TEMP	6		TEMP	6	
AJ32	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AK32	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AF27	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AG28	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AK31	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AL31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AE25	PB4C	5		PB4C	5	
AE24	PB4D	5		PB4D	5	
AK30	PB5A	5		PB5A	5	
AL30	PB5B	5		PB5B	5	
AD23	PB5C	5		PB5C	5	
AE23	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AK29	PB7A	5		PB7A	5	
AL29	PB7B	5		PB7B	5	
AF26	PB7C	5		PB7C	5	
AF25	PB7D	5		PB7D	5	
AJ28	PB8A	5		PB8A	5	
AK28	PB8B	5		PB8B	5	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ1	PB69A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AK1	PB69B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ2	PB69C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH3	PB69D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AH1	PROBE_VCC	-		PROBE_VCC	-	
AH2	PROBE_GND	-		PROBE_GND	-	
AD9	PR57D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AC10	PR57C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AG2	PR57B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AG1	PR57A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD8	PR56D	3		PR70D	3	
AC9	PR56C	3		PR70C	3	
AF2	PR56B	3		PR70B	3	
AF1	PR56A	3		PR70A	3	
AE6	PR55D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AE7	PR55C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AE1	PR55B	3		PR69B	3	
AE2	PR55A	3		PR69A	3	
AB8	PR53D	3		PR67D	3	
AC8	PR53C	3		PR67C	3	
AE4	PR53B	3		PR67B	3	
AE3	PR53A	3		PR67A	3	
AA10	PR52D	3		PR66D	3	
AA9	PR52C	3		PR66C	3	
AD1	PR52B	3		PR66B	3	
AC1	PR52A	3		PR66A	3	
AC7	PR51D	3	VREF2_3	PR65D	3	VREF2_3
AB7	PR51C	3		PR65C	3	
AD5	PR51B	3		PR65B	3	
AC5	PR51A	3		PR65A	3	
AE5	PR49D	3		PR62D	3	
AF5	PR49C	3		PR62C	3	
AD3	PR49B	3		PR62B	3	
AD4	PR49A	3		PR62A	3	
Y10	PR48D	3		PR61D	3	
Y9	PR48C	3		PR61C	3	
AC2	PR48B	3		PR61B	3	
AD2	PR48A	3		PR61A	3	
AC6	PR47D	3		PR60D	3	
AB6	PR47C	3		PR60C	3	
AA1	PR47B	3		PR60B	3	
AB1	PR47A	3		PR60A	3	
AA5	PR44D	3		PR53D	3	
AB5	PR44C	3		PR53C	3	
Y1	PR44B	3		PR53B	3	
W1	PR44A	3		PR53A	3	
W8	PR43D	3		PR52D	3	
Y7	PR43C	3		PR52C	3	
Y5	PR43B	3		PR52B	3	
W5	PR43A	3		PR52A	3	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E16	PT45C	1	D3/MPI_DATA3	PT54C	1	D3/MPI_DATA3
C13	PT45B	1	D2/MPI_DATA2	PT53B	1	D2/MPI_DATA2
C14	PT45A	1	D1/MPI_DATA1	PT53A	1	D1/MPI_DATA1
B14	PT43B	1	D0/MPI_DATA0	PT51B	1	D0/MPI_DATA0
B13	PT43A	1	QOUT/CEON	PT51A	1	QOUT/CEON
L13	PT42D	1	VREF2_1	PT50D	1	VREF2_1
C15	PT42B	1	DOUT	PT50B	1	DOUT
D15	PT42A	1	MCA_DONE_IN	PT50A	1	MCA_DONE_IN
J16	PT41B	1	MCA_CLK_P1_OUT	PT49B	1	MCA_CLK_P1_OUT
K16	PT41A	1	MCA_CLK_P1_IN	PT49A	1	MCA_CLK_P1_IN
H15	PT39D	1	D21/PCLKC1_1/MPI_DATA21	PT47D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT39C	1	D22/PCLKT1_1/MPI_DATA22	PT47C	1	D22/PCLKT1_1/MPI_DATA22
A14	PT39B	1	MCA_CLK_P2_OUT	PT47B	1	MCA_CLK_P2_OUT
A13	PT39A	1	MCA_CLK_P2_IN	PT47A	1	MCA_CLK_P2_IN
G16	PT38D	1	MCA_DONE_OUT	PT46D	1	MCA_DONE_OUT
F16	PT38C	1	BUSYN/RCLK/SCK	PT46C	1	BUSYN/RCLK/SCK
B16	PT38B	1	DP0/MPI_PAR0	PT46B	1	DP0/MPI_PAR0
B15	PT38A	1	MPI_TA	PT46A	1	MPI_TA
L16	PT37C	1	DP2/MPI_PAR2	PT45C	1	DP2/MPI_PAR2
A16	PT37B	1	PCLKC1_0	PT45B	1	PCLKC1_0
A15	PT37A	1	PCLKT1_0/MPI_CLK	PT45A	1	PCLKT1_0/MPI_CLK
L17	PT35C	1	D24/PCLKT1_4/MPI_DATA24	PT43C	1	D24/PCLKT1_4/MPI_DATA24
A17	PT35B	1	MPI_RETRY	PT43B	1	MPI_RETRY
A18	PT35A	1	A0/MPI_ADDR14	PT43A	1	A0/MPI_ADDR14
F17	PT33D	1	A1/MPI_ADDR15	PT42D	1	A1/MPI_ADDR15
G17	PT33C	1	A2/MPI_ADDR16	PT42C	1	A2/MPI_ADDR16
B17	PT33B	1	A3/MPI_ADDR17	PT42B	1	A3/MPI_ADDR17
B18	PT33A	1	A4/MPI_ADDR18	PT42A	1	A4/MPI_ADDR18
H17	PT32D	1	D25/PCLKC1_5/MPI_DATA25	PT41D	1	D25/PCLKC1_5/MPI_DATA25
H18	PT32C	1	D26/PCLKT1_5/MPI_DATA26	PT41C	1	D26/PCLKT1_5/MPI_DATA26
A19	PT32B	1	A5/MPI_ADDR19	PT41B	1	A5/MPI_ADDR19
A20	PT32A	1	A6/MPI_ADDR20	PT41A	1	A6/MPI_ADDR20
L20	PT31C	1	VREF1_1	PT39C	1	VREF1_1
J17	PT31B	1	A7/MPI_ADDR21	PT39B	1	A7/MPI_ADDR21
K17	PT31A	1	A8/MPI_ADDR22	PT39A	1	A8/MPI_ADDR22
C18	PT29B	1	A9/MPI_ADDR23	PT38B	1	A9/MPI_ADDR23
D18	PT29A	1	A10/MPI_ADDR24	PT38A	1	A10/MPI_ADDR24
B19	PT28B	1	A11/MPI_ADDR25	PT37B	1	A11/MPI_ADDR25
B20	PT28A	1	A12/MPI_ADDR26	PT37A	1	A12/MPI_ADDR26
E17	PT27D	1	D11/MPI_DATA11	PT35D	1	D11/MPI_DATA11
E18	PT27C	1	D12/MPI_DATA12	PT35C	1	D12/MPI_DATA12
C20	PT27B	1	A13/MPI_ADDR27	PT35B	1	A13/MPI_ADDR27
C19	PT27A	1	A14/MPI_ADDR28	PT35A	1	A14/MPI_ADDR28
H19	PT25D	1	A16/MPI_ADDR30	PT33D	1	A16/MPI_ADDR30
G19	PT25C	1	D13/MPI_DATA13	PT33C	1	D13/MPI_DATA13
D20	PT25B	1	A15/MPI_ADDR29	PT33B	1	A15/MPI_ADDR29
D19	PT25A	1	A17/MPI_ADDR31	PT33A	1	A17/MPI_ADDR31
H20	PT24D	1	A19/MPI_TSI21	PT30D	1	A19/MPI_TSI21
G20	PT24C	1	A20/MPI_BDIP	PT30C	1	A20/MPI_BDIP
E19	PT24B	1	A18/MPI_TSI20	PT30B	1	A18/MPI_TSI20

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E22	VCC12	-		VCC12	-	
E21	VCC12	-		VCC12	-	
E3	VCC12	-		VCC12	-	
E4	VCC12	-		VCC12	-	
E6	VCC12	-		VCC12	-	
E7	VCC12	-		VCC12	-	
E8	VCC12	-		VCC12	-	
E9	VCC12	-		VCC12	-	
E11	VCC12	-		VCC12	-	
E12	VCC12	-		VCC12	-	
A23	GND	-		GND	-	
A31	GND	-		GND	-	
AA13	GND	-		GND	-	
AA15	GND	-		GND	-	
AA18	GND	-		GND	-	
AA20	GND	-		GND	-	
AA26	GND	-		GND	-	
AA6	GND	-		GND	-	
AB10	GND	-		GND	-	
AB24	GND	-		GND	-	
AC14	GND	-		GND	-	
AC22	GND	-		GND	-	
AC29	GND	-		GND	-	
AC3	GND	-		GND	-	
AD11	GND	-		GND	-	
AD19	GND	-		GND	-	
AD27	GND	-		GND	-	
AD7	GND	-		GND	-	
AF12	GND	-		GND	-	
AF18	GND	-		GND	-	
AF24	GND	-		GND	-	
AF30	GND	-		GND	-	
AF4	GND	-		GND	-	
AG15	GND	-		GND	-	
AG21	GND	-		GND	-	
AG9	GND	-		GND	-	
AJ10	GND	-		GND	-	
AJ16	GND	-		GND	-	
AJ20	GND	-		GND	-	
AJ26	GND	-		GND	-	
AJ29	GND	-		GND	-	
AJ4	GND	-		GND	-	
AK13	GND	-		GND	-	
AK17	GND	-		GND	-	
AK23	GND	-		GND	-	
AK7	GND	-		GND	-	
AL1	GND	-		GND	-	
AL32	GND	-		GND	-	
AM2	GND	-		GND	-	
AM31	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P10	GND	-		GND	-	
P13	GND	-		GND	-	
P15	GND	-		GND	-	
P18	GND	-		GND	-	
P20	GND	-		GND	-	
P24	GND	-		GND	-	
R12	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R17	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
R6	GND	-		GND	-	
T15	GND	-		GND	-	
T18	GND	-		GND	-	
T30	GND	-		GND	-	
T4	GND	-		GND	-	
U15	GND	-		GND	-	
U18	GND	-		GND	-	
U29	GND	-		GND	-	
U3	GND	-		GND	-	
V12	GND	-		GND	-	
V14	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V21	GND	-		GND	-	
V27	GND	-		GND	-	
V7	GND	-		GND	-	
W13	GND	-		GND	-	
W15	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W9	GND	-		GND	-	
Y12	GND	-		GND	-	
Y14	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y30	GND	-		GND	-	
Y4	GND	-		GND	-	
N13	VCC	-		VCC	-	
N15	VCC	-		VCC	-	
N16	VCC	-		VCC	-	
N17	VCC	-		VCC	-	
N18	VCC	-		VCC	-	
N20	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F15	PT55A	1	D5/MPI_DATA5	PT74A	1	D5/MPI_DATA5
K14	PT54D	1	D4/MPI_DATA4	PT73D	1	D4/MPI_DATA4
K13	PT54C	1	D3/MPI_DATA3	PT73C	1	D3/MPI_DATA3
B15	PT53B	1	D2/MPI_DATA2	PT73B	1	D2/MPI_DATA2
A15	PT53A	1	D1/MPI_DATA1	PT73A	1	D1/MPI_DATA1
J14	PT51D	1	D16/PCLKC1_3/MPI_DATA16	PT71D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT51C	1	D17/PCLKT1_3/MPI_DATA17	PT71C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT51B	1	D0/MPI_DATA0	PT71B	1	D0/MPI_DATA0
B16	PT51A	1	QOUT/CEON	PT71A	1	QOUT/CEON
J13	PT50D	1	VREF2_1	PT70D	1	VREF2_1
H13	PT50C	1	D18/MPI_DATA18	PT70C	1	D18/MPI_DATA18
D15	PT50B	1	DOUT	PT70B	1	DOUT
E15	PT50A	1	MCA_DONE_IN	PT70A	1	MCA_DONE_IN
J16	PT49D	1	D19/PCLKC1_2/MPI_DATA19	PT69D	1	D19/PCLKC1_2/MPI_DATA19
J17	PT49C	1	D20/PCLKT1_2/MPI_DATA20	PT69C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT49B	1	MCA_CLK_P1_OUT	PT69B	1	MCA_CLK_P1_OUT
E16	PT49A	1	MCA_CLK_P1_IN	PT69A	1	MCA_CLK_P1_IN
H15	PT47D	1	D21/PCLKC1_1/MPI_DATA21	PT67D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT47C	1	D22/PCLKT1_1/MPI_DATA22	PT67C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT47B	1	MCA_CLK_P2_OUT	PT67B	1	MCA_CLK_P2_OUT
C16	PT47A	1	MCA_CLK_P2_IN	PT67A	1	MCA_CLK_P2_IN
L17	PT46D	1	MCA_DONE_OUT	PT66D	1	MCA_DONE_OUT
K17	PT46C	1	BUSYN/RCLK/SCK	PT66C	1	BUSYN/RCLK/SCK
E17	PT46B	1	DP0/MPI_PAR0	PT66B	1	DP0/MPI_PAR0
F17	PT46A	1	MPI_TA	PT66A	1	MPI_TA
G17	PT45D	1	D23/MPI_DATA23	PT65D	1	D23/MPI_DATA23
H17	PT45C	1	DP2/MPI_PAR2	PT65C	1	DP2/MPI_PAR2
A17	PT45B	1	PCLKC1_0	PT65B	1	PCLKC1_0
B17	PT45A	1	PCLKT1_0/MPI_CLK	PT65A	1	PCLKT1_0/MPI_CLK
G18	PT43D	1	DP3/PCLKC1_4/MPI_PAR3	PT63D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT43C	1	D24/PCLKT1_4/MPI_DATA24	PT63C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT43B	1	MPI_RETRY	PT63B	1	MPI_RETRY
F18	PT43A	1	A0/MPI_ADDR14	PT63A	1	A0/MPI_ADDR14
J18	PT42D	1	A1/MPI_ADDR15	PT61D	1	A1/MPI_ADDR15
J19	PT42C	1	A2/MPI_ADDR16	PT61C	1	A2/MPI_ADDR16
C20	PT42B	1	A3/MPI_ADDR17	PT61B	1	A3/MPI_ADDR17
C19	PT42A	1	A4/MPI_ADDR18	PT61A	1	A4/MPI_ADDR18
K18	PT41D	1	D25/PCLKC1_5/MPI_DATA25	PT60D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT41C	1	D26/PCLKT1_5/MPI_DATA26	PT60C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT41B	1	A5/MPI_ADDR19	PT60B	1	A5/MPI_ADDR19
E19	PT41A	1	A6/MPI_ADDR20	PT60A	1	A6/MPI_ADDR20
H19	PT39D	1	D27/MPI_DATA27	PT59D	1	D27/MPI_DATA27
H20	PT39C	1	VREF1_1	PT59C	1	VREF1_1
A18	PT39B	1	A7/MPI_ADDR21	PT59B	1	A7/MPI_ADDR21
B18	PT39A	1	A8/MPI_ADDR22	PT59A	1	A8/MPI_ADDR22

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
R7	NC	-		PR39D	2	
P7	NC	-		PR39C	2	
N3	NC	-		PR39B	2	
M3	NC	-		PR39A	2	
H1	NC	-		PR26B	2	
G1	NC	-		PR26A	2	
L5	NC	-		PR25B	2	
K5	NC	-		PR25A	2	
G2	NC	-		PR24B	2	
F2	NC	-		PR24A	2	
F1	NC	-		PR22B	2	
E1	NC	-		PR22A	2	
A2	GND	-		GND	-	
A33	GND	-		GND	-	
AA15	GND	-		GND	-	
AA20	GND	-		GND	-	
AA32	GND	-		GND	-	
AA4	GND	-		GND	-	
AB28	GND	-		GND	-	
AB6	GND	-		GND	-	
AC11	GND	-		GND	-	
AC18	GND	-		GND	-	
AC25	GND	-		GND	-	
AD23	GND	-		GND	-	
AD3	GND	-		GND	-	
AD31	GND	-		GND	-	
AE12	GND	-		GND	-	
AE15	GND	-		GND	-	
AE29	GND	-		GND	-	
AE7	GND	-		GND	-	
AE9	GND	-		GND	-	
AF20	GND	-		GND	-	
AF26	GND	-		GND	-	
AG32	GND	-		GND	-	
AG4	GND	-		GND	-	
AH13	GND	-		GND	-	
AH19	GND	-		GND	-	
AH25	GND	-		GND	-	
AH7	GND	-		GND	-	
AJ10	GND	-		GND	-	
AJ16	GND	-		GND	-	
AJ22	GND	-		GND	-	
AJ28	GND	-		GND	-	
AK3	GND	-		GND	-	
AK31	GND	-		GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
D9	B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-	
E9	B_VDDIB3_R	-	
L13	VCC12	-	
J11	B_REFCLKN_R	-	
H11	B_REFCLKP_R	-	
M15	PT93D	1	HDC/SI
M16	PT93C	1	LDCN/SCS
F14	PT93B	1	D8/MPI_DATA8
G14	PT93A	1	CS1/MPI_CS1
L15	PT90D	1	D9/MPI_DATA9
L14	PT90C	1	D10/MPI_DATA10
D14	PT90B	1	CS0N/MPI_CS0N
E14	PT90A	1	RDN/MPI_STRB_N
L16	PT89D	1	WRN/MPI_WR_N
K16	PT89C	1	D7/MPI_DATA7
G15	PT89B	1	D6/MPI_DATA6
F15	PT89A	1	D5/MPI_DATA5
K14	PT87D	1	D4/MPI_DATA4
K13	PT87C	1	D3/MPI_DATA3
B15	PT87B	1	D2/MPI_DATA2
A15	PT87A	1	D1/MPI_DATA1
J14	PT86D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT86C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT86B	1	D0/MPI_DATA0
B16	PT86A	1	QOUT/CEON
J13	PT83D	1	VREF2_1
H13	PT83C	1	D18/MPI_DATA18
D15	PT83B	1	DOUT
E15	PT83A	1	MCA_DONE_IN
J16	PT81D	1	D19/PCLKC1_2/MPI_DATA19

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
Y18	VCC	-	
Y20	VCC	-	
AB15	VCC12	-	
AB20	VCC12	-	
N15	VCC12	-	
N20	VCC12	-	
R13	VCC12	-	
R22	VCC12	-	
Y13	VCC12	-	
Y22	VCC12	-	
AA12	VCCAUX	-	
AA23	VCCAUX	-	
AB12	VCCAUX	-	
AB16	VCCAUX	-	
AB17	VCCAUX	-	
AB18	VCCAUX	-	
AB19	VCCAUX	-	
AB23	VCCAUX	-	
AC12	VCCAUX	-	
AC13	VCCAUX	-	
Y19	GND	-	
AC14	VCCAUX	-	
AC17	VCCAUX	-	
AC21	VCCAUX	-	
AC22	VCCAUX	-	
AC23	VCCAUX	-	
M13	VCCAUX	-	
M14	VCCAUX	-	
M18	VCCAUX	-	
M21	VCCAUX	-	
M22	VCCAUX	-	
N12	VCCAUX	-	
N16	VCCAUX	-	
N17	VCCAUX	-	
N18	VCCAUX	-	
N19	VCCAUX	-	
N23	VCCAUX	-	
P12	VCCAUX	-	
P23	VCCAUX	-	
T13	VCCAUX	-	
T22	VCCAUX	-	
U12	VCCAUX	-	
U13	VCCAUX	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2}

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G34	A_REFCLKP_L	-		A_REFCLKP_L	-	
H34	A_REFCLKN_L	-		A_REFCLKN_L	-	
N30	VCC12	-		VCC12	-	
H33	RESP_ULC	-		RESP_ULC	-	
P25	RESETN	1		RESETN	1	
P26	TSALLN	1		TSALLN	1	
P31	DONE	1		DONE	1	
P23	INITN	1		INITN	1	
P30	M0	1		M0	1	
P22	M1	1		M1	1	
P24	M2	1		M2	1	
R22	M3	1		M3	1	
J37	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J38	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
P32	PL16C	7		PL15C	7	
R32	PL16D	7		PL15D	7	
G40	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
H40	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N33	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P33	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
G41	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
H41	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
T29	PL18C	7		PL18C	7	
U29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
G42	PL20A	7		PL19A	7	
H42	PL20B	7		PL19B	7	
M34	PL20C	7		PL19C	7	
M35	PL20D	7		PL19D	7	
K37	PL21A	7		PL26A	7	
L37	PL21B	7		PL26B	7	
N34	PL21C	7		PL26C	7	
P34	PL21D	7		PL26D	7	
K38	PL22A	7		PL30A	7	
L38	PL22B	7		PL30B	7	
T33	PL22C	7		PL30C	7	
R33	PL22D	7		PL30D	7	
J41	PL24A	7		PL34A	7	
K41	PL24B	7		PL34B	7	
U31	PL24C	7		PL34C	7	
V31	PL24D	7		PL34D	7	
K42	PL25A	7		PL38A	7	
J42	PL25B	7		PL38B	7	
J36	PL25C	7		PL38C	7	
K36	PL25D	7		PL38D	7	
N38	PL26A	7		PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P