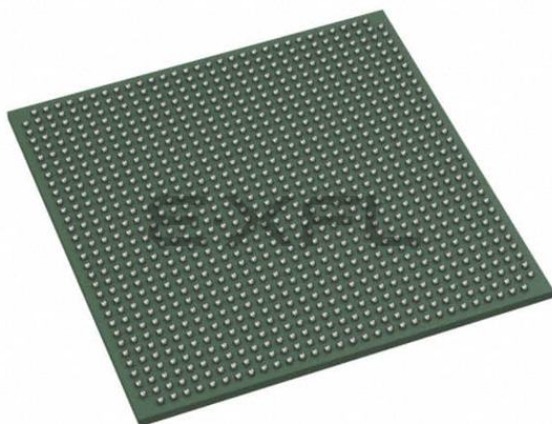




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	562
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga40e-7ff1020c

Features

■ High Performance FPGA Fabric

- 15K to 115K four input Look-up Tables (LUT4s)
- 139 to 942 I/Os
- 700MHz global clock; 1GHz edge clocks

■ 4 to 32 High Speed SERDES and flexiPCS™ (per Device)

- Performance ranging from 600Mbps to 3.8Gbps
- Excellent Rx jitter tolerance (0.8UI at 3.125Gbps)
- Low Tx jitter (0.25UI typical at 3.125Gbps)
- Built-in Pre-emphasis and equalization
- Low power (typically 105mW per channel)
- Embedded Physical Coding Sublayer (PCS) provides pre-engineered implementation for the following standards:
 - GbE, XAUI, PCI Express, SONET, Serial RapidIO, 1G Fibre Channel, 2G Fibre Channel

■ 2Gbps High Performance PURESPEED™ I/O

- Supports the following performance bandwidths
 - Differential I/O up to 2Gbps DDR (1GHz Clock)
 - Single-ended memory interfaces up to 800Mbps
- 144 Tap programmable Input Delay (INDEL) block on every I/O dynamically aligns data to clock for robust performance
 - Dynamic bit Adaptive Input Logic (AIL) monitoring and control circuitry per pin that automatically ensures proper set-up and hold
 - Dynamic bus: uses control bus from DLL
 - Static per bit
- Electrical standards supported:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2, LVTTTL
 - SSTL 3/2/18 I, II; HSTL 18/15 I, II
 - PCI, PCI-X
 - LVDS, Mini-LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS
- Programmable On Die Termination (ODT)
 - Includes Thevenin Equivalent and low power V_{TT} termination options

■ Memory Intensive FPGA

- sysMEM™ embedded Block RAM

- 1 to 7.8 Mbits memory
- True Dual Port/Pseudo Dual Port/Single Port
- Dedicated FIFO logic for all block RAM
- 500MHz performance
- Additional 240K to 1.8Mbits distributed RAM

■ sysCLOCK™ Network

- Eight analog PLLs per device
 - Frequency range from 15MHz to 1GHz
 - Spread spectrum support
- 12 DLLs per device with direct control of I/O delay
 - Frequency range from 100MHz to 700MHz
- Extensive clocking network
 - 700MHz primary and 325 MHz secondary clocks
 - 1GHz I/O-connected edge clocks
- Precision Clock Divider
 - Phase matched x2 and x4 division of incoming clocks
- Dynamic Clock Select (DCS)
 - Glitch free clock MUX

■ Masked Array for Cost Optimization (MACO™) Blocks

- On-chip structured ASIC Blocks provide pre-engineered IP for low power, low cost system level integration

■ High Performance System Bus

- Ties FPGA elements together with a standard bus framework
 - Connects to peripheral user interfaces for run-time dynamic configuration

■ System Level Support

- IEEE standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer
- IEEE Standard 1532 in-system configuration
- 1.2V and 1.0V operation
- Onboard oscillator for initialization and general use
- Embedded PowerPC microprocessor interface
- Low cost wire-bond and high pin count flip-chip packaging
- Low cost SPI Flash RAM configuration

DLLs and dynamic glitch free clock MUXs which are required in today's high end system designs. High-speed, high-bandwidth I/O make this family ideal for high-throughput systems.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeSC family of FPGA devices. Synthesis library support for LatticeSC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeSC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeSC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Innovative high-performance FPGA architecture, high-speed SERDES with PCS support, sysMEM embedded memory and high performance I/O are combined in the LatticeSC to provide excellent performance for today's leading edge systems designs. Table 1-3 details the performance of several common functions implemented within the LatticeSC.

Table1-3. Speed Performance for Typical Functions¹

Functions	Performance (MHz) ²
32-bit Address Decoder	539
64-bit Address Decoder	517
32:1 Multiplexer	779
64-bit Adder (ripple)	353
32x8 Distributed Single Port (SP) RAM	768
64-bit Counter (up or down counter, non-loadable)	369
True Dual-Port 1024x18 bits	372
FIFO Port A: x36 bits, B: x9 bits	375

1. For additional information, see Typical Building BLock Function Performance table in this data sheet.

2. Advance information (-7 speed grade).

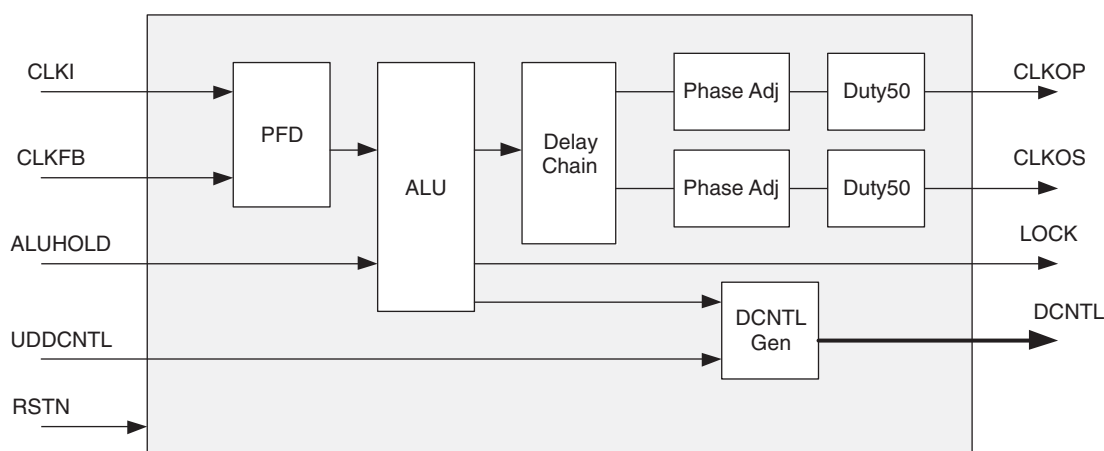
There is a Digital Control (DCNTL) bus available from the DLL block. This Digital Control bus is available to the delay lines in the PIC blocks in the adjacent banks. The UDDCNTL signal allows the user to latch the current value on the digital control bus.

Figure 2-12 shows the DLL block diagram of the DLL inputs and outputs. The output of the phase frequency detector controls an arithmetic logic unit (ALU) to add or subtract one delay tap. The digital output of this ALU is used to control the delay value of the delay chain and this digital code is transmitted via the DCNTL bus.

The sysCLOCK DLL can be configured at power-up, then, if desired, reconfigured dynamically through the Serial Memory Interface bus which interfaces with the on-chip Microprocessor Interface (MPI) bus. In addition, users can drive the SMI interface from routing if desired.

The user can configure the DLL for many common functions such as clock injection match and single delay cell. Lattice provides primitives in its design for time reference delay (DDR memory) and clock injection delay removal.

Figure 2-12. DLL Diagram



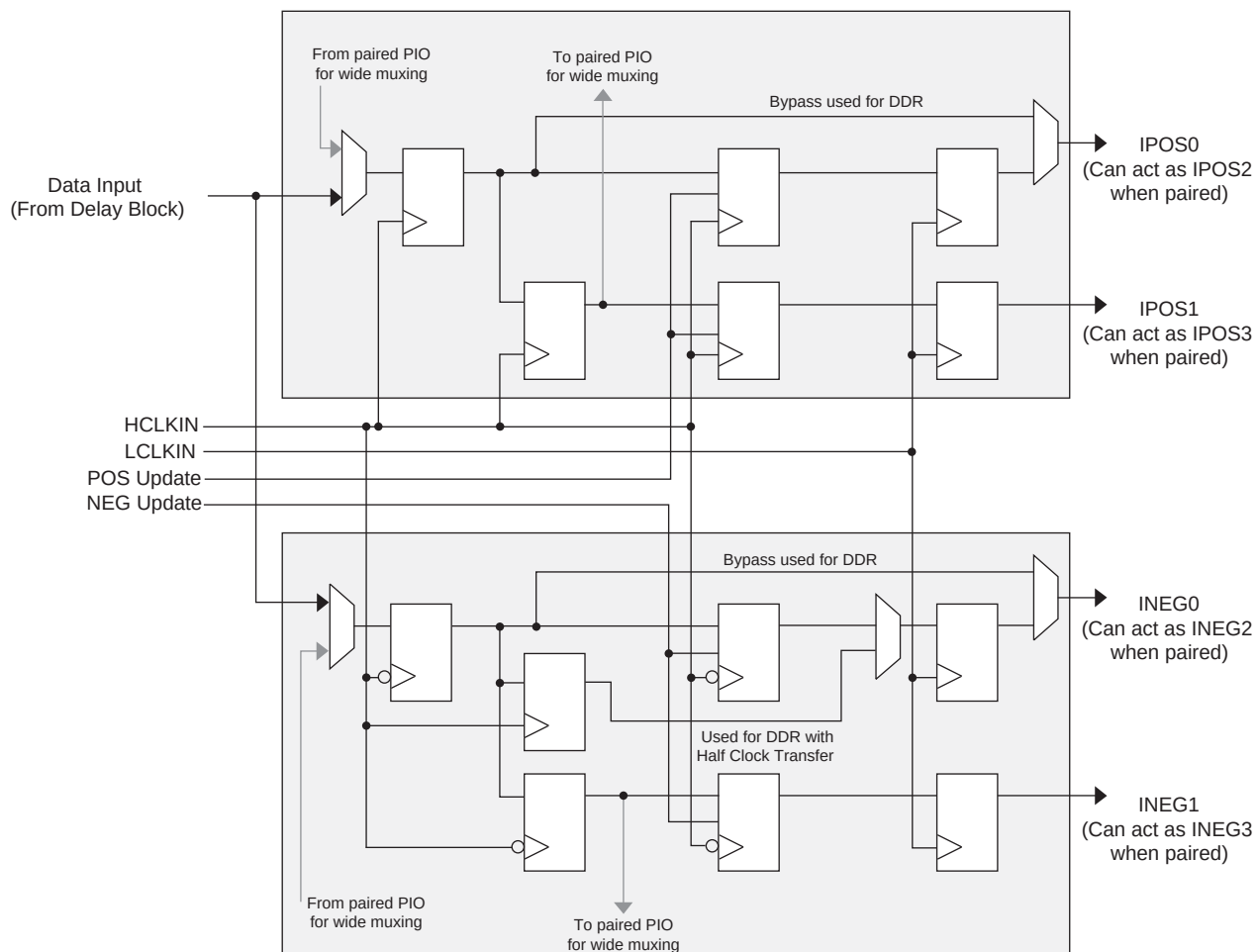
PLL/DLL Cascading

The LatticeSC devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are as follows:

- PLL to PLL
- PLL to DLL
- DLL to DLL
- DLL to PLL

DLLs are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLL and PLLs.

When cascading the DLL to the PLL, the DLL can be used to drive the PLL to create fine phase shifts of an input clock signal. Figure 2-13 shows a shift of all outputs for CLKOP and CLKOS out in time.

Figure 2-21. Input DDR/Shift Register Block

Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the PURESPEED I/O buffers. The block contains a register for SDR operation and a group of registers for DDR and shift register operation. The output signal (DO) can be derived directly from one of the inputs (bypass mode), the SDR register or the DDR/shift register block. Figure 2-22 shows the diagram of the Output Register Block.

Output SDR Register/Latch Block

The SDR register operates on the positive edge of the high-speed clock. It has clock enable that is driven by the clock enable output signal generated by the control MUX. In addition it has a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register LSR input is driven from LSRO, which is generated from the PIO control MUX. The GSR inputs is driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Output DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer from the low-speed clock domain. It functions as a gearbox allowing low-speed parallel data from the FPGA fabric be output as a higher speed serial stream. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. Figure 2-22 shows a simplified block diagram of the shift register block.

3. Bottom Side (Banks 4 and 5)

These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but true HLVDS and RSDS differential drivers are not available. Adaptive input logic is available on PIOs A or C.

Table 2-8 lists the standards supported by each side.

Table 2-8. I/O Standards Supported by Different Banks

Description	Top Side Banks 1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
I/O Buffer Type	Single-ended, Differential Receiver	Single-ended, Differen- tial Receiver and Driver	Single-ended, Differential Receiver	Single-ended, Differen- tial Receiver and Driver
Output Standards Supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_I, II SSTL33_I, II HSTL15_I, II, III ¹ , IV ¹ HSTL18_I, II, III ¹ , IV ¹ SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL ² , GTL+ ²	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_I, II HSTL15_I, III HSTL18_I, II, III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL ² , GTL+ ²	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_I, II SSTL33_I, II HSTL15_I, II, III ¹ , IV ¹ HSTL18_I, II, III ¹ , IV ¹ SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL ² , GTL+ ²	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_I, II HSTL15_I, III HSTL18_I, II, III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL ² , GTL+ ²
Input Standards Supported	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Clock Inputs	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Differential Output Support via Emulation	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL
AIL Support	No	Yes	Yes	Yes

1. Input only.

2. Input only. Outputs supported by bussing multiple outputs together.

Supported Standards

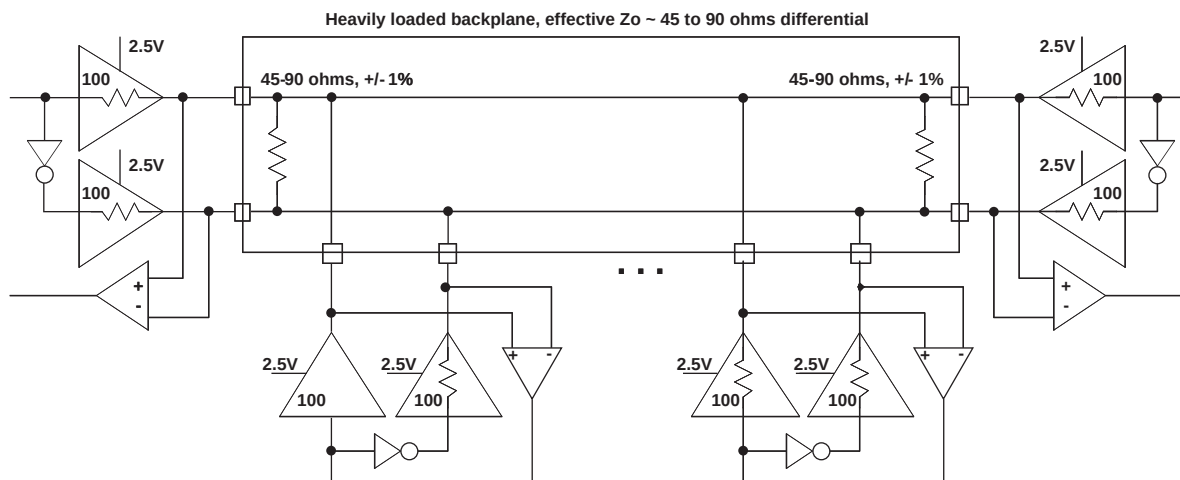
The LatticeSC PURESPEED I/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 12, 15, 18, 25 and 33 standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, termination resistance, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL, HSTL, GTL (input only), GTL+ (input only), PCI33, PCIX33, PCIX15, AGP-1X33 and AGP-2X33. Differential standards supported include LVDS, RSDS, BLVDS, MLVDS, LVPECL, differential SSTL and differential HSTL. Tables 12 and 13 show the I/O standards (together with their supply and reference voltages) supported by the LatticeSC devices. The tables also provide the available internal termination schemes. For further information on utilizing the PURESPEED I/O buffer to support a variety of standards please see details of additional technical documentation at the end of this data sheet.

Density Shifting

The LatticeSC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

BLVDS

The LatticeSC devices support BLVDS standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example**Table 3-2. BLVDS DC Conditions¹****Over Recommended Operating Conditions**

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z _{OUT}	Output impedance	100	100	ohm
R _{TLEFT}	Left end termination	45	90	ohm
R _{TRIGHT}	Right end termination	45	90	ohm
V _{OH}	Output high voltage	1.375	1.48	V
V _{OL}	Output low voltage	1.125	1.02	V
V _{OD}	Output differential voltage	0.25	0.46	V
V _{CM}	Output common mode voltage	1.25	1.25	V
I _{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

Pin Information Summary

Pin Type		256 fpBGA	900 fpBGA		1020 fcBGA	
		LFSC/M15	LFSC/M15	LFSC/M25	LFSC/M25	LFSC/M40
Single Ended User I/O		139	300	378	476	562
Differential Pair User I/O		60	141	182	235	277
LVDS Output Pairs		22	44	60	60	78
Configuration	Dedicated	9	11	11	11	11
	Muxes/MPI sysBus	0	55	55	55	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		2	4	4	4	4
VCC		10	46	46	40	40
VCC12		10	35	35	36	36
VCCAUX		10	36	36	32	32
VCCIO	Bank 1	3	18	18	10	10
	Bank 2	2	14	14	8	8
	Bank 3	2	15	15	10	10
	Bank 4	3	15	15	10	10
	Bank 5	3	15	15	10	10
	Bank 6	2	15	15	10	10
	Bank 7	2	16	16	8	8
VTT	Bank 2	0	2	2	2	2
	Bank 3	0	3	3	3	3
	Bank 4	0	3	3	3	3
	Bank 5	0	3	3	3	3
	Bank 6	0	3	3	3	3
	Bank 7	0	2	2	2	2
GND		26	177	177	134	134
NC		0	102	24	92	6
Single Ended User / Differential I/O per Bank	Bank 1	21/8	63/30	63/30	68/32	68/32
	Bank 2	15/7	26/13	30/15	34/17	54/27
	Bank 3	19/8	43/20	62/29	84/42	94/47
	Bank 4	25/11	50/22	66/32	84/41	99/48
	Bank 5	25/11	49/23	65/32	88/44	99/49
	Bank 6	19/8	43/20	62/29	84/42	94/47
	Bank 7	15/7	26/13	30/15	34/17	54/27
LVDS Output Pairs Per Bank	Bank 2	5	7	9	9	15
	Bank 3	6	15	21	21	24
	Bank 6	6	15	21	21	24
	Bank 7	5	7	9	9	15
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		28	60	60	108	108
Total		256	900	900	1020	1152

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
F14	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
E15	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
E14	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
D9	VCCJ	-	
C16	TDO	-	TDO
B15	TMS	-	
B16	TCK	-	
E13	TDI	-	
C14	PROGRAMN	1	
C15	CCLK	1	
A15	PT43D	1	HDC/SI
A14	PT43C	1	LDCN/SCS
B14	PT41A	1	CS1
E12	PT39B	1	CS0N
D13	PT39A	1	RDN
D12	PT37D	1	WRN
E10	PT37C	1	D7
C11	PT37B	1	D6
D10	PT37A	1	D5
A13	PT36D	1	D4
B12	PT36C	1	D3
A12	PT35B	1	D2
C12	PT35A	1	D1
A11	PT33B	1	D0
B11	PT33A	1	QOUT/CEON
E9	PT32D	1	VREF2_1
E8	PT32B	1	DOUT
D8	PT28C	1	BUSYN/RCLK/SCK
A10	PT27B	1	PCLKC1_0
C10	PT27A	1	PCLKT1_0
E7	PT21C	1	VREF1_1
C9	A_VDDIB3_L	-	
A9	A_HDINP3_L	-	PCS 360 CH 3 IN P
B9	A_HDINN3_L	-	PCS 360 CH 3 IN N
A8	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B8	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
C8	A_VDDOB3_L	-	
B7	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
C7	A_VDDOB2_L	-	
A7	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
B6	A_HDINN2_L	-	PCS 360 CH 2 IN N
A6	A_HDINP2_L	-	PCS 360 CH 2 IN P
C6	A_VDDIB2_L	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF4	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AE5	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AG3	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AH2	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AD6	PB4C	5		PB4C	5	
AJ2	PB5A	5		PB5A	5	
AK2	PB5B	5		PB5B	5	
AD7	PB5C	5		PB5C	5	
AD8	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AH3	PB7A	5		PB11A	5	
AJ3	PB7B	5		PB11B	5	
AF9	PB7C	5		PB11C	5	
AE10	PB7D	5		PB11D	5	
AK3	PB8A	5		PB12A	5	
AJ4	PB8B	5		PB12B	5	
AE11	PB9A	5		PB13A	5	
AF10	PB9B	5		PB13B	5	
AK4	PB11A	5		PB16A	5	
AK5	PB11B	5		PB16B	5	
AH10	PB12A	5	PCLKT5_3	PB20A	5	PCLKT5_3
AH11	PB12B	5	PCLKC5_3	PB20B	5	PCLKC5_3
AF13	PB12C	5	PCLKT5_4	PB20C	5	PCLKT5_4
AE14	PB12D	5	PCLKC5_4	PB20D	5	PCLKC5_4
AK6	PB13A	5	PCLKT5_5	PB21A	5	PCLKT5_5
AK7	PB13B	5	PCLKC5_5	PB21B	5	PCLKC5_5
AF14	PB13C	5		PB21C	5	
AJ11	PB15A	5	PCLKT5_0	PB23A	5	PCLKT5_0
AJ12	PB15B	5	PCLKC5_0	PB23B	5	PCLKC5_0
AH13	PB15D	5	VREF2_5	PB23D	5	VREF2_5
AK8	PB16A	5	PCLKT5_1	PB24A	5	PCLKT5_1
AK9	PB16B	5	PCLKC5_1	PB24B	5	PCLKC5_1
AH14	PB17A	5	PCLKT5_2	PB25A	5	PCLKT5_2
AG14	PB17B	5	PCLKC5_2	PB25B	5	PCLKC5_2
AK10	PB19A	5		PB28A	5	
AK11	PB19B	5		PB28B	5	
AH15	PB20A	5		PB29A	5	
AG15	PB20B	5		PB29B	5	
AH12	PB21A	5		PB31A	5	
AJ13	PB21B	5		PB31B	5	
AD15	PB21C	5		PB31C	5	
AE15	PB21D	5		PB31D	5	
AK12	PB23A	5		PB32A	5	
AK13	PB23B	5		PB32B	5	
AJ14	PB24A	5		PB33A	5	
AJ15	PB24B	5		PB33B	5	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G6	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
A6	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
D6	A_VDDOB2_R	-		A_VDDOB2_R	-	
B6	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
D7	A_VDDOB3_R	-		A_VDDOB3_R	-	
B7	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
A7	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
G7	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
F7	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
H7	A_VDDIB3_R	-		A_VDDIB3_R	-	
H8	B_VDDIB0_R	-		B_VDDIB0_R	-	
F8	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
G8	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
A8	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D8	B_VDDOB0_R	-		B_VDDOB0_R	-	
B8	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D9	B_VDDOB1_R	-		B_VDDOB1_R	-	
B9	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
A9	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
H10	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
G10	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
H9	B_VDDIB1_R	-		B_VDDIB1_R	-	
H11	B_VDDIB2_R	-		B_VDDIB2_R	-	
F11	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
G11	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
A11	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D11	B_VDDOB2_R	-		B_VDDOB2_R	-	
B11	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D12	B_VDDOB3_R	-		B_VDDOB3_R	-	
B12	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
A12	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
G12	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
F12	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
H12	B_VDDIB3_R	-		B_VDDIB3_R	-	
B10	VCC12	-		VCC12	-	
D10	B_REFCLKN_R	-		B_REFCLKN_R	-	
C10	B_REFCLKP_R	-		B_REFCLKP_R	-	
J15	PT49D	1	HDC/SI	PT61D	1	HDC/SI
K15	PT49C	1	LDCN/SCS	PT61C	1	LDCN/SCS
E13	PT49B	1	D8/MPI_DATA8	PT59B	1	D8/MPI_DATA8
F13	PT49A	1	CS1/MPI_CS1	PT59A	1	CS1/MPI_CS1
H13	PT47D	1	D9/MPI_DATA9	PT58D	1	D9/MPI_DATA9
G13	PT47C	1	D10/MPI_DATA10	PT58C	1	D10/MPI_DATA10
E14	PT47B	1	CS0N/MPI_CS0N	PT57B	1	CS0N/MPI_CS0N
F14	PT47A	1	RDN/MPI_STRB_N	PT57A	1	RDN/MPI_STRB_N
H14	PT46D	1	WRN/MPI_WR_N	PT55D	1	WRN/MPI_WR_N
G14	PT46C	1	D7/MPI_DATA7	PT55C	1	D7/MPI_DATA7
D13	PT46B	1	D6/MPI_DATA6	PT55B	1	D6/MPI_DATA6
D14	PT46A	1	D5/MPI_DATA5	PT55A	1	D5/MPI_DATA5
E15	PT45D	1	D4/MPI_DATA4	PT54D	1	D4/MPI_DATA4

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ9	PB78C	4		PB117C	4	
AJ8	PB78D	4		PB117D	4	
AP3	PB79A	4		PB119A	4	
AN3	PB79B	4		PB119B	4	
AF10	PB79C	4		PB119C	4	
AE10	PB79D	4		PB119D	4	
AL7	PB81A	4		PB121A	4	
AL6	PB81B	4		PB121B	4	
AK7	PB81C	4		PB121C	4	
AK6	PB81D	4		PB121D	4	
AN5	PB82A	4		PB123A	4	
AN4	PB82B	4		PB123B	4	
AH9	PB82C	4	VREF1_4	PB123C	4	VREF1_4
AH8	PB82D	4		PB123D	4	
AM3	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB124A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB124B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB83C	4		PB124C	4	
AG8	PB83D	4		PB124D	4	
AN2	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB125A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB125B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB125C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB125D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-		PROBE_VCC	-	
AF8	PROBE_GND	-		PROBE_GND	-	
AG7	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR95D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR95C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AL4	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR95B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR95A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR70D	3		PR94D	3	
AD9	PR70C	3		PR94C	3	
AH4	PR70B	3		PR94B	3	
AJ4	PR70A	3		PR94A	3	
AK5	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR93D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR93C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR69B	3		PR93B	3	
AL1	PR69A	3		PR93A	3	
AH5	PR67D	3		PR91D	3	
AG5	PR67C	3		PR91C	3	
AL2	PR67B	3		PR91B	3	
AK2	PR67A	3		PR91A	3	
AB9	PR66D	3		PR90D	3	
AC9	PR66C	3		PR90C	3	
AH1	PR66B	3		PR90B	3	
AG1	PR66A	3		PR90A	3	
AE8	PR65D	3	VREF2_3	PR89D	3	VREF2_3

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K20	GND	-		GND	-	
K23	GND	-		GND	-	
K26	GND	-		GND	-	
K28	GND	-		GND	-	
K6	GND	-		GND	-	
K9	GND	-		GND	-	
L12	GND	-		GND	-	
L32	GND	-		GND	-	
L4	GND	-		GND	-	
M10	GND	-		GND	-	
M17	GND	-		GND	-	
M24	GND	-		GND	-	
N29	GND	-		GND	-	
N7	GND	-		GND	-	
P15	GND	-		GND	-	
P20	GND	-		GND	-	
P3	GND	-		GND	-	
P31	GND	-		GND	-	
R10	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
T15	GND	-		GND	-	
T17	GND	-		GND	-	
T18	GND	-		GND	-	
T20	GND	-		GND	-	
T28	GND	-		GND	-	
T6	GND	-		GND	-	
U16	GND	-		GND	-	
U19	GND	-		GND	-	
U23	GND	-		GND	-	
U32	GND	-		GND	-	
U4	GND	-		GND	-	
V12	GND	-		GND	-	
V16	GND	-		GND	-	
V19	GND	-		GND	-	
V3	GND	-		GND	-	
V31	GND	-		GND	-	
W15	GND	-		GND	-	
W17	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W29	GND	-		GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J17	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT81B	1	MCA_CLK_P1_OUT
E16	PT81A	1	MCA_CLK_P1_IN
H15	PT78D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT78C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT78B	1	MCA_CLK_P2_OUT
C16	PT78A	1	MCA_CLK_P2_IN
L17	PT75D	1	MCA_DONE_OUT
K17	PT75C	1	BUSYN/RCLK/SCK
E17	PT75B	1	DP0/MPI_PAR0
F17	PT75A	1	MPI_TA
G17	PT73D	1	D23/MPI_DATA23
H17	PT73C	1	DP2/MPI_PAR2
A17	PT73B	1	PCLKC1_0
B17	PT73A	1	PCLKT1_0/MPI_CLK
G18	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT71C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT71B	1	MPI_RETRY
F18	PT71A	1	A0/MPI_ADDR14
J18	PT69D	1	A1/MPI_ADDR15
J19	PT69C	1	A2/MPI_ADDR16
C20	PT69B	1	A3/MPI_ADDR17
C19	PT69A	1	A4/MPI_ADDR18
K18	PT66D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT66C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT66B	1	A5/MPI_ADDR19
E19	PT66A	1	A6/MPI_ADDR20
H19	PT63D	1	D27/MPI_DATA27
H20	PT63C	1	VREF1_1
A18	PT63B	1	A7/MPI_ADDR21
B18	PT63A	1	A8/MPI_ADDR22
H21	PT61D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT61C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT61B	1	A9/MPI_ADDR23
B19	PT61A	1	A10/MPI_ADDR24
H22	PT58D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT58C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT58B	1	A11/MPI_ADDR25
G20	PT58A	1	A12/MPI_ADDR26
K21	PT57D	1	D11/MPI_DATA11
K22	PT57C	1	D12/MPI_DATA12
A20	PT57B	1	A13/MPI_ADDR27
B20	PT57A	1	A14/MPI_ADDR28

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD33	PL59D	6		PL73D	6	
AA38	PL60A	6		PL74A	6	
AB38	PL60B	6		PL74B	6	
AC29	PL60C	6		PL74C	6	
AD29	PL60D	6		PL74D	6	
AA41	PL61A	6		PL75A	6	
AB41	PL61B	6		PL75B	6	
AC34	PL61C	6		PL75C	6	
AD34	PL61D	6		PL75D	6	
AA42	PL63A	6		PL77A	6	
AB42	PL63B	6		PL77B	6	
AC37	PL63C	6		PL77C	6	
AD37	PL63D	6		PL77D	6	
AC38	PL64A	6		PL78A	6	
AD38	PL64B	6		PL78B	6	
AD36	PL64C	6		PL78C	6	
AE36	PL64D	6		PL78D	6	
AC39	PL65A	6		PL79A	6	
AD39	PL65B	6		PL79B	6	
AD35	PL65C	6		PL79C	6	
AE35	PL65D	6		PL79D	6	
AC40	PL67A	6		PL81A	6	
AD40	PL67B	6		PL81B	6	
AE37	PL67C	6		PL81C	6	
AF37	PL67D	6		PL81D	6	
AC41	PL68A	6		PL82A	6	
AD41	PL68B	6		PL82B	6	
AE34	PL68C	6		PL82C	6	
AF34	PL68D	6		PL82D	6	
AC42	PL69A	6		PL83A	6	
AD42	PL69B	6		PL83B	6	
AE33	PL69C	6		PL83C	6	
AF33	PL69D	6		PL83D	6	
AE38	PL72A	6		PL86A	6	
AF38	PL72B	6		PL86B	6	
AE32	PL72C	6		PL86C	6	
AF32	PL72D	6		PL86D	6	
AE41	PL73A	6		PL87A	6	
AF41	PL73B	6		PL87B	6	
AE31	PL73C	6		PL87C	6	
AF31	PL73D	6		PL87D	6	
AE42	PL74A	6		PL88A	6	
AF42	PL74B	6		PL88B	6	
AG37	PL74C	6		PL88C	6	
AH37	PL74D	6		PL88D	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
A26	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N
C34	D_VDDOB2_L	-		D_VDDOB2_L	-	
B26	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P
C32	VCC12	-		VCC12	-	
E27	D_HDINN2_L	-	PCS 363 CH 2 IN N	D_HDINN2_L	-	PCS 363 CH 2 IN N
D27	D_HDINP2_L	-	PCS 363 CH 2 IN P	D_HDINP2_L	-	PCS 363 CH 2 IN P
G25	D_VDDIB2_L	-		D_VDDIB2_L	-	
F29	VCC12	-		VCC12	-	
H26	D_VDDIB1_L	-		D_VDDIB1_L	-	
F30	VCC12	-		VCC12	-	
D28	D_HDINP1_L	-	PCS 363 CH 1 IN P	D_HDINP1_L	-	PCS 363 CH 1 IN P
E28	D_HDINN1_L	-	PCS 363 CH 1 IN N	D_HDINN1_L	-	PCS 363 CH 1 IN N
B27	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P
F36	VCC12	-		VCC12	-	
A27	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N
F35	D_VDDOB1_L	-		D_VDDOB1_L	-	
A28	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N
M30	D_VDDOB0_L	-		D_VDDOB0_L	-	
B28	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P
F37	VCC12	-		VCC12	-	
E29	D_HDINN0_L	-	PCS 363 CH 0 IN N	D_HDINN0_L	-	PCS 363 CH 0 IN N
D29	D_HDINP0_L	-	PCS 363 CH 0 IN P	D_HDINP0_L	-	PCS 363 CH 0 IN P
H27	D_VDDIB0_L	-		D_VDDIB0_L	-	
G28	VCC12	-		VCC12	-	
J28	C_REFCLKP_L	-		C_REFCLKP_L	-	
K28	C_REFCLKN_L	-		C_REFCLKN_L	-	
F32	VCC12	-		VCC12	-	
G29	C_VDDIB3_L	-		C_VDDIB3_L	-	
C31	VCC12	-		VCC12	-	
D30	C_HDINP3_L	-	PCS 362 CH 3 IN P	C_HDINP3_L	-	PCS 362 CH 3 IN P
E30	C_HDINN3_L	-	PCS 362 CH 3 IN N	C_HDINN3_L	-	PCS 362 CH 3 IN N
B29	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P
F38	VCC12	-		VCC12	-	
A29	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N
J33	C_VDDOB3_L	-		C_VDDOB3_L	-	
A30	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N
K33	C_VDDOB2_L	-		C_VDDOB2_L	-	
B30	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P
J34	VCC12	-		VCC12	-	
F31	C_HDINN2_L	-	PCS 362 CH 2 IN N	C_HDINN2_L	-	PCS 362 CH 2 IN N
E31	C_HDINP2_L	-	PCS 362 CH 2 IN P	C_HDINP2_L	-	PCS 362 CH 2 IN P
G30	C_VDDIB2_L	-		C_VDDIB2_L	-	
H28	VCC12	-		VCC12	-	
C37	C_VDDIB1_L	-		C_VDDIB1_L	-	
H30	VCC12	-		VCC12	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AW25	VCCIO5	-		VCCIO5	-	
AW31	VCCIO5	-		VCCIO5	-	
AW37	VCCIO5	-		VCCIO5	-	
AY22	VCCIO5	-		VCCIO5	-	
AY28	VCCIO5	-		VCCIO5	-	
AY34	VCCIO5	-		VCCIO5	-	
AB39	VCCIO6	-		VCCIO6	-	
AC36	VCCIO6	-		VCCIO6	-	
AD32	VCCIO6	-		VCCIO6	-	
AE40	VCCIO6	-		VCCIO6	-	
AF35	VCCIO6	-		VCCIO6	-	
AG31	VCCIO6	-		VCCIO6	-	
AH39	VCCIO6	-		VCCIO6	-	
AJ36	VCCIO6	-		VCCIO6	-	
AK32	VCCIO6	-		VCCIO6	-	
AL40	VCCIO6	-		VCCIO6	-	
AM35	VCCIO6	-		VCCIO6	-	
AP39	VCCIO6	-		VCCIO6	-	
AR36	VCCIO6	-		VCCIO6	-	
AU40	VCCIO6	-		VCCIO6	-	
AA40	VCCIO7	-		VCCIO7	-	
H36	VCCIO7	-		VCCIO7	-	
J40	VCCIO7	-		VCCIO7	-	
L35	VCCIO7	-		VCCIO7	-	
M39	VCCIO7	-		VCCIO7	-	
P36	VCCIO7	-		VCCIO7	-	
R40	VCCIO7	-		VCCIO7	-	
T31	VCCIO7	-		VCCIO7	-	
U35	VCCIO7	-		VCCIO7	-	
V39	VCCIO7	-		VCCIO7	-	
W32	VCCIO7	-		VCCIO7	-	
Y36	VCCIO7	-		VCCIO7	-	
AA14	VTT_2	2		VTT_2	2	
AA15	VTT_2	2		VTT_2	2	
R12	VTT_2	2		VTT_2	2	
V14	VTT_2	2		VTT_2	2	
AB14	VTT_3	3		VTT_3	3	
AB15	VTT_3	3		VTT_3	3	
AE14	VTT_3	3		VTT_3	3	
AJ13	VTT_3	3		VTT_3	3	
AH21	VTT_4	4		VTT_4	4	
AJ18	VTT_4	4		VTT_4	4	
AJ19	VTT_4	4		VTT_4	4	
AJ20	VTT_4	4		VTT_4	4	
AJ21	VTT_4	4		VTT_4	4	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-7FFN1020C ¹	-7	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-6FFN1020C ¹	-6	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-5FFN1020C ¹	-5	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-7FCN1152C ²	-7	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-6FCN1152C ²	-6	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-5FCN1152C ²	-5	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	40.4
LFSC3GA40E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	40.4
LFSC3GA40E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-7FFN1020C ¹	-7	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-6FFN1020C ¹	-6	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-5FFN1020C ¹	-5	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-7FFAN1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-6FFAN1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-5FFAN1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-7FCN1152C ²	-7	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FCN1152C ²	-6	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FCN1152C ²	-5	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-7FFN1152C	-7	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FFN1152C	-6	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FFN1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

For Further Information

For further information about the flexiPCS, see the [LatticeSC/M Family flexiPCS Data Sheet](#).

A variety of technical notes for the LatticeSC/M family are also available on the Lattice Semiconductor website at www.latticesemi.com.

- [LatticeSC PURESPEED I/O Usage Guide](#) (TN1088)
- [LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide](#) (TN1158)
- [LatticeSC sysCLOCK PLL/DLL User's Guide](#) (TN1098)
- [On-Chip Memory Usage Guide for LatticeSC Devices](#) (TN1094)
- [LatticeSC/M DDR/DDR2 SDRAM Memory Interface User's Guide](#) (TN1099)
- [LatticeSC QDRII/II+ SRAM Memory Interface User's Guide](#) (TN1096)
- [LatticeSC sysCONFIG Usage Guide](#) (TN1080)
- [LatticeSC MPI/System Bus](#) (TN1085)
- [SPI Serial Flash Programming Using ispJTAG in LatticeSC Devices](#) (TN1100)
- [Power Estimation and Management for LatticeSC Devices](#) (TN1101)
- [LatticeSC SERDES Jitter](#) (TN1084)
- [LatticeSC FPGAs: Implementing 3.3V Interfaces in 2.5V VCCIO Banks](#) (TN1110)
- [Lattice PCI Express Basic Demo User's Guide](#) (UG08)
- [LatticeSC flexiPCS/SERDES Design Guide](#) (TN1145)
- [Temperature Sensing Diode in LatticeSC Devices](#) (TN1115)
- [SPI4.2 Interoperability Between ORSPI4 and LatticeSC Devices](#) (TN1116)

For further information on Interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- Optical Interface (SPI-4.2, XSBI, CSIX and XGMII): www.oiforum.com
- RAPIDIO: www.rapidio.org
- PCI/PCIX: www.pcisig.com