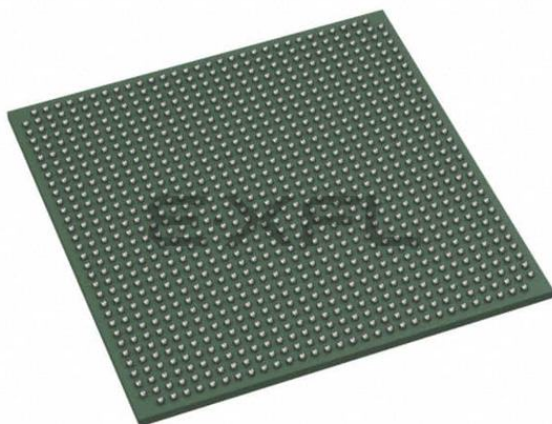




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	562
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga40e-7ffn1020c

Features

■ High Performance FPGA Fabric

- 15K to 115K four input Look-up Tables (LUT4s)
- 139 to 942 I/Os
- 700MHz global clock; 1GHz edge clocks

■ 4 to 32 High Speed SERDES and flexiPCS™ (per Device)

- Performance ranging from 600Mbps to 3.8Gbps
- Excellent Rx jitter tolerance (0.8UI at 3.125Gbps)
- Low Tx jitter (0.25UI typical at 3.125Gbps)
- Built-in Pre-emphasis and equalization
- Low power (typically 105mW per channel)
- Embedded Physical Coding Sublayer (PCS) provides pre-engineered implementation for the following standards:
 - GbE, XAUI, PCI Express, SONET, Serial RapidIO, 1G Fibre Channel, 2G Fibre Channel

■ 2Gbps High Performance PURESPEED™ I/O

- Supports the following performance bandwidths
 - Differential I/O up to 2Gbps DDR (1GHz Clock)
 - Single-ended memory interfaces up to 800Mbps
- 144 Tap programmable Input Delay (INDEL) block on every I/O dynamically aligns data to clock for robust performance
 - Dynamic bit Adaptive Input Logic (AIL) monitoring and control circuitry per pin that automatically ensures proper set-up and hold
 - Dynamic bus: uses control bus from DLL
 - Static per bit
- Electrical standards supported:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2, LVTTTL
 - SSTL 3/2/18 I, II; HSTL 18/15 I, II
 - PCI, PCI-X
 - LVDS, Mini-LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS
- Programmable On Die Termination (ODT)
 - Includes Thevenin Equivalent and low power V_{TT} termination options

■ Memory Intensive FPGA

- sysMEM™ embedded Block RAM

- 1 to 7.8 Mbits memory
- True Dual Port/Pseudo Dual Port/Single Port
- Dedicated FIFO logic for all block RAM
- 500MHz performance
- Additional 240K to 1.8Mbits distributed RAM

■ sysCLOCK™ Network

- Eight analog PLLs per device
 - Frequency range from 15MHz to 1GHz
 - Spread spectrum support
- 12 DLLs per device with direct control of I/O delay
 - Frequency range from 100MHz to 700MHz
- Extensive clocking network
 - 700MHz primary and 325 MHz secondary clocks
 - 1GHz I/O-connected edge clocks
- Precision Clock Divider
 - Phase matched x2 and x4 division of incoming clocks
- Dynamic Clock Select (DCS)
 - Glitch free clock MUX

■ Masked Array for Cost Optimization (MACO™) Blocks

- On-chip structured ASIC Blocks provide pre-engineered IP for low power, low cost system level integration

■ High Performance System Bus

- Ties FPGA elements together with a standard bus framework
 - Connects to peripheral user interfaces for run-time dynamic configuration

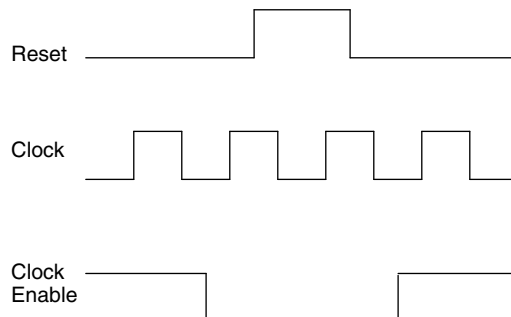
■ System Level Support

- IEEE standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer
- IEEE Standard 1532 in-system configuration
- 1.2V and 1.0V operation
- Onboard oscillator for initialization and general use
- Embedded PowerPC microprocessor interface
- Low cost wire-bond and high pin count flip-chip packaging
- Low cost SPI Flash RAM configuration

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset, as shown in Figure 2-16.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM, FIFO and shift register implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-16. The reset timing rules apply to the RPRreset input vs. the RE input and the RST input vs. the WE and RE inputs. Both RST and RPRreset are always asynchronous EBR inputs. For the EBR shift register mode, the GSR signal is always enabled and the local RESET pin is always asynchronous.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled. For more information about on-chip memory, see TN1094, [On-Chip Memory Usage Guide for LatticeSC Devices](#).

Programmable I/O Cells (PIC)

Each PIC contains four PIOs connected to their respective PURESPEED I/O Buffer which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to PURESPEED I/O buffer, and receives input (DI) from the buffer. The PIO contains advanced capabilities to allow the support of speeds up to 2Gbps. These include dedicated shift and DDR logic and adaptive input logic. The dedicated resources simplify the design of robust interfaces.

Table 2-10. Supported Output Standards⁴

Output Standard	Drive	V _{CCIO} (Nom)	On-chip Output Termination
Single-ended Interfaces			
LVTTL/D ¹	8mA, 16mA, 24mA	3.3	None.
LVC MOS33/D ¹	8mA, 16mA, 24mA	3.3	None
LVC MOS25/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	2.5	None, series: 25, 33, 50, 100
LVC MOS18/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	1.8	None, series: 25, 33, 50, 100
LVC MOS15/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	1.5	None, series: 25, 33, 50, 100
LVC MOS12/D ^{1,2}	2mA, 4mA, 8mA, 12mA	1.2	None, series: 25, 33, 50, 100
PCIX15	N/A	1.5	None
PCI33, PCIX33, AGP1X33, AGP2X33	N/A	3.3	None
HSTL18_I	N/A	1.8	None, series: 50
HSTL18_II	N/A	1.8	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
HSTL15_I	N/A	1.5	None, series: 50
HSTL15_II	N/A	1.5	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
SSTL33_I	N/A	3.3	None
SSTL33_II	N/A	3.3	None
SSTL25_I	N/A	2.5	None, series: 50
SSTL25_II	N/A	2.5	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
SSTL18_I	N/A	1.8	None, series: 33
SSTL18_II	N/A	1.8	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
Differential Interfaces			
SSTL18D_I	N/A	1.8	None, series: 33
SSTL25D_I	N/A	2.5	None, series: 50
SSTL18D_II, SSTL25D_II	N/A	1.2/2.5/3.3	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
SSTL33D_I, II	N/A	3.3	None
HSTL15D_I, HSTL18D_I	N/A	1.5/1.8	None, series: 50
HST15D_II, HSTL18D_II	N/A	1.5/1.8	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
LVDS	2mA, 3.5mA, 4mA, 6mA	N/A	None
Mini-LVDS	3.5mA, 4mA, 6mA	N/A	None
BLVDS25	N/A	N/A	None
MLVDS25	N/A	N/A	None
LVPECL33 ³	N/A	3.3	None
RSDS	2mA, 3.5mA, 4mA, 6mA	N/A	None

1. D refers to open drain capability.

2. User can select either drive current or driver impedances but not both.

3. Emulated with external resistors.

4. No GTL or GTL+ support.

PCI Clamp

A programmable PCI clamp is available on the top and bottom banks of the device. The PCI clamp can be turned “ON” or “OFF” on each pin independently. The PCI clamp is used when implementing a 3.3V PCI interface. The

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.024	-0.106	0.019	-0.004	0.016	0.099	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.074	-0.134	0.08	-0.022	0.088	0.089	ns
LVC MOS18_OD	LVC MOS 1.8 open drain	0.002	-0.206	0	-0.196	-0.002	-0.221	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	-0.344	-0.164	-0.379	-0.186	-0.412	-0.209	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	-0.125	-0.137	-0.145	-0.157	-0.164	-0.176	ns
LVC MOS15_12mA	LVC MOS 1.5 12mA drive	-0.027	-0.166	-0.043	-0.07	-0.059	0.026	ns
LVC MOS15_16mA	LVC MOS 1.5 16mA drive	0.025	-0.195	0.013	-0.089	0.003	0.017	ns
LVC MOS15_OD	LVC MOS 1.5 open drain	-0.047	-0.267	-0.067	-0.267	-0.087	-0.299	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	-0.473	-0.293	-0.505	-0.317	-0.537	-0.34	ns
LVC MOS12_4mA	LVC MOS 1.2 4mA drive	-0.218	-0.239	-0.25	-0.271	-0.28	-0.303	ns
LVC MOS12_8mA	LVC MOS 1.2 8mA drive	-0.109	-0.269	-0.143	-0.181	-0.176	-0.093	ns
LVC MOS12_12mA	LVC MOS 1.2 12mA drive	-0.054	-0.3	-0.085	-0.203	-0.114	-0.106	ns
LVC MOS12_OD	LVC MOS 1.2 open drain	-0.126	-0.371	-0.166	-0.398	-0.204	-0.43	ns
PCI33	PCI	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX33	PCI-X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX15	PCI-X 1.5	0.208	0.227	0.233	0.312	0.259	0.398	ns
AGP1X33	AGP-1X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
AGP2X33	AGP-2X	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns

Figure 3-8. Read Mode with Input and Output Registers

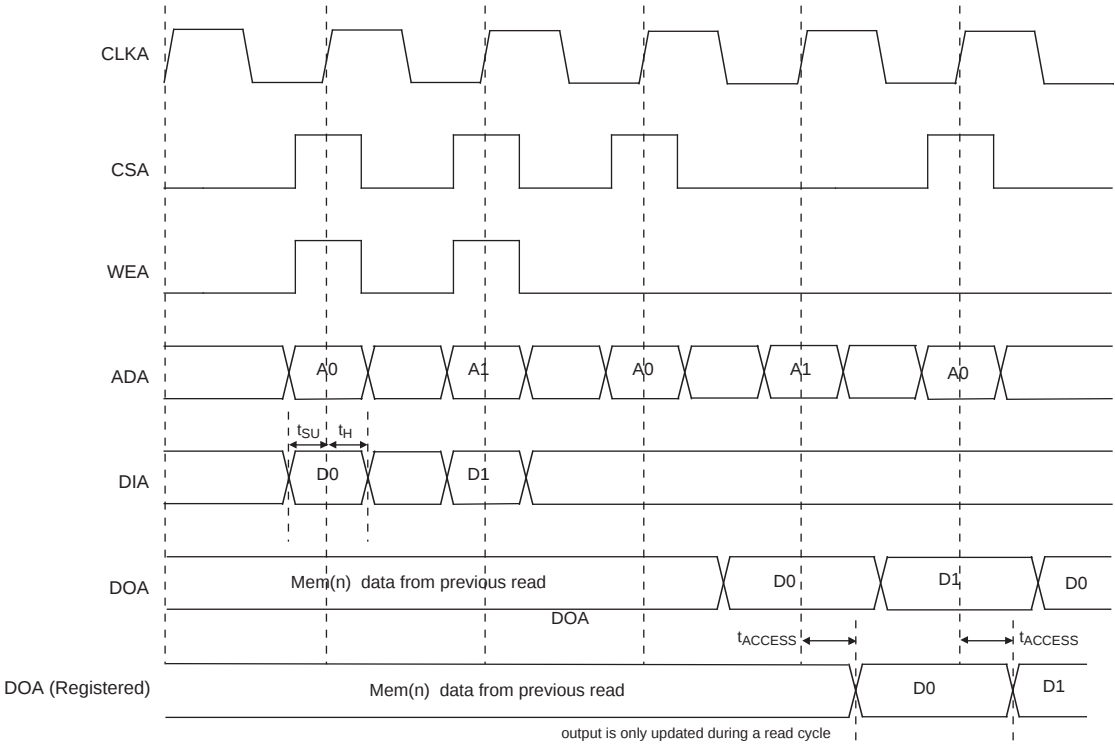
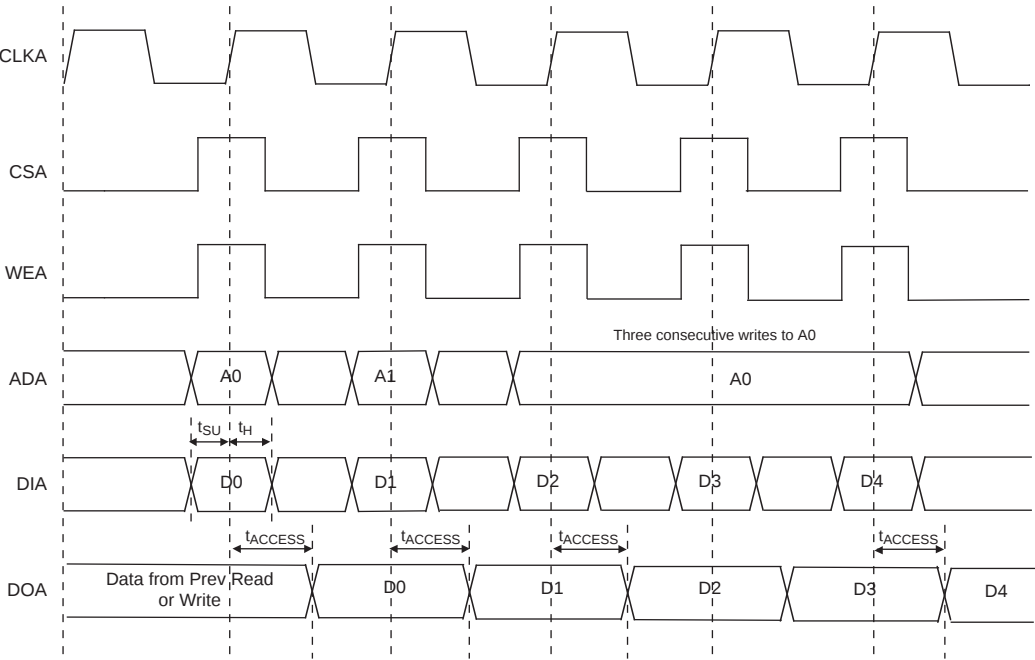


Figure 3-9. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

sysCLOCK DLL Timing**Over Recommended Operating Conditions**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		100	—	700	MHz
f_{OUTOP}	Output Clock Frequency (CLKOP)		100	—	700	MHz
f_{OUTOS}	Output Clock Frequency (CLKOS)		25	—	700	MHz
AC Characteristics						
t_{DUTY}	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, 50% duty cycle input clock, duty cycle correction turned off, time reference delay mode)	38	—	62	%
t_{DUTYRD}	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, arbitrary duty cycle input clock, duty cycle correction turned on, time reference delay mode)	45	—	55	%
$t_{DUTYCIR}$	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, arbitrary duty cycle input clock, duty cycle correction turned on, clock injection removal mode)	40	—	60	%
t_{OPJIT}^1	Output Clock Period Jitter		—	—	200	ps
t_{CPJIT}^1	Output Clock Cycle-to-Cycle Jitter		—	—	200	ps
t_{SKEW}	Output Clock to Clock Skew (Between Two Outputs with the Same Phase Setting)		—	—	100	ps
t_{LOCK}	DLL Lock-in Time		8	—	18500	cycles
t_{IDUTY}	Input Clock Duty Cycle	Applies to all operating conditions	35	—	65	%
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 250	ps
t_{HI}	Input Clock High Time	At 80% level	500	—	—	ps
t_{LO}	Input Clock Low Time	At 20% level	500	—	—	ps
t_{RSWD}	Reset Signal Pulse Width		3	—	—	ns
t_{FDEL}	Timeshift Delay Step Size		35	45	80	ps
t_{DLL}	Delay Through the DLL when No Delay Taps are Chosen but Not in Bypass Mode.		—	760	—	ps

1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
D[n:0]	I/O	In parallel configuration modes, D[7:0] receives configuration data, and each pin is pull-up enabled. For slave serial mode, D0 is the data input. D[7:3] is the output internal status for peripheral mode when RDN is low. D[7:0] is also the first byte of MPI data pins. In MPI configuration mode, MPI selectable data bus width from 8 and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
DP[m:0]	I/O	MPI selectable parity data bus width from 1, 2, and 3-bit DP[0] for D[7:0], DP[1] for D[15:8], and DP[2] for D[23:16].
BUSYN/RCLK/SCK	O	During configuration in peripheral mode, high on BUSYN indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D[7] in asynchronous peripheral mode. During configuration in slave parallel mode, low on BUSYN inhibits the external host from sending new data. The output is used by slave parallel and master serial modes only for decompression. During configuration in master parallel and master byte modes, RCLK is a read clock output signal to an external memory. The RCLK frequency is the same as CCLK when used with uncompressed bit-streams. RCLK will be 1/8 the frequency of CCLK when the bitstream is compressed. During configuration in SPI modes, SCK is generated by the device and connected to the CLK input of the FLASH memory.
MPI Interface (Dedicated pin)		
MPI_IRQ_N	O	MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins.
MPI Interface (User I/O if MPI is not used.)		
MPI_CS0N MPI_CS1	I	MPI chip select pins, active low on MPI_CS0N while active high on MPI_CS1. Both have to be active during the whole transfer data phase. During transfer address phase, both can be inactive so that the decoding for them from address can be slow. If they are active during address phase, one cycle can be saved for sync read.
MPI_CLK	I	This is the PowerPC bus clock. It can be a source of the clock for embedded system bus. If MPI_CLK is used as system bus clock, MPI will be set into sync mode by default. All of the operation on PowerPC side of MPI are synchronized to the rising edge of this clock.
MPI_TSIZE[1:0]	I	Driven by a bus master to indicate the data transfer size for the transaction. 01 for byte, 10 for half-word, and 00 for word.
MPI_WR_N	I	Driven high indicates that a read access is in progress. Driven low indicates that a write access is in process.
MPI_BURST	I	Driven active low indicates that a burst transfer is in progress. Driven high indicates that the current transfer is not a burst.
MPI_BDIP	I	Active low "Burst Data in Process" is driven by a PowerPC processor. Asserted indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2}

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
E4	A_VDDAX25_L	-	
B1	A_REFCLKP_L	-	
C1	A_REFCLKN_L	-	
D2	RESP_ULC	-	
F5	RESETN	1	
D1	DONE	1	
E1	INITN	1	
E2	M0	1	
E3	M1	1	
E5	M2	1	
E6	M3	1	
F2	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
F1	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
F3	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G1	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
G4	PL18D	7	VREF2_7
H3	PL22A	7	
H2	PL22B	7	
H5	PL22C	7	VREF1_7
G5	PL22D	7	DIFFR_7
H1	PL23A	7	PCLKT7_1
J1	PL23B	7	PCLKC7_1
J2	PL24A	7	PCLKT7_0
J3	PL24B	7	PCLKC7_0
H4	PL24C	7	PCLKT7_2
H6	PL24D	7	PCLKC7_2
J4	PL26A	6	PCLKT6_0
K5	PL26B	6	PCLKC6_0
J5	PL26C	6	PCLKT6_1
J6	PL26D	6	PCLKC6_1
K1	PL28A	6	
L1	PL28B	6	
L4	PL28C	6	PCLKT6_2
K4	PL28D	6	PCLKC6_2
L2	PL31C	6	VREF1_6
L3	PL35A	6	
M3	PL35B	6	
M2	PL35D	6	DIFFR_6
M1	PL37A	6	
N1	PL37B	6	
P2	PL41D	6	VREF2_6
M5	PL43A	6	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT37D	1	WRN/MPI_WR_N	PT46D	1	WRN/MPI_WR_N
F18	PT37C	1	D7/MPI_DATA7	PT46C	1	D7/MPI_DATA7
C18	PT37B	1	D6/MPI_DATA6	PT46B	1	D6/MPI_DATA6
C17	PT37A	1	D5/MPI_DATA5	PT46A	1	D5/MPI_DATA5
E17	PT36D	1	D4/MPI_DATA4	PT45D	1	D4/MPI_DATA4
E16	PT36C	1	D3/MPI_DATA3	PT45C	1	D3/MPI_DATA3
G18	PT35B	1	D2/MPI_DATA2	PT45B	1	D2/MPI_DATA2
G17	PT35A	1	D1/MPI_DATA1	PT45A	1	D1/MPI_DATA1
B18	PT33B	1	D0/MPI_DATA0	PT43B	1	D0/MPI_DATA0
B17	PT33A	1	QOUT/CEON	PT43A	1	QOUT/CEON
G16	PT32D	1	VREF2_1	PT42D	1	VREF2_1
A18	PT32B	1	DOUT	PT42B	1	DOUT
A17	PT32A	1	MCA_DONE_IN	PT42A	1	MCA_DONE_IN
H18	PT31B	1	MCA_CLK_P1_OUT	PT41B	1	MCA_CLK_P1_OUT
H17	PT31A	1	MCA_CLK_P1_IN	PT41A	1	MCA_CLK_P1_IN
D17	PT29B	1	MCA_CLK_P2_OUT	PT39B	1	MCA_CLK_P2_OUT
D16	PT29A	1	MCA_CLK_P2_IN	PT39A	1	MCA_CLK_P2_IN
F17	PT28D	1	MCA_DONE_OUT	PT38D	1	MCA_DONE_OUT
F16	PT28C	1	BUSYN/RCLK/SCK	PT38C	1	BUSYN/RCLK/SCK
C16	PT28B	1	DP0/MPI_PAR0	PT38B	1	DP0/MPI_PAR0
C15	PT28A	1	MPI_TA	PT38A	1	MPI_TA
B16	PT27B	1	PCLKC1_0	PT37B	1	PCLKC1_0
B15	PT27A	1	PCLKT1_0/MPI_CLK	PT37A	1	PCLKT1_0/MPI_CLK
H16	PT25D	1	DP3/PCLKC1_4/MPI_PAR3	PT35D	1	DP3/PCLKC1_4/MPI_PAR3
A16	PT25B	1	MPI_RETRY	PT35B	1	MPI_RETRY
A15	PT25A	1	A0/MPI_ADDR14	PT35A	1	A0/MPI_ADDR14
G15	PT24D	1	A1/MPI_ADDR15	PT33D	1	A1/MPI_ADDR15
F15	PT24C	1	A2/MPI_ADDR16	PT33C	1	A2/MPI_ADDR16
E15	PT24B	1	A3/MPI_ADDR17	PT33B	1	A3/MPI_ADDR17
D15	PT24A	1	A4/MPI_ADDR18	PT33A	1	A4/MPI_ADDR18
C14	PT23B	1	A5/MPI_ADDR19	PT32B	1	A5/MPI_ADDR19
C13	PT23A	1	A6/MPI_ADDR20	PT32A	1	A6/MPI_ADDR20
H14	PT21C	1	VREF1_1	PT31C	1	VREF1_1
B14	PT21B	1	A7/MPI_ADDR21	PT31B	1	A7/MPI_ADDR21
B13	PT21A	1	A8/MPI_ADDR22	PT31A	1	A8/MPI_ADDR22
G14	PT20B	1	A9/MPI_ADDR23	PT29B	1	A9/MPI_ADDR23
F14	PT20A	1	A10/MPI_ADDR24	PT29A	1	A10/MPI_ADDR24
A14	PT19B	1	A11/MPI_ADDR25	PT28B	1	A11/MPI_ADDR25
A13	PT19A	1	A12/MPI_ADDR26	PT28A	1	A12/MPI_ADDR26
G13	PT17D	1	D11/MPI_DATA11	PT27D	1	D11/MPI_DATA11
H13	PT17C	1	D12/MPI_DATA12	PT27C	1	D12/MPI_DATA12
E14	PT17B	1	A13/MPI_ADDR27	PT27B	1	A13/MPI_ADDR27
E13	PT17A	1	A14/MPI_ADDR28	PT27A	1	A14/MPI_ADDR28
G12	PT15D	1	A16/MPI_ADDR30	PT25D	1	A16/MPI_ADDR30
G11	PT15C	1	D13/MPI_DATA13	PT25C	1	D13/MPI_DATA13

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W24	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC18	VCCAUX	-		VCCAUX	-	
AC19	VCCAUX	-		VCCAUX	-	
AD17	VCCAUX	-		VCCAUX	-	
AD18	VCCAUX	-		VCCAUX	-	
AD19	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
AC14	VCCAUX	-		VCCAUX	-	
AD12	VCCAUX	-		VCCAUX	-	
AD13	VCCAUX	-		VCCAUX	-	
AD14	VCCAUX	-		VCCAUX	-	
U7	VCCAUX	-		VCCAUX	-	
U8	VCCAUX	-		VCCAUX	-	
V7	VCCAUX	-		VCCAUX	-	
V8	VCCAUX	-		VCCAUX	-	
W7	VCCAUX	-		VCCAUX	-	
W8	VCCAUX	-		VCCAUX	-	
M7	VCCAUX	-		VCCAUX	-	
M8	VCCAUX	-		VCCAUX	-	
N7	VCCAUX	-		VCCAUX	-	
N8	VCCAUX	-		VCCAUX	-	
H10	VCCIO1	-		VCCIO1	-	
H21	VCCIO1	-		VCCIO1	-	
H22	VCCIO1	-		VCCIO1	-	
H9	VCCIO1	-		VCCIO1	-	
J11	VCCIO1	-		VCCIO1	-	
J12	VCCIO1	-		VCCIO1	-	
J13	VCCIO1	-		VCCIO1	-	
J14	VCCIO1	-		VCCIO1	-	
J15	VCCIO1	-		VCCIO1	-	
J16	VCCIO1	-		VCCIO1	-	
J17	VCCIO1	-		VCCIO1	-	
J18	VCCIO1	-		VCCIO1	-	
J19	VCCIO1	-		VCCIO1	-	
J20	VCCIO1	-		VCCIO1	-	
J23	VCCIO2	-		VCCIO2	-	
J24	VCCIO2	-		VCCIO2	-	
K23	VCCIO2	-		VCCIO2	-	
K24	VCCIO2	-		VCCIO2	-	
L22	VCCIO2	-		VCCIO2	-	
L23	VCCIO2	-		VCCIO2	-	
M22	VCCIO2	-		VCCIO2	-	
N22	VCCIO2	-		VCCIO2	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM21	PB29A	5		PB38A	5	
AM20	PB29B	5		PB38B	5	
AH21	PB29C	5		PB38C	5	
AH20	PB29D	5		PB38D	5	
AJ18	PB31A	5		PB39A	5	
AK18	PB31B	5		PB39B	5	
AH19	PB31C	5		PB39C	5	
AH18	PB31D	5		PB39D	5	
AL19	PB32A	5		PB41A	5	
AM19	PB32B	5		PB41B	5	
AH17	PB32C	5		PB41C	5	
AG17	PB32D	5		PB41D	5	
AL18	PB33A	5		PB42A	5	
AM18	PB33B	5		PB42B	5	
AC17	PB33C	5		PB42C	5	
AD17	PB33D	5		PB42D	5	
AL17	PB35A	5		PB43A	5	
AM17	PB35B	5		PB43B	5	
AE17	PB35C	5		PB43C	5	
AF17	PB35D	5		PB43D	5	
AM16	PB37A	4		PB45A	4	
AL16	PB37B	4		PB45B	4	
AF16	PB37C	4		PB45C	4	
AE16	PB37D	4		PB45D	4	
AM15	PB38A	4		PB46A	4	
AL15	PB38B	4		PB46B	4	
AD16	PB38C	4		PB46C	4	
AC16	PB38D	4		PB46D	4	
AM14	PB39A	4		PB47A	4	
AL14	PB39B	4		PB47B	4	
AG16	PB39C	4		PB47C	4	
AH16	PB39D	4		PB47D	4	
AK15	PB41A	4		PB49A	4	
AJ15	PB41B	4		PB49B	4	
AH15	PB41C	4		PB49C	4	
AH14	PB41D	4		PB49D	4	
AM13	PB42A	4		PB50A	4	
AM12	PB42B	4		PB50B	4	
AH13	PB42C	4		PB50C	4	
AH12	PB42D	4		PB50D	4	
AK14	PB43A	4		PB51A	4	
AJ14	PB43B	4		PB51B	4	
AE15	PB43C	4		PB51C	4	
AD15	PB43D	4		PB51D	4	
AL13	PB46A	4	PCLKT4_2	PB53A	4	PCLKT4_2
AL12	PB46B	4	PCLKC4_2	PB53B	4	PCLKC4_2
AG14	PB46C	4	PCLKT4_7	PB53C	4	PCLKT4_7
AG13	PB46D	4	PCLKC4_7	PB53D	4	PCLKC4_7
AM11	PB47A	4	PCLKT4_1	PB54A	4	PCLKT4_1
AM10	PB47B	4	PCLKC4_1	PB54B	4	PCLKC4_1

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ1	PB69A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AK1	PB69B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ2	PB69C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH3	PB69D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AH1	PROBE_VCC	-		PROBE_VCC	-	
AH2	PROBE_GND	-		PROBE_GND	-	
AD9	PR57D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AC10	PR57C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AG2	PR57B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AG1	PR57A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD8	PR56D	3		PR70D	3	
AC9	PR56C	3		PR70C	3	
AF2	PR56B	3		PR70B	3	
AF1	PR56A	3		PR70A	3	
AE6	PR55D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AE7	PR55C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AE1	PR55B	3		PR69B	3	
AE2	PR55A	3		PR69A	3	
AB8	PR53D	3		PR67D	3	
AC8	PR53C	3		PR67C	3	
AE4	PR53B	3		PR67B	3	
AE3	PR53A	3		PR67A	3	
AA10	PR52D	3		PR66D	3	
AA9	PR52C	3		PR66C	3	
AD1	PR52B	3		PR66B	3	
AC1	PR52A	3		PR66A	3	
AC7	PR51D	3	VREF2_3	PR65D	3	VREF2_3
AB7	PR51C	3		PR65C	3	
AD5	PR51B	3		PR65B	3	
AC5	PR51A	3		PR65A	3	
AE5	PR49D	3		PR62D	3	
AF5	PR49C	3		PR62C	3	
AD3	PR49B	3		PR62B	3	
AD4	PR49A	3		PR62A	3	
Y10	PR48D	3		PR61D	3	
Y9	PR48C	3		PR61C	3	
AC2	PR48B	3		PR61B	3	
AD2	PR48A	3		PR61A	3	
AC6	PR47D	3		PR60D	3	
AB6	PR47C	3		PR60C	3	
AA1	PR47B	3		PR60B	3	
AB1	PR47A	3		PR60A	3	
AA5	PR44D	3		PR53D	3	
AB5	PR44C	3		PR53C	3	
Y1	PR44B	3		PR53B	3	
W1	PR44A	3		PR53A	3	
W8	PR43D	3		PR52D	3	
Y7	PR43C	3		PR52C	3	
Y5	PR43B	3		PR52B	3	
W5	PR43A	3		PR52A	3	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K20	GND	-		GND	-	
K23	GND	-		GND	-	
K26	GND	-		GND	-	
K28	GND	-		GND	-	
K6	GND	-		GND	-	
K9	GND	-		GND	-	
L12	GND	-		GND	-	
L32	GND	-		GND	-	
L4	GND	-		GND	-	
M10	GND	-		GND	-	
M17	GND	-		GND	-	
M24	GND	-		GND	-	
N29	GND	-		GND	-	
N7	GND	-		GND	-	
P15	GND	-		GND	-	
P20	GND	-		GND	-	
P3	GND	-		GND	-	
P31	GND	-		GND	-	
R10	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
T15	GND	-		GND	-	
T17	GND	-		GND	-	
T18	GND	-		GND	-	
T20	GND	-		GND	-	
T28	GND	-		GND	-	
T6	GND	-		GND	-	
U16	GND	-		GND	-	
U19	GND	-		GND	-	
U23	GND	-		GND	-	
U32	GND	-		GND	-	
U4	GND	-		GND	-	
V12	GND	-		GND	-	
V16	GND	-		GND	-	
V19	GND	-		GND	-	
V3	GND	-		GND	-	
V31	GND	-		GND	-	
W15	GND	-		GND	-	
W17	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W29	GND	-		GND	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM17	VCCIO4	-		VCCIO4	-	
AM5	VCCIO4	-		VCCIO4	-	
AE20	VCCIO5	-		VCCIO5	-	
AE23	VCCIO5	-		VCCIO5	-	
AE26	VCCIO5	-		VCCIO5	-	
AH22	VCCIO5	-		VCCIO5	-	
AH28	VCCIO5	-		VCCIO5	-	
AJ19	VCCIO5	-		VCCIO5	-	
AJ25	VCCIO5	-		VCCIO5	-	
AL18	VCCIO5	-		VCCIO5	-	
AL24	VCCIO5	-		VCCIO5	-	
AL30	VCCIO5	-		VCCIO5	-	
AM21	VCCIO5	-		VCCIO5	-	
AM27	VCCIO5	-		VCCIO5	-	
AA31	VCCIO6	-		VCCIO6	-	
AB29	VCCIO6	-		VCCIO6	-	
AC24	VCCIO6	-		VCCIO6	-	
AD32	VCCIO6	-		VCCIO6	-	
AE28	VCCIO6	-		VCCIO6	-	
AG31	VCCIO6	-		VCCIO6	-	
AK32	VCCIO6	-		VCCIO6	-	
T29	VCCIO6	-		VCCIO6	-	
U31	VCCIO6	-		VCCIO6	-	
V32	VCCIO6	-		VCCIO6	-	
W28	VCCIO6	-		VCCIO6	-	
Y26	VCCIO6	-		VCCIO6	-	
E31	VCCIO7	-		VCCIO7	-	
G28	VCCIO7	-		VCCIO7	-	
H32	VCCIO7	-		VCCIO7	-	
K29	VCCIO7	-		VCCIO7	-	
L31	VCCIO7	-		VCCIO7	-	
M25	VCCIO7	-		VCCIO7	-	
N28	VCCIO7	-		VCCIO7	-	
P32	VCCIO7	-		VCCIO7	-	
R25	VCCIO7	-		VCCIO7	-	
J25	VCCIO1	-		VCCIO1	-	
N11	VTT_2	2		VTT_2	2	
R12	VTT_2	2		VTT_2	2	
T12	VTT_2	2		VTT_2	2	
AB11	VTT_3	3		VTT_3	3	
W12	VTT_3	3		VTT_3	3	
Y12	VTT_3	3		VTT_3	3	
AC15	VTT_4	4		VTT_4	4	
AC16	VTT_4	4		VTT_4	4	
AD13	VTT_4	4		VTT_4	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP27	PB26A	5	
AP26	PB26B	5	
AK25	PB26C	5	
AK24	PB26D	5	
AN25	PB29A	5	
AN24	PB29B	5	
AE22	PB29C	5	
AE21	PB29D	5	
AM26	PB31A	5	
AM25	PB31B	5	
AF22	PB31C	5	
AF21	PB31D	5	
AN23	PB47A	5	
AN22	PB47B	5	
AP23	PB57A	5	
AP22	PB57B	5	
AG21	PB57C	5	
AG20	PB57D	5	
AP25	PB50A	5	PCLKT5_3
AP24	PB50B	5	PCLKC5_3
AD21	PB50C	5	PCLKT5_4
AD20	PB50D	5	PCLKC5_4
AL23	PB51A	5	PCLKT5_5
AL22	PB51B	5	PCLKC5_5
AH24	PB51C	5	
AH23	PB51D	5	
AM23	PB53A	5	PCLKT5_0
AM22	PB53B	5	PCLKC5_0
AJ24	PB53C	5	
AJ23	PB53D	5	VREF2_5
AN21	PB54A	5	PCLKT5_1
AN20	PB54B	5	PCLKC5_1
AE19	PB54C	5	PCLKT5_6
AD19	PB54D	5	PCLKC5_6
AK21	PB55A	5	PCLKT5_2
AK20	PB55B	5	PCLKC5_2
AK23	PB55C	5	PCLKT5_7
AK22	PB55D	5	PCLKC5_7
AL20	PB58A	5	
AL19	PB58B	5	
AG19	PB58C	5	
AF19	PB58D	5	
AP21	PB61A	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP26	PB41C	5		PB43C	5	
AN26	PB41D	5		PB43D	5	
AY30	PB43A	5		PB45A	5	
AY29	PB43B	5		PB45B	5	
AU30	PB43C	5		PB45C	5	
AU31	PB43D	5		PB45D	5	
AV27	PB44A	5		PB46A	5	
AV26	PB44B	5		PB46B	5	
AT28	PB44C	5		PB46C	5	
AT27	PB44D	5		PB46D	5	
BA29	PB45A	5		PB47A	5	
BA28	PB45B	5		PB47B	5	
AL25	PB45C	5		PB47C	5	
AM25	PB45D	5		PB47D	5	
BB29	PB47A	5		PB49A	5	
BB28	PB47B	5		PB49B	5	
AN25	PB47C	5		PB49C	5	
AP25	PB47D	5		PB49D	5	
AY27	PB48A	5	PCLKT5_3	PB50A	5	PCLKT5_3
AY26	PB48B	5	PCLKC5_3	PB50B	5	PCLKC5_3
AT25	PB48C	5	PCLKT5_4	PB50C	5	PCLKT5_4
AT24	PB48D	5	PCLKC5_4	PB50D	5	PCLKC5_4
AW27	PB49A	5	PCLKT5_5	PB51A	5	PCLKT5_5
AW26	PB49B	5	PCLKC5_5	PB51B	5	PCLKC5_5
AU29	PB49C	5		PB51C	5	
AU28	PB49D	5		PB51D	5	
BB27	PB51A	5	PCLKT5_0	PB53A	5	PCLKT5_0
BB26	PB51B	5	PCLKC5_0	PB53B	5	PCLKC5_0
AR25	PB51C	5		PB53C	5	
AR24	PB51D	5	VREF2_5	PB53D	5	VREF2_5
BA27	PB52A	5	PCLKT5_1	PB54A	5	PCLKT5_1
BA26	PB52B	5	PCLKC5_1	PB54B	5	PCLKC5_1
AP24	PB52C	5	PCLKT5_6	PB54C	5	PCLKT5_6
AN24	PB52D	5	PCLKC5_6	PB54D	5	PCLKC5_6
AV25	PB53A	5	PCLKT5_2	PB55A	5	PCLKT5_2
AV24	PB53B	5	PCLKC5_2	PB55B	5	PCLKC5_2
AU27	PB53C	5	PCLKT5_7	PB55C	5	PCLKT5_7
AU26	PB53D	5	PCLKC5_7	PB55D	5	PCLKC5_7
BA25	PB55A	5		PB57A	5	
BA24	PB55B	5		PB57B	5	
AU24	PB55C	5		PB57C	5	
AU25	PB55D	5		PB57D	5	
BB24	PB56A	5		PB58A	5	
BB25	PB56B	5		PB58B	5	
AM23	PB56C	5		PB58C	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL23	PB56D	5		PB58D	5	
AW24	PB57A	5		PB61A	5	
AW23	PB57B	5		PB61B	5	
AN23	PB57C	5		PB61C	5	
AP23	PB57D	5		PB61D	5	
AY23	PB59A	5		PB63A	5	
AY24	PB59B	5		PB63B	5	
AU23	PB59C	5		PB63C	5	
AU22	PB59D	5		PB63D	5	
AV23	PB60A	5		PB66A	5	
AV22	PB60B	5		PB66B	5	
AM22	PB60C	5		PB66C	5	
AL22	PB60D	5		PB66D	5	
BA23	PB61A	5		PB69A	5	
BA22	PB61B	5		PB69B	5	
AN22	PB61C	5		PB69C	5	
AP22	PB61D	5		PB69D	5	
BB23	PB63A	5		PB71A	5	
BB22	PB63B	5		PB71B	5	
AT22	PB63C	5		PB71C	5	
AR22	PB63D	5		PB71D	5	
BB21	PB65A	4		PB73A	4	
BB20	PB65B	4		PB73B	4	
AR21	PB65C	4		PB73C	4	
AT21	PB65D	4		PB73D	4	
BA21	PB66A	4		PB75A	4	
BA20	PB66B	4		PB75B	4	
AP21	PB66C	4		PB75C	4	
AN21	PB66D	4		PB75D	4	
AV21	PB67A	4		PB78A	4	
AV20	PB67B	4		PB78B	4	
AM21	PB67C	4		PB78C	4	
AL21	PB67D	4		PB78D	4	
AY20	PB69A	4		PB81A	4	
AY19	PB69B	4		PB81B	4	
AU21	PB69C	4		PB81C	4	
AU20	PB69D	4		PB81D	4	
AW20	PB70A	4		PB83A	4	
AW19	PB70B	4		PB83B	4	
AP20	PB70C	4		PB83C	4	
AN20	PB70D	4		PB83D	4	
BB19	PB71A	4		PB86A	4	
BB18	PB71B	4		PB86B	4	
AM20	PB71C	4		PB86C	4	
AL20	PB71D	4		PB86D	4	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

For Further Information

For further information about the flexiPCS, see the [LatticeSC/M Family flexiPCS Data Sheet](#).

A variety of technical notes for the LatticeSC/M family are also available on the Lattice Semiconductor website at www.latticesemi.com.

- [LatticeSC PURESPEED I/O Usage Guide](#) (TN1088)
- [LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide](#) (TN1158)
- [LatticeSC sysCLOCK PLL/DLL User's Guide](#) (TN1098)
- [On-Chip Memory Usage Guide for LatticeSC Devices](#) (TN1094)
- [LatticeSC/M DDR/DDR2 SDRAM Memory Interface User's Guide](#) (TN1099)
- [LatticeSC QDR/II+ SRAM Memory Interface User's Guide](#) (TN1096)
- [LatticeSC sysCONFIG Usage Guide](#) (TN1080)
- [LatticeSC MPI/System Bus](#) (TN1085)
- [SPI Serial Flash Programming Using ispJTAG in LatticeSC Devices](#) (TN1100)
- [Power Estimation and Management for LatticeSC Devices](#) (TN1101)
- [LatticeSC SERDES Jitter](#) (TN1084)
- [LatticeSC FPGAs: Implementing 3.3V Interfaces in 2.5V VCCIO Banks](#) (TN1110)
- [Lattice PCI Express Basic Demo User's Guide](#) (UG08)
- [LatticeSC flexiPCS/SERDES Design Guide](#) (TN1145)
- [Temperature Sensing Diode in LatticeSC Devices](#) (TN1115)
- [SPI4.2 Interoperability Between ORSPI4 and LatticeSC Devices](#) (TN1116)

For further information on Interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- Optical Interface (SPI-4.2, XSBI, CSIX and XGMII): www.oiforum.com
- RAPIDIO: www.rapidio.org
- PCI/PCIX: www.pcisig.com

Date	Version	Section	Change Summary
March 2007 (cont.)	01.5 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Internal Timing Parameters with ispLEVER 6.1 SP1 results.
			Updated t_{FDEL} and t_{CDEL} specifications.
			Updated LatticeSC Family Timing Adders with ispLEVER 6.1 SP1 results.
			Updated PLL specifications to expand frequency range down to 2 MHz and break out jitter for the different ranges.
			Added footnote to sysCLOCK PLL Timing table specifying the conditions for the jitter measurements.
			Added t_{DLL} specification to sysCLOCK DLL Timing table.
			Added footnote to sysCLOCK DLL Timing table specifying the conditions for the jitter measurements.
			Added sysCONFIG Master Parallel Configuration Mode and sysCONFIG SPI Port to LatticeSC sysCONFIG Port Timing table.
		Pin Information	Updated Pin Information Summary with SC40 information.
			Updated LFSC25 Logic Signal Connections: FF1020 with SC40 information.
			Updated LFSC80 Logic Signal Connections: FC1152 with SC40 information.
August 2007	01.6	General	Changed references of "HDC" to "HDC/SI".
			Changed references of "LDCN" to "LDCN/SCS".
			Changed references of "BUSYN/RCLK" to "BUSYN/RCLK/SCK".
			Changed references of "RDCFGN" to "TSALLN".
			Changed references of "TDO/RDDATA" to "TDO".
		Architecture	Updated text in Ripple Mode section.
			Added information to Global Set/Reset.
			Added information for Spread Spectrum Clocking
			Modified information for PLL/DLL Cascading. DLL to PLL is now supported.
			Modified AIL Block text and figure.
			Modified Figure 2-20 DDR/Shift Register Block.
			Added Information to Hot Socketing.
			Added new information for I/O Architecture Rules.
			Added information to SERDES Power Supply Sequencing Requirements.
		DC and Switching Characteristics	Added footnote to Hot Socketing Specifications table.
			Modified Initialization and Standby Supply Current table.
			Modified GSR Timing table.
			Modified sysCLOCK DLL Timing table to include I_{DUTY} .
			Deleted Readback Timing information from sysCONFIG Port Timing table.
			Modified data in External Switching Characteristics table.
		Pin Information	Added information to the Signal Descriptions table for HDC/SI, LDCN/SCS.
			Added footnote to Signal Descriptions table.
			Modified Description for signal BUSYN/RCLK/SCK.
			Modified data in Pin Information Summary and device-specific Pinout Information tables.