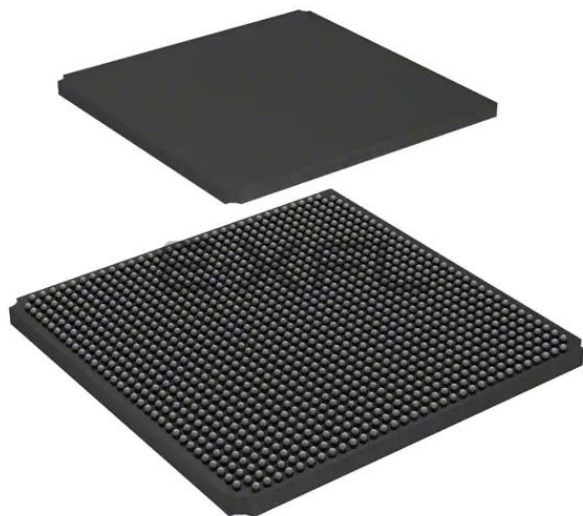




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

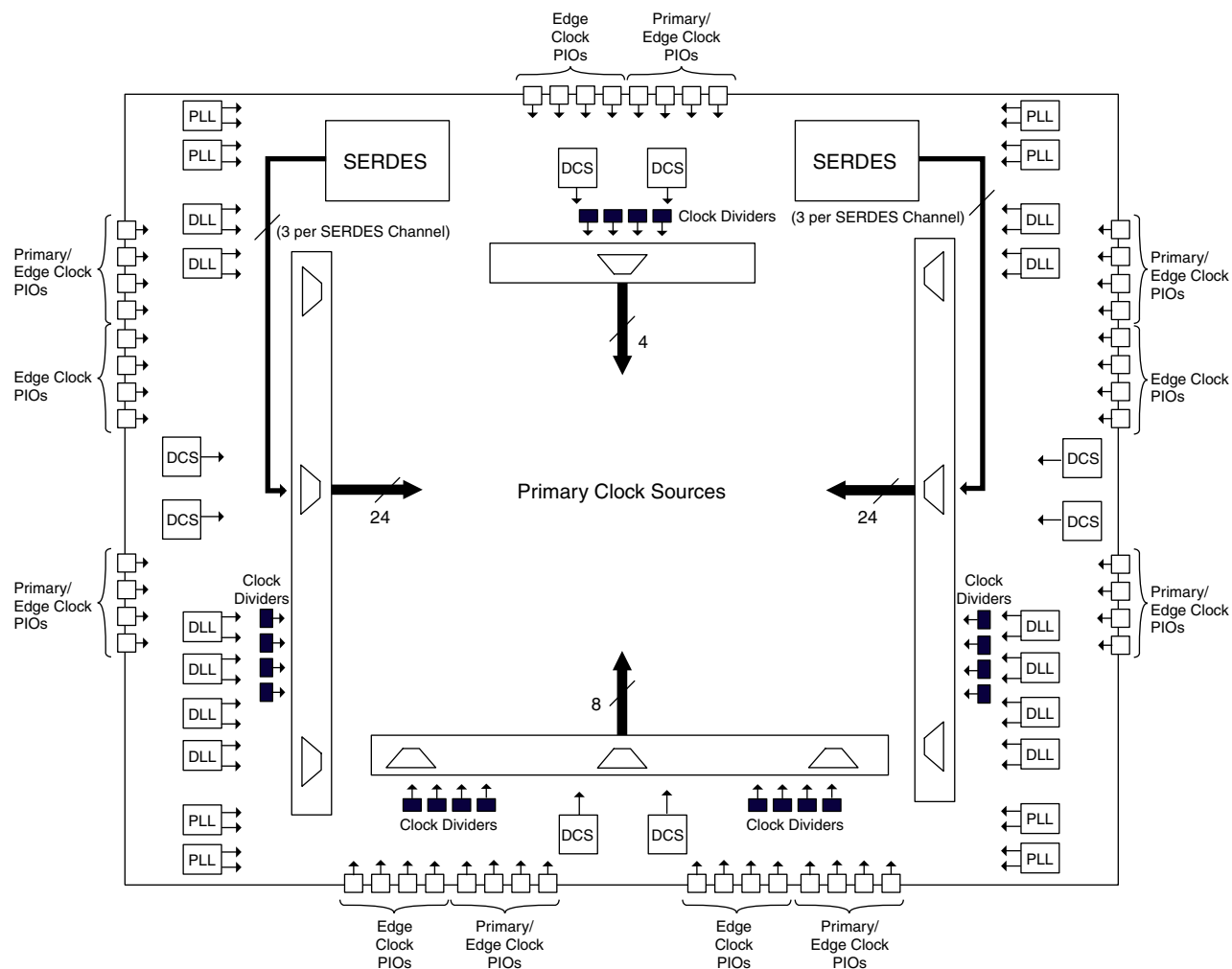
Details

Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-5fcn1152c

- Two outputs per PLL
- Clock divider outputs
- Digital Clock Select (DCS) block outputs
- Three outputs per SERDES quad

Figure 2-5 shows the arrangement of the primary clock sources.

Figure 2-5. Clock Sources



Primary Clock Routing

The clock routing structure in LatticeSC devices consists of 12 Primary Clock lines per quadrant. The primary clocks are generated from 64:1 MUXs located in each quadrant. Three of the inputs to each 64:1 MUX comes from local routing, one is connected to GND and rest of the 60 inputs are from the primary clock sources. Figure 2-6 shows this clock routing.

Table 2-6. Input/Output/Tristate Gearing Resource Rules

PIO	Input/Output Logic			Tri-State/Bidi	
	x1	x2	x4	x1	x2/x4
A	?	?	?	?	N/A
B	?	No I/O Logic	No I/O Logic	?	N/A
C	?	?	No I/O Logic	?	N/A
D	?	No I/O Logic	No I/O Logic	?	N/A

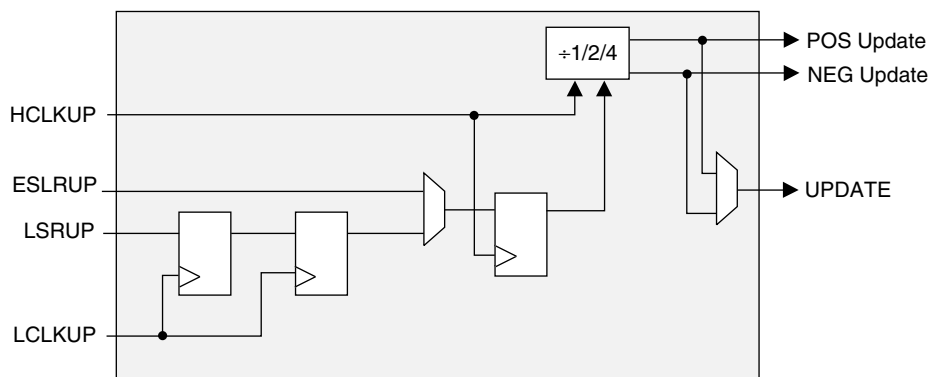
Note: Pin can still be used without I/O logic.

Control Logic Block

The control logic block allows the modification of control signals selected by the routing before they are used in the PIO. It can optionally invert all signals passing through it except the Global Set/Reset. Global Set/Reset can be enabled or disabled. It can route either the edge clock or the clock to the high-speed clock nets. The clock provided to the PIO by routing is used as the slow-speed clocks. In addition this block contains delays that can be inserted in the clock nets to enable Lattice's unique cycle boosting capability.

Update Block

The update block is used to generate the POS update and NEG update signals used by the DDR/Shift register blocks within the PIO. Note the update block is only required in shift modes. This is required in order to do the high speed to low speed handoff. One of these update signals is also selected and output from the PIC as the signal UPDATE. It consists of a shift chain that operates off either the high-speed input or output clock. The values of each register in the chain are set or reset depending on the desired mode of operation. The set/reset signal is generated from either the edge reset ELSR or the local reset LSR. These signals are optionally inverted by the Control Logic Block and provided to the update block as ELSRUP and LSRUP. The Lattice design tools automatically configure and connect the update block when one of the DDR or shift register primitives is used.

Figure 2-25. Update Block

PURESPEED I/O Buffer

Each I/O is associated with a flexible buffer referred to as PURESPEED I/O buffer. These buffers are arranged around the periphery of the device in seven groups referred to as Banks. The PURESPEED I/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL. The availability of programmable on-chip termination for both input and output use, further enhances the utility of these buffers.

Figure 2-26. LatticeSC Banks

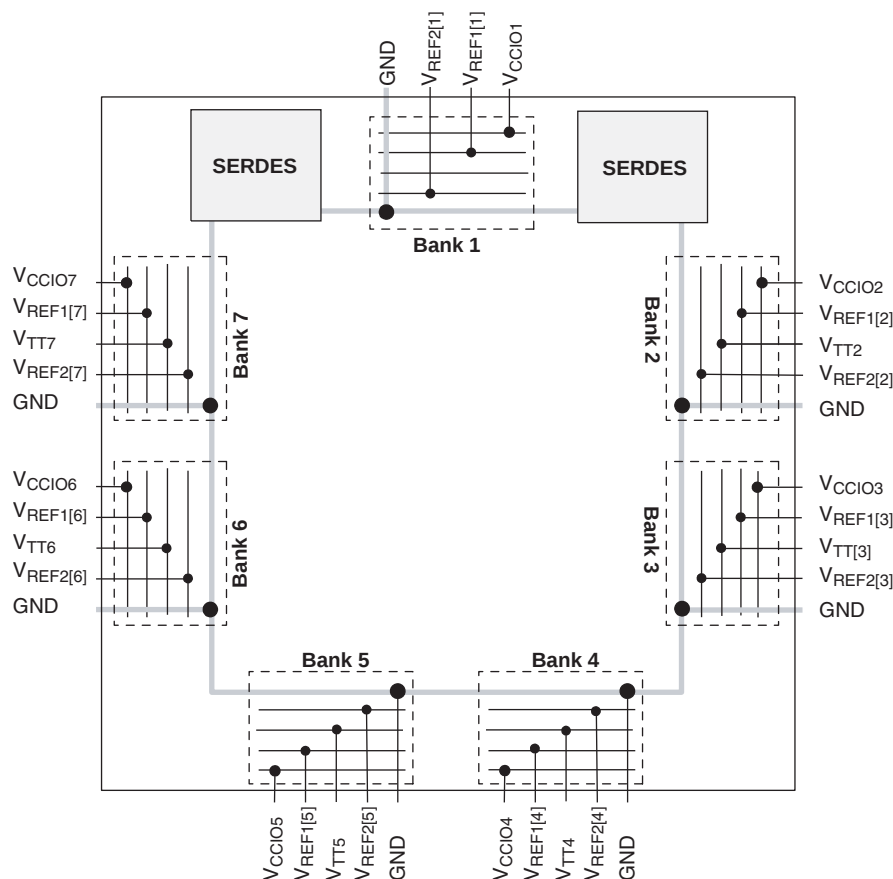


Table 2-7. Maximum Number of I/Os Per Bank in LatticeSC Family

Device	LFSC/M15	LFSC/M25	LFSC/M40	LFSC/M80	LFSC/M115
Bank1	104	80	136	80	136
Bank2	28	36	60	96	136
Bank3	60	84	96	132	156
Bank4	72	100	124	184	208
Bank5	72	100	124	184	208
Bank6	60	84	96	132	156
Bank7	28	36	60	96	136

Note: Not all the I/Os of the Banks are available in all the packages

The LatticeSC devices contain three types of PURESPEED I/O buffers:

1. Left and Right Sides (Banks 2, 3, 6 and 7)

These buffers can support LVCMOS standards up to 2.5V. A differential output driver (for LVDS and RSFS) is provided on all primary PIO pairs (A and B) and differential receivers are available on all pairs. Complimentary drivers are available. Adaptive input logic is available on PIOs A or C.

2. Top Side (Bank 1)

These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but differential drivers for LVDS and RSFS are not available. Adaptive input logic is not available on this side. Complimentary output drivers are available.

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.024	-0.106	0.019	-0.004	0.016	0.099	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.074	-0.134	0.08	-0.022	0.088	0.089	ns
LVC MOS18_OD	LVC MOS 1.8 open drain	0.002	-0.206	0	-0.196	-0.002	-0.221	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	-0.344	-0.164	-0.379	-0.186	-0.412	-0.209	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	-0.125	-0.137	-0.145	-0.157	-0.164	-0.176	ns
LVC MOS15_12mA	LVC MOS 1.5 12mA drive	-0.027	-0.166	-0.043	-0.07	-0.059	0.026	ns
LVC MOS15_16mA	LVC MOS 1.5 16mA drive	0.025	-0.195	0.013	-0.089	0.003	0.017	ns
LVC MOS15_OD	LVC MOS 1.5 open drain	-0.047	-0.267	-0.067	-0.267	-0.087	-0.299	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	-0.473	-0.293	-0.505	-0.317	-0.537	-0.34	ns
LVC MOS12_4mA	LVC MOS 1.2 4mA drive	-0.218	-0.239	-0.25	-0.271	-0.28	-0.303	ns
LVC MOS12_8mA	LVC MOS 1.2 8mA drive	-0.109	-0.269	-0.143	-0.181	-0.176	-0.093	ns
LVC MOS12_12mA	LVC MOS 1.2 12mA drive	-0.054	-0.3	-0.085	-0.203	-0.114	-0.106	ns
LVC MOS12_OD	LVC MOS 1.2 open drain	-0.126	-0.371	-0.166	-0.398	-0.204	-0.43	ns
PCI33	PCI	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX33	PCI-X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX15	PCI-X 1.5	0.208	0.227	0.233	0.312	0.259	0.398	ns
AGP1X33	AGP-1X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
AGP2X33	AGP-2X	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns

LatticeSC/M sysCONFIG Port Timing (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Asynchronous Peripheral Configuration Mode				
t_{WRAP}	WRN, CS0N and CS1 Pulse Width	5	-	ns
t_{SAP}	D[7:0] Setup Time	1.5	-	ns
t_{RDYAP}	RDY Delay	—	8	ns
t_{BAP}	RDY Low	1	8	CCLK periods
t_{WR2AP}	Earliest WRN After RDY Goes High	0	—	ns
t_{DENAP}	RDN to D[7:0] Enable/Disable	—	7.5	ns
t_{DAP}	CCLK to DOUT	—	7.5	ns
sysCONFIG Slave Serial Configuration Mode				
t_{SSS}	DIN Setup Time	5.2	—	ns
t_{HSS}	DIN Hold Time	0	—	ns
t_{CHSS}	CCLK High Time	3.75	—	ns
t_{CLSS}	CCLK Low Time	3.75	—	ns
f_{CSS}	CCLK Frequency	—	150	MHz
t_{DSS}	CCLK to DOUT	—	7.5	ns
sysCONFIG Slave Parallel Configuration Mode				
t_{S1SP}	CS0N, CS1, WRN Setup Time	5.2	—	ns
t_{H1SP}	CS0N, CS1, WRN Hold Time	0	—	ns
t_{S2SP}	D[7:0] Setup Time	5.2	—	ns
t_{H2SP}	D[7:0] Hold Time	0	—	ns
t_{CHSP}	CCLK High Time	3.75	—	ns
t_{CL}	CCLK Low Time	3.75	—	ns
f_{CSP}	CCLK Frequency	—	150	MHz

sysCONFIG MPI Port

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{MPICTRL_SET}$	MPI Control (MPCSTRBN, MPCWRN, MPCCLK, etc.) to MPCCLK Setup Time	4.9	—	5.2	—	5.5	—	ns
t_{MPIADR_SET}	MPI Address to MPCCLK Setup Time	3.9	—	4.2	—	4.5	—	ns
t_{MPIDAT_SET}	MPI Write Data to MPCCLK Setup Time	4.9	—	5.2	—	5.5	—	ns
$t_{MPIDPAR_SET}$	MPI Write Parity Data to MPCCLK Setup Time	3.9	—	4.2	—	4.5	—	ns
t_{MPI_HLD}	All Hold Times	0	—	0	—	0	—	ns
$t_{MPICTRL_DEL}$	MPCCLK to MPI Control (MPCTA, MPC-TEA, MPCRETRY)	—	5.6	—	6.7	—	8.7	ns
t_{MPIDAT_DEL}	MPCCLK to MPI Data	—	5.6	—	6.7	—	8.7	ns
$t_{MPIDPAR_DEL}$	MPCCLK to MPI Parity Data	—	4.9	—	5.7	—	7.7	ns
$f_{MPI_CLK_FRQ}$	MPCCLK Frequency	—	100	—	83	—	66	MHz

Signal Descriptions (Cont.)

Signal Name	I/O	Description
PROBE_GND	—	GND signal - Connected to internal VSS node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.
PLL and Clock Functions (Used as user-programmable I/O pins when not in use for PLL, DLL or clock pins.)		
[LOC]_PLL[T, C]_FB_[A/B]	I	PLL feedback input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the PLL is located in: ULC (upper left), URC (upper right), LLC (lower left) and LRC (lower right). [T, C] indicates whether input is true or complement. [A, B] indicates PLL reference within the corner.
[LOC]_DLL[T, C]_FB_[C, D, E, F]	I	DLL feedback input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the DLL is located in: ULC (upper left), URC (upper right), LLC (lower left) and LRC (lower right). [T/C] indicates whether input is true or complement. [C, D, E, F] indicates DLL reference within a corner. Note: E and F are only available on the lower corners.
[LOC]_PLL[T, C]_IN[A/B]	I	PLL reference clock input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the PLL is located in: ULC (upper left corner), URC (upper right corner), LLC (lower left corner) and LRC (lower right corner). [T, C] indicates whether input is true or complement. [A, B] indicates PLL reference within the corner.
[LOC]_DLL[T, C]_IN[C, D, E, F]		DLL reference clock inputs. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the DLL is located in: ULC (upper left corner), URC (upper right corner), LLC (lower left corner) and LRC (lower right corner). [T/C] indicates whether input is true or complement. [C, D, E, F] indicates DLL reference within a corner. Note: E and F are only available on the lower corners. PCKLxy_[0:3] can drive primary clocks, edge clocks, and CLKDIVs. PCLKxy_[4:7] can only drive edge clocks.
PCLKxy_z		General clock inputs. x indicates whether T (true) or C (complement). y indicates the I/O bank the clock is associated with. z indicates the clock number within a bank.
Test and Programming (Dedicated pins. Pull-up is enabled on input pins during configuration.)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence).
TDO	O	Output pin - Test Data out pin used to shift data out of device using 1149.1.
Configuration Pads (Dedicated pins. Used during sysCONFIG.)		
M[3:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN.
INITN	I/O	Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled that will pull the I/O above 1.5V.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
N12	PB39C	4	
T15	PB40A	4	PCLKT4_3
R16	PB40B	4	PCLKC4_3
L12	PB43A	4	
M12	PB43B	4	
P16	PB44A	4	
N16	PB44B	4	
R14	PB47C	4	VREF1_4
P15	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
M13	PB48B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
N13	PB49A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
P14	PB49B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
M16	PR45B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
L16	PR45A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
M14	PR43B	3	
M15	PR43A	3	
K16	PR41D	3	VREF2_3
J16	PR37B	3	
H16	PR37A	3	
L13	PR35D	3	DIFFR_3
L14	PR35B	3	
L15	PR35A	3	
K12	PR31C	3	VREF1_3
J13	PR28D	3	PCLKC3_2
K13	PR28C	3	PCLKT3_2
H15	PR28B	3	
F16	PR28A	3	
J11	PR26D	3	PCLKC3_1
J12	PR26C	3	PCLKT3_1
J15	PR26B	3	PCLKC3_0
J14	PR26A	3	PCLKT3_0
E16	PR24D	2	PCLKC2_2
D16	PR24C	2	PCLKT2_2
H11	PR24B	2	PCLKC2_0
H12	PR24A	2	PCLKT2_0
H13	PR23B	2	PCLKC2_1
H14	PR23A	2	PCLKT2_1
G12	PR22D	2	DIFFR_2
G13	PR22C	2	VREF1_2
F8	PR22B	2	
F9	PR22A	2	
G16	PR18D	2	VREF2_2
F15	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ1	PB69A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AK1	PB69B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ2	PB69C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH3	PB69D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AH1	PROBE_VCC	-		PROBE_VCC	-	
AH2	PROBE_GND	-		PROBE_GND	-	
AD9	PR57D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AC10	PR57C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AG2	PR57B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AG1	PR57A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD8	PR56D	3		PR70D	3	
AC9	PR56C	3		PR70C	3	
AF2	PR56B	3		PR70B	3	
AF1	PR56A	3		PR70A	3	
AE6	PR55D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AE7	PR55C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AE1	PR55B	3		PR69B	3	
AE2	PR55A	3		PR69A	3	
AB8	PR53D	3		PR67D	3	
AC8	PR53C	3		PR67C	3	
AE4	PR53B	3		PR67B	3	
AE3	PR53A	3		PR67A	3	
AA10	PR52D	3		PR66D	3	
AA9	PR52C	3		PR66C	3	
AD1	PR52B	3		PR66B	3	
AC1	PR52A	3		PR66A	3	
AC7	PR51D	3	VREF2_3	PR65D	3	VREF2_3
AB7	PR51C	3		PR65C	3	
AD5	PR51B	3		PR65B	3	
AC5	PR51A	3		PR65A	3	
AE5	PR49D	3		PR62D	3	
AF5	PR49C	3		PR62C	3	
AD3	PR49B	3		PR62B	3	
AD4	PR49A	3		PR62A	3	
Y10	PR48D	3		PR61D	3	
Y9	PR48C	3		PR61C	3	
AC2	PR48B	3		PR61B	3	
AD2	PR48A	3		PR61A	3	
AC6	PR47D	3		PR60D	3	
AB6	PR47C	3		PR60C	3	
AA1	PR47B	3		PR60B	3	
AB1	PR47A	3		PR60A	3	
AA5	PR44D	3		PR53D	3	
AB5	PR44C	3		PR53C	3	
Y1	PR44B	3		PR53B	3	
W1	PR44A	3		PR53A	3	
W8	PR43D	3		PR52D	3	
Y7	PR43C	3		PR52C	3	
Y5	PR43B	3		PR52B	3	
W5	PR43A	3		PR52A	3	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y6	PR42D	3	DIFFR_3	PR51D	3	DIFFR_3
W6	PR42C	3		PR51C	3	
Y2	PR42B	3		PR51B	3	
W2	PR42A	3		PR51A	3	
W7	PR40D	3		PR49D	3	
V8	PR40C	3		PR49C	3	
W4	PR40B	3		PR49B	3	
W3	PR40A	3		PR49A	3	
V5	PR39D	3		PR48D	3	
U6	PR39C	3		PR48C	3	
V3	PR39B	3		PR48B	3	
V4	PR39A	3		PR48A	3	
V10	PR38D	3		PR47D	3	
V9	PR38C	3		PR47C	3	
V2	PR38B	3		PR47B	3	
V1	PR38A	3		PR47A	3	
U8	PR36D	3		PR45D	3	
U7	PR36C	3		PR45C	3	
U2	PR36B	3		PR45B	3	
U1	PR36A	3		PR45A	3	
U5	PR35D	3		PR44D	3	
T6	PR35C	3		PR44C	3	
T1	PR35B	3		PR44B	3	
T2	PR35A	3		PR44A	3	
U9	PR34D	3		PR43D	3	
U10	PR34C	3	VREF1_3	PR43C	3	VREF1_3
R1	PR34B	3		PR43B	3	
R2	PR34A	3		PR43A	3	
T7	PR31D	3	PCLKC3_2	PR40D	3	PCLKC3_2
T8	PR31C	3	PCLKT3_2	PR40C	3	PCLKT3_2
R4	PR31B	3		PR40B	3	
R3	PR31A	3		PR40A	3	
T5	PR30D	3	PCLKC3_3	PR39D	3	PCLKC3_3
R5	PR30C	3	PCLKT3_3	PR39C	3	PCLKT3_3
P2	PR30B	3		PR39B	3	
P1	PR30A	3		PR39A	3	
T9	PR29D	3	PCLKC3_1	PR38D	3	PCLKC3_1
T10	PR29C	3	PCLKT3_1	PR38C	3	PCLKT3_1
P4	PR29B	3	PCLKC3_0	PR38B	3	PCLKC3_0
P3	PR29A	3	PCLKT3_0	PR38A	3	PCLKT3_0
P5	PR27D	2	PCLKC2_2	PR36D	2	PCLKC2_2
P6	PR27C	2	PCLKT2_2	PR36C	2	PCLKT2_2
N1	PR27B	2	PCLKC2_0	PR36B	2	PCLKC2_0
N2	PR27A	2	PCLKT2_0	PR36A	2	PCLKT2_0
R9	PR26D	2	PCLKC2_3	PR35D	2	PCLKC2_3
R8	PR26C	2	PCLKT2_3	PR35C	2	PCLKT2_3
M1	PR26B	2	PCLKC2_1	PR35B	2	PCLKC2_1
L1	PR26A	2	PCLKT2_1	PR35A	2	PCLKT2_1
N9	PR25D	2	DIFFR_2	PR23D	2	DIFFR_2
M9	PR25C	2	VREF1_2	PR23C	2	VREF1_2

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT24A	1	MPI_TEA	PT30A	1	MPI_TEA
J18	PT23D	1	D14/MPI_DATA14	PT28D	1	D14/MPI_DATA14
K18	PT23C	1	DP1/MPI_PAR1	PT28C	1	DP1/MPI_PAR1
E20	PT23B	1	A21/MPI_BURST	PT27B	1	A21/MPI_BURST
F20	PT23A	1	D15/MPI_DATA15	PT27A	1	D15/MPI_DATA15
C23	B_REFCLKP_L	-		B_REFCLKP_L	-	
D23	B_REFCLKN_L	-		B_REFCLKN_L	-	
B23	VCC12	-		VCC12	-	
H21	B_VDDIB3_L	-		B_VDDIB3_L	-	
F21	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
G21	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D21	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D22	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G22	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
F22	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H22	B_VDDIB2_L	-		B_VDDIB2_L	-	
H24	B_VDDIB1_L	-		B_VDDIB1_L	-	
G23	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
H23	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
A24	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
B24	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-		B_VDDOB1_L	-	
B25	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-		B_VDDOB0_L	-	
A25	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
G25	B_HDINN0_L	-	PCS 361 CH 0 IN N	B_HDINN0_L	-	PCS 361 CH 0 IN N
F25	B_HDINP0_L	-	PCS 361 CH 0 IN P	B_HDINP0_L	-	PCS 361 CH 0 IN P
H25	B_VDDIB0_L	-		B_VDDIB0_L	-	
H26	A_VDDIB3_L	-		A_VDDIB3_L	-	
F26	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
G26	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
D26	A_VDDOB3_L	-		A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
D27	A_VDDOB2_L	-		A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
G27	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
F27	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
H27	A_VDDIB2_L	-		A_VDDIB2_L	-	
F29	A_VDDIB1_L	-		A_VDDIB1_L	-	
G28	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
H28	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A29	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B29	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
D29	A_VDDOB1_L	-		A_VDDOB1_L	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB57D	4		PB79D	4	
AN13	PB58A	4	PCLKT4_3	PB80A	4	PCLKT4_3
AN12	PB58B	4	PCLKC4_3	PB80B	4	PCLKC4_3
AD14	PB58C	4	PCLKT4_4	PB80C	4	PCLKT4_4
AD15	PB58D	4	PCLKC4_4	PB80D	4	PCLKC4_4
AP13	PB61A	4		PB73A	4	
AP12	PB61B	4		PB73B	4	
AK13	PB61C	4		PB73C	4	
AK12	PB61D	4		PB73D	4	
AP11	PB62A	4		PB83A	4	
AP10	PB62B	4		PB83B	4	
AN11	PB63A	4		PB99A	4	
AN10	PB63B	4		PB99B	4	
AF14	PB63C	4		PB99C	4	
AF13	PB63D	4		PB99D	4	
AM10	PB67A	4		PB101A	4	
AM9	PB67B	4		PB101B	4	
AE14	PB67C	4		PB101C	4	
AE13	PB67D	4		PB101D	4	
AP9	PB69A	4		PB104A	4	
AP8	PB69B	4		PB104B	4	
AK11	PB69C	4		PB104C	4	
AK10	PB69D	4		PB104D	4	
AL10	PB70A	4		PB107A	4	
AL9	PB70B	4		PB107B	4	
AF12	PB70C	4		PB107C	4	
AF11	PB70D	4		PB107D	4	
AN9	PB73A	4		PB109A	4	
AN8	PB73B	4		PB109B	4	
AG11	PB73C	4		PB109C	4	
AG10	PB73D	4		PB109D	4	
AP7	PB74A	4		PB111A	4	
AP6	PB74B	4		PB111B	4	
AG13	PB74C	4		PB111C	4	
AG12	PB74D	4		PB111D	4	
AN7	PB75A	4		PB113A	4	
AN6	PB75B	4		PB113B	4	
AK9	PB75C	4		PB113C	4	
AK8	PB75D	4		PB113D	4	
AP5	PB77A	4		PB115A	4	
AP4	PB77B	4		PB115B	4	
AD11	PB77C	4		PB115C	4	
AE11	PB77D	4		PB115D	4	
AM7	PB78A	4		PB117A	4	
AM6	PB78B	4		PB117B	4	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y4	PR48B	3		PR63B	3	
W4	PR48A	3		PR63A	3	
W11	PR47D	3		PR60D	3	
V11	PR47C	3		PR60C	3	
W2	PR47B	3		PR60B	3	
V2	PR47A	3		PR60A	3	
W9	PR45D	3		PR57D	3	
V9	PR45C	3		PR57C	3	
V1	PR45B	3		PR57B	3	
U1	PR45A	3		PR57A	3	
W10	PR44D	3		PR56D	3	
V10	PR44C	3		PR56C	3	
U2	PR44B	3		PR56B	3	
T2	PR44A	3		PR56A	3	
Y8	PR43D	3		PR55D	3	
W8	PR43C	3	VREF1_3	PR55C	3	VREF1_3
W5	PR43B	3		PR55B	3	
V5	PR43A	3		PR55A	3	
V7	PR40D	3	PCLKC3_2	PR52D	3	PCLKC3_2
U7	PR40C	3	PCLKT3_2	PR52C	3	PCLKT3_2
T1	PR40B	3		PR52B	3	
R1	PR40A	3		PR52A	3	
V8	PR39D	3	PCLKC3_3	PR51D	3	PCLKC3_3
U8	PR39C	3	PCLKT3_3	PR51C	3	PCLKT3_3
U5	PR39B	3		PR51B	3	
T5	PR39A	3		PR51A	3	
V6	PR38D	3	PCLKC3_1	PR50D	3	PCLKC3_1
U6	PR38C	3	PCLKT3_1	PR50C	3	PCLKT3_1
T4	PR38B	3	PCLKC3_0	PR50B	3	PCLKC3_0
T3	PR38A	3	PCLKT3_0	PR50A	3	PCLKT3_0
U9	PR36D	2	PCLKC2_2	PR48D	2	PCLKC2_2
T9	PR36C	2	PCLKT2_2	PR48C	2	PCLKT2_2
R2	PR36B	2	PCLKC2_0	PR48B	2	PCLKC2_0
P2	PR36A	2	PCLKT2_0	PR48A	2	PCLKT2_0
T11	PR35D	2	PCLKC2_3	PR47D	2	PCLKC2_3
U11	PR35C	2	PCLKT2_3	PR47C	2	PCLKT2_3
R4	PR35B	2	PCLKC2_1	PR47B	2	PCLKC2_1
R3	PR35A	2	PCLKT2_1	PR47A	2	PCLKT2_1
T8	PR34D	2		PR46D	2	
R8	PR34C	2		PR46C	2	
P1	PR34B	2		PR46B	2	
N1	PR34A	2		PR46A	2	
R6	PR31D	2		PR43D	2	
P6	PR31C	2		PR43C	2	
M1	PR31B	2		PR43B	2	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AC19	VTT_5	5		VTT_5	5	
AC20	VTT_5	5		VTT_5	5	
AD22	VTT_5	5		VTT_5	5	
AB24	VTT_6	6		VTT_6	6	
W23	VTT_6	6		VTT_6	6	
Y23	VTT_6	6		VTT_6	6	
N24	VTT_7	7		VTT_7	7	
R23	VTT_7	7		VTT_7	7	
T23	VTT_7	7		VTT_7	7	
M12	VDDAX25_R	-		VDDAX25_R	-	
M23	VDDAX25_L	-		VDDAX25_L	-	
Y16	GND	-		GND	-	
Y14	GND	-		GND	-	
N21	VCC12	-		VCC12	-	
P22	VCC12	-		VCC12	-	
AA22	VCC12	-		VCC12	-	
AB21	VCC12	-		VCC12	-	
AB14	VCC12	-		VCC12	-	
AA13	VCC12	-		VCC12	-	
P13	VCC12	-		VCC12	-	
N14	VCC12	-		VCC12	-	
G26	NC	-		NC	-	
G9	NC	-		NC	-	
J12	NC	-		NC	-	
H12	NC	-		NC	-	
H23	NC	-		NC	-	
J23	NC	-		NC	-	

1. Differential pair grouping within a PCI is A (True) and B (complement) and C (True) and D (Complement).

2. The LatticeSC/M40 and LatticeSC/M80 in an 1152-pin package support a 32-bit MPI interface.

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
K26	GND	-	
K28	GND	-	
K6	GND	-	
K9	GND	-	
L12	GND	-	
L32	GND	-	
L4	GND	-	
M10	GND	-	
M17	GND	-	
M24	GND	-	
N29	GND	-	
N7	GND	-	
P15	GND	-	
P20	GND	-	
P3	GND	-	
P31	GND	-	
R10	GND	-	
R14	GND	-	
R16	GND	-	
R19	GND	-	
R21	GND	-	
R26	GND	-	
T15	GND	-	
T17	GND	-	
T18	GND	-	
T20	GND	-	
T28	GND	-	
T6	GND	-	
U16	GND	-	
U19	GND	-	
U23	GND	-	
U32	GND	-	
U4	GND	-	
V12	GND	-	
V16	GND	-	
V19	GND	-	
V3	GND	-	
V31	GND	-	
W15	GND	-	
W17	GND	-	
W18	GND	-	
W20	GND	-	
W29	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P38	PL26B	7		PL40B	7	
N35	PL26C	7		PL40C	7	
N36	PL26D	7		PL40D	7	
N39	PL29A	7		PL43A	7	
P39	PL29B	7		PL43B	7	
R34	PL29C	7	VREF1_7	PL43C	7	VREF1_7
T34	PL29D	7	DIFFR_7	PL43D	7	DIFFR_7
L41	PL30A	7		PL44A	7	
M41	PL30B	7		PL44B	7	
W29	PL30C	7		PL44C	7	
Y29	PL30D	7		PL44D	7	
L42	PL31A	7		PL45A	7	
M42	PL31B	7		PL45B	7	
U32	PL31C	7		PL45C	7	
V32	PL31D	7		PL45D	7	
R37	PL33A	7		PL47A	7	
T37	PL33B	7		PL47B	7	
M36	PL33C	7		PL47C	7	
M37	PL33D	7		PL47D	7	
P40	PL34A	7		PL48A	7	
N40	PL34B	7		PL48B	7	
R35	PL34C	7		PL48C	7	
T35	PL34D	7		PL48D	7	
N41	PL35A	7		PL49A	7	
P41	PL35B	7		PL49B	7	
V33	PL35C	7		PL49C	7	
U33	PL35D	7		PL49D	7	
R38	PL37A	7		PL51A	7	
T38	PL37B	7		PL51B	7	
R36	PL37C	7		PL51C	7	
T36	PL37D	7		PL51D	7	
N42	PL38A	7		PL52A	7	
P42	PL38B	7		PL52B	7	
Y31	PL38C	7		PL52C	7	
AA31	PL38D	7		PL52D	7	
U37	PL39A	7		PL53A	7	
V37	PL39B	7		PL53B	7	
U34	PL39C	7		PL53C	7	
V34	PL39D	7		PL53D	7	
U39	PL41A	7		PL55A	7	
T39	PL41B	7		PL55B	7	
V35	PL41C	7		PL55C	7	
W35	PL41D	7		PL55D	7	
R41	PL42A	7		PL56A	7	
T41	PL42B	7		PL56B	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BA19	PB73A	4		PB87A	4	
BA18	PB73B	4		PB87B	4	
AU19	PB73C	4		PB87C	4	
AU18	PB73D	4		PB87D	4	
AV19	PB74A	4	PCLKT4_2	PB89A	4	PCLKT4_2
AV18	PB74B	4	PCLKC4_2	PB89B	4	PCLKC4_2
AN19	PB74C	4	PCLKT4_7	PB89C	4	PCLKT4_7
AP19	PB74D	4	PCLKC4_7	PB89D	4	PCLKC4_7
BB17	PB75A	4	PCLKT4_1	PB90A	4	PCLKT4_1
BB16	PB75B	4	PCLKC4_1	PB90B	4	PCLKC4_1
AT19	PB75C	4	PCLKT4_6	PB90C	4	PCLKT4_6
AT18	PB75D	4	PCLKC4_6	PB90D	4	PCLKC4_6
BA17	PB77A	4	PCLKT4_0	PB91A	4	PCLKT4_0
BA16	PB77B	4	PCLKC4_0	PB91B	4	PCLKC4_0
AR19	PB77C	4	VREF2_4	PB91C	4	VREF2_4
AR18	PB77D	4		PB91D	4	
AY17	PB79A	4	PCLKT4_5	PB93A	4	PCLKT4_5
AY16	PB79B	4	PCLKC4_5	PB93B	4	PCLKC4_5
AN18	PB79C	4		PB93C	4	
AP18	PB79D	4		PB93D	4	
AW17	PB80A	4	PCLKT4_3	PB94A	4	PCLKT4_3
AW16	PB80B	4	PCLKC4_3	PB94B	4	PCLKC4_3
AU17	PB80C	4	PCLKT4_4	PB94C	4	PCLKT4_4
AU16	PB80D	4	PCLKC4_4	PB94D	4	PCLKC4_4
AV17	PB81A	4		PB95A	4	
AV16	PB81B	4		PB95B	4	
AL18	PB81C	4		PB95C	4	
AM18	PB81D	4		PB95D	4	
BB15	PB83A	4		PB97A	4	
BB14	PB83B	4		PB97B	4	
AP17	PB83C	4		PB97C	4	
AN17	PB83D	4		PB97D	4	
BA15	PB84A	4		PB98A	4	
BA14	PB84B	4		PB98B	4	
AT16	PB84C	4		PB98C	4	
AT15	PB84D	4		PB98D	4	
AV15	PB85A	4		PB99A	4	
AV14	PB85B	4		PB99B	4	
AR16	PB85C	4		PB99C	4	
AR15	PB85D	4		PB99D	4	
AY14	PB87A	4		PB101A	4	
AY13	PB87B	4		PB101B	4	
AU15	PB87C	4		PB101C	4	
AU14	PB87D	4		PB101D	4	
BB13	PB88A	4		PB102A	4	

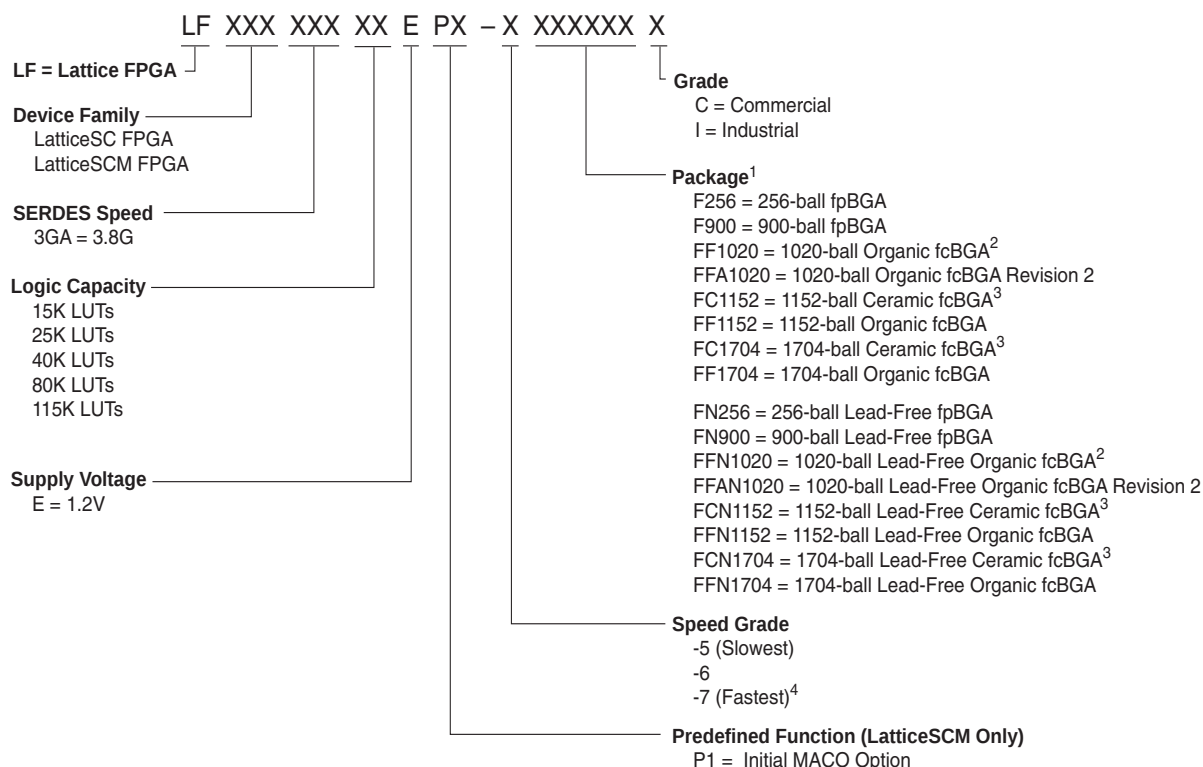
LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB6	PR57D	3		PR71D	3	
AA6	PR57C	3		PR71C	3	
Y2	PR57B	3		PR71B	3	
W2	PR57A	3		PR71A	3	
AB7	PR56D	3		PR70D	3	
AA7	PR56C	3		PR70C	3	
Y3	PR56B	3		PR70B	3	
W3	PR56A	3		PR70A	3	
AC11	PR55D	3		PR69D	3	
AB11	PR55C	3	VREF1_3	PR69C	3	VREF1_3
Y4	PR55B	3		PR69B	3	
W4	PR55A	3		PR69A	3	
AB8	PR52D	3	PCLKC3_2	PR66D	3	PCLKC3_2
AA8	PR52C	3	PCLKT3_2	PR66C	3	PCLKT3_2
Y5	PR52B	3		PR66B	3	
W5	PR52A	3		PR66A	3	
AC12	PR51D	3	PCLKC3_3	PR65D	3	PCLKC3_3
AB12	PR51C	3	PCLKT3_3	PR65C	3	PCLKT3_3
V1	PR51B	3		PR65B	3	
U1	PR51A	3		PR65A	3	
W7	PR50D	3	PCLKC3_1	PR64D	3	PCLKC3_1
V7	PR50C	3	PCLKT3_1	PR64C	3	PCLKT3_1
V2	PR50B	3	PCLKC3_0	PR64B	3	PCLKC3_0
U2	PR50A	3	PCLKT3_0	PR64A	3	PCLKT3_0
AB9	PR48D	2	PCLKC2_2	PR62D	2	PCLKC2_2
AA9	PR48C	2	PCLKT2_2	PR62C	2	PCLKT2_2
T1	PR48B	2	PCLKC2_0	PR62B	2	PCLKC2_0
R1	PR48A	2	PCLKT2_0	PR62A	2	PCLKT2_0
AB10	PR47D	2	PCLKC2_3	PR61D	2	PCLKC2_3
AA10	PR47C	2	PCLKT2_3	PR61C	2	PCLKT2_3
U3	PR47B	2	PCLKC2_1	PR61B	2	PCLKC2_1
T3	PR47A	2	PCLKT2_1	PR61A	2	PCLKT2_1
Y9	PR46D	2		PR60D	2	
W9	PR46C	2		PR60C	2	
V5	PR46B	2		PR60B	2	
U5	PR46A	2		PR60A	2	
AA11	PR43D	2		PR57D	2	
Y11	PR43C	2		PR57C	2	
Y6	PR43B	2		PR57B	2	
W6	PR43A	2		PR57A	2	
Y10	PR42D	2		PR56D	2	
W10	PR42C	2		PR56C	2	
T2	PR42B	2		PR56B	2	
R2	PR42A	2		PR56A	2	
W8	PR41D	2		PR55D	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P

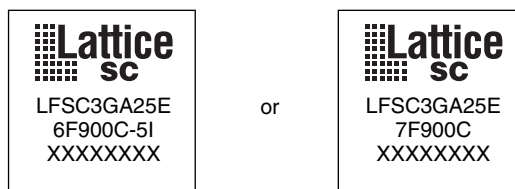
Part Number Description



1. fpBGA = 1.0 mm pitch BGA, fcBGA = 1.0 mm flip-chip BGA (organic and ceramic).
2. Converted to organic fcBGA per PCN #02A-10.
3. Converted to organic fcBGA per PCN #01A-10.
4. Not available in the LatticeSC115 and LatticeSCM115 devices.

Ordering Information

Depending on the speed and temperature grade, the device can either be dual marked or single marked. The commercial grade is one speed grade faster than the associated dual marked industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:



Temperature Grade	Speed Grade	Single or Dual Mark?
Commercial	-7	Either OK
	-6	Dual Only
	-5	Single Only
Industrial	-6	Either OK
	-5	Dual Only

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-6FFN1020I ¹	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-5FFN1020I ¹	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-6FFN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-5FFN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-6FCN1152I ²	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FCN1152I ²	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSC3GA80E-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).