Lattice Semiconductor Corporation - LFSC3GA80E-5FCN1704C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	904
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BCBGA, FCBGA
Supplier Device Package	1704-CFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-5fcn1704c

Table 1-1. LatticeSC Family Selection Guide[1]

Device	SC15	SC25	SC40	SC80	SC115
LUT4s (K)	15	25	40	80	115
sysMEM Blocks (18Kb)	56	104	216	308	424
Embedded Memory (Mbits)	1.03	1.92	3.98	5.68	7.8
Max. Distributed Memory (Mbits)	0.24	0.41	0.65	1.28	1.84
Number of 3.8Gbps SERDES (Max.)	8	16	16	32	32
DLLs	12	12	12	12	12
Analog PLLs	8	8	8	8	8
MACO Blocks	4	6	10	10	12
Package I/O/SERDES Combinations (1mm ball pitch)					
256-ball fpBGA (17 x 17mm)	139/4				
900-ball fpBGA (31 x 31mm)	300/8	378/8			
1020-ball fcBGA (33 x 33mm)[2]		476/16	562/16		
1152-ball fcBGA (35 x 35mm)[3]			604/16	660/16	660/16
1704-ball fcBGA (42.5 x 42.5mm)[3]				904/32	942/32

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per PCN #02A-10.
3. Ceramic fcBGA converted to organic fcBGA per PCN #01A-10.

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

Table 1-2. LatticeSCM Family

Device	SCM15	SCM25	SCM40	SCM80	SCM115
flexiMAC Blocks • 1GbE Mode • 10GbE Mode • PCI Express Mode	1	2	2	2	4
SPI4.2 Blocks	1	2	2	2	2
Memory Controller Blocks • DDR/DDR2 DRAM Mode • QDR II/II+ SRAM Mode • RLDRAM I • RLDRAM II CIO/SIO	1	2	2	2	2
Low-Speed CDR Blocks	0	0	2	2	2
PCI Express LTSSM (PHY) Blocks	1	0	2	2	2

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

Introduction

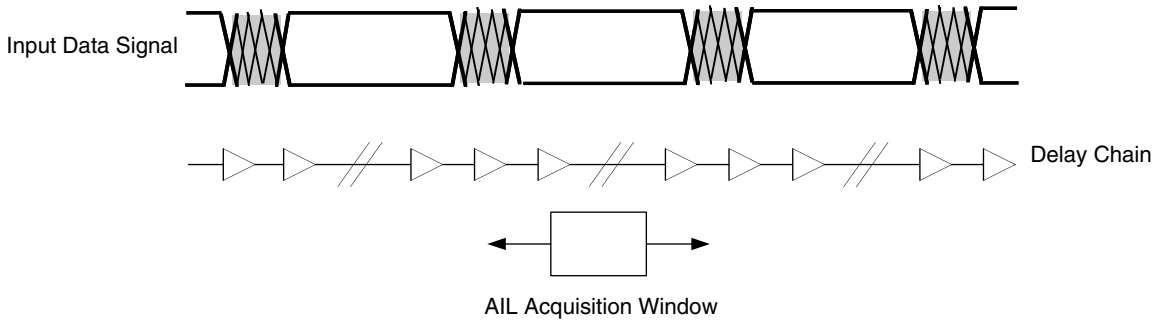
The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

Adaptive Input Logic (AIL) Overview

The Adaptive Input Logic (AIL) provides the ability of the input logic to dynamically find a solution by monitoring multiple samples of the input data. The input data signal from the input buffer is run through a delay chain. Data, transitions, jitter, noise are all contained inside of the delay chain. The AIL will then search the delay chain for a clean sampling point for data. Once found the AIL will monitor and walk with the data dynamically. This novel approach of using a delay chain to create multiple copies of the data provides a lower power solution than oversampling data with a higher speed clock. Figure 2-19 provides a high level view of the AIL methodology.

Figure 2-19. LatticeSC AIL Delay of Input Data Waveform



The AIL slides the acquisition window through the delay chain searching for stable data based solely on data transitions. A specific training pattern is not required to perform this bit alignment, simply data transitions. The size of the acquisition window is user-selectable allowing the AIL to operate over the full range of the PURESPEED I/O range. Based on dynamic user control the AIL can either continuously adjust the window location based on data edge detection or it can be locked to a specific delay.

The AIL operates on single data and double data rate interfaces and is available on most FPGA input pins on the LatticeSC device and all buffer types. The AIL block is low power using only 0.003 mW/MHz typical (6 mW @ 2 Gbps) for PRBS 2^7 data. Multiple AIL inputs can be used to create a bus with a FPGA circuit to realign the bus to a common clock cycle. The FPGA circuit to realign the bus is required and is provided by Lattice as a reference design.

For more information on the LatticeSC AIL please refer to TN1158 LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide.

Input DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer to the low-speed clock domain. It functions as a gearbox allowing high-speed incoming data to be passed into the FPGA fabric. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. The PIOs A and C on the left, right and bottom of the device also contain an optional Adaptive Input Logic (AIL) element. This logic automatically aligns incoming data with the clock allowing for easy design of high-speed interfaces. Figure 2-21 shows a simplified block diagram of the shift register block. The shift block in conjunction with the update and clock divider blocks automatically handles the hand off between the low-speed and high-speed clock domains.

3. **Bottom Side (Banks 4 and 5)**
   These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but true HLVDS and RSDS differential drivers are not available. Adaptive input logic is available on PIOs A or C.

Table 2-8 lists the standards supported by each side.

Table 2-8. I/O Standards Supported by Different Banks

Description	Top Side Banks 1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
I/O Buffer Type	Single-ended, Differential Receiver	Single-ended, Differential Receiver and Driver	Single-ended, Differential Receiver	Single-ended, Differential Receiver and Driver
Output Standards Supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II SSTL33_ I, II HSTL15_I, II, III[1], IV[1] HSTL18_I, II,III[1], IV[1] SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL[2], GTL+[2]	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II HSTL15_I,III HSTL18_I,II,III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL[2], GTL+[2]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II SSTL33_ I, II HSTL15_I, II, III[1], IV[1] HSTL18_I, II,III[1], IV[1] SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL[2], GTL+[2]	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II HSTL15_I,III HSTL18_I,II,III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL[2], GTL+[2]
Input Standards Supported	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Clock Inputs	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Differential Output Support via Emulation	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL
AIL Support	No	Yes	Yes	Yes

1. Input only.
2. Input only. Outputs supported by bussing multiple outputs together.

Supported Standards

The LatticeSC PURESPEED I/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 12, 15, 18, 25 and 33 standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, termination resistance, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL, HSTL, GTL (input only), GTL+ (input only), PCI33, PCIX33, PCIX15, AGP-1X33 and AGP-2X33. Differential standards supported include LVDS, RSDS, BLVDS, MLVDS, LVPECL, differential SSTL and differential HSTL. Tables 12 and 13 show the I/O standards (together with their supply and reference voltages) supported by the LatticeSC devices. The tables also provide the available internal termination schemes. For further information on utilizing the PURESPEED I/O buffer to support a variety of standards please see details of additional technical documentation at the end of this data sheet.

Table 2-10. Supported Output Standards[4]

Output Standard	Drive	V_{CCIO} (Nom)	On-chip Output Termination
Single-ended Interfaces			
LVTTL/D[1]	8mA, 16mA, 24mA	3.3	None.
LVCMOS33/D[1]	8mA, 16mA, 24mA	3.3	None
LVCMOS25/D[1, 2]	4mA, 8mA, 12mA, 16mA,	2.5	None, series: 25, 33, 50, 100
LVCMOS18/D[1, 2]	4mA, 8mA, 12mA, 16mA,	1.8	None, series: 25, 33, 50, 100
LVCMOS15/D[1, 2]	4mA, 8mA, 12mA, 16mA,	1.5	None, series: 25, 33, 50, 100
LVCMOS12/D[1, 2]	2mA, 4mA, 8mA, 12mA	1.2	None, series: 25, 33, 50, 100
PCIX15	N/A	1.5	None
PCI33, PCIX33, AGP1X33, AGP2X33	N/A	3.3	None
HSTL18_I	N/A	1.8	None, series: 50
HSTL18_II	N/A	1.8	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
HSTL15_I	N/A	1.5	None, series: 50
HSTL15_II	N/A	1.5	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
SSTL33_I	N/A	3.3	None
SSTL33_II	N/A	3.3	None
SSTL25_I	N/A	2.5	None, series: 50
SSTL25_II	N/A	2.5	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
SSTL18_ I	N/A	1.8	None, series: 33
SSTL18_II	N/A	1.8	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
Differential Interfaces			
SSTL18D_I	N/A	1.8	None, series: 33
SSTL25D_I	N/A	2.5	None, series: 50
SSTL18D_II, SSTL25D_II	N/A	1.2/2.5/3.3	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
SSTL33D_I, II	N/A	3.3	None
HSTL15D_I, HSTL18D_I	N/A	1.5/1.8	None, series: 50
HST15D_II, HSTL18D_II	N/A	1.5/1.8	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
LVDS	2mA, 3.5mA, 4mA, 6mA	N/A	None
Mini-LVDS	3.5mA, 4mA, 6mA	N/A	None
BLVDS25	N/A	N/A	None
MLVDS25	N/A	N/A	None
LVPECL33[3]	N/A	3.3	None
RSDS	2mA, 3.5mA, 4mA, 6mA	N/A	None

1. D refers to open drain capability.
2. User can select either drive current or driver impedances but not both.
3. Emulated with external resistors.
4. No GTL or GTL+ support.

PCI Clamp

A programmable PCI clamp is available on the top and bottom banks of the device. The PCI clamp can be turned “ON” or “OFF” on each pin independently. The PCI clamp is used when implementing a 3.3V PCI interface. The

Signal Descriptions (Cont.)

Signal Name	I/O	Description
MPI_STRBN	I	Driven active low indicates the start of a transaction on the PowerPC bus. MPI will strobe the address bus at next rising edge of clock.
MPI_ADDR[31:14]	I	Address bus driven by a PowerPC bus master. Only 18-bit width is needed. It has to be the least significant bit of the PowerPC 32-bit address A[31:14].
MPI_DAT[n:0]	I/O	Selectable data bus width from 8, and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
MPI_PAR[m:0]	I/O	Selectable parity bus width from 1, 2, and 3-bit. MPI_DP[0] for MPI_D[7:0], MPI_DP[1] for MPI_D[15:8] and MPI_DP[2] for MPI_D[23:16].
MPI_TA	O	Transfer acknowledge. Driven active low indicates that MPI received the data on the write cycle or returned data on the read cycle.
MPI_TEA	O	Transfer Error Acknowledge. Driven active low indicates that MPI detects a bus error on the internal system bus for current transaction.
MPI_RETRY	O	Active low MPI Retry requests the MPC860 to relinquish the bus and retry the cycle.
Multi-chip Alignment (User I/O if not used.)		
MCA_DONE_OUT	O	Multi-chip alignment done output (to second MCA chip)
MCA_DONE_IN	I	Multi-chip alignment done input (from second MCA chip)
MCA_CLK_P[1:2]_OUT	O	Multi-chip alignment clock [1:2] output (sourced by MCA master chip)
MCA_CLK_P[1:2]_IN	I	Multi-chip alignment clock [1:2] input (from MCA master chip
TEMP	—	Temperature sensing diode pin. Dedicated pin. Accuracy is typically +/- 10°C.
Miscellaneous Dedicated Pins		
XRES	—	External reference resistor between this pin and ground. The reference resistor is used to calibrate the programmable terminating resistors used in the I/Os. Dedicated pin. Value: 1K ± 1% ohm.
DIFFRx	—	Only used if a differential driver is used in a bank. This DIFFRx must be connected to ground via an external 1K ±1% ohm resistor for all banks that have a differential driver.
SERDES Block (Dedicated Pins)		
[A:D]_HDINPx_[L/R]	I	High-speed input (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDINNx_[L/R]	I	High-speed input (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTPx_[L/R]	O	High-speed output (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTNx_[L/R]	O	High-speed output (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_REFCLKP_[L/R]	I	Ref clock input (positive), aux channel on left [L] or right [R] side of device.
[A:D]_REFCLKN_[L/R]	I	Ref clock input (negative), aux channel on left [L] or right [R] side of device.

Pin Information Summary

Pin Type		256 fpBGA	900 fpBGA		1020 fcBGA	
		LFSC/M15	LFSC/M15	LFSC/M25	LFSC/M25	LFSC/M40
Single Ended User I/O		139	300	378	476	562
Differential Pair User I/O		60	141	182	235	277
LVDS Output Pairs		22	44	60	60	78
Configuration	Dedicated	9	11	11	11	11
	Muxes/MPI sysBus	0	55	55	55	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		2	4	4	4	4
VCC		10	46	46	40	40
VCC12		10	35	35	36	36
VCCAUX		10	36	36	32	32
VCCIO	Bank 1	3	18	18	10	10
	Bank 2	2	14	14	8	8
	Bank 3	2	15	15	10	10
	Bank 4	3	15	15	10	10
	Bank 5	3	15	15	10	10
	Bank 6	2	15	15	10	10
	Bank 7	2	16	16	8	8
VTT	Bank 2	0	2	2	2	2
	Bank 3	0	3	3	3	3
	Bank 4	0	3	3	3	3
	Bank 5	0	3	3	3	3
	Bank 6	0	3	3	3	3
	Bank 7	0	2	2	2	2
GND		26	177	177	134	134
NC		0	102	24	92	6
Single Ended User / Differential I/O per Bank	Bank 1	21/8	63/30	63/30	68/32	68/32
	Bank 2	15/7	26/13	30/15	34/17	54/27
	Bank 3	19/8	43/20	62/29	84/42	94/47
	Bank 4	25/11	50/22	66/32	84/41	99/48
	Bank 5	25/11	49/23	65/32	88/44	99/49
	Bank 6	19/8	43/20	62/29	84/42	94/47
	Bank 7	15/7	26/13	30/15	34/17	54/27
LVDS Output Pairs Per Bank	Bank 2	5	7	9	9	15
	Bank 3	6	15	21	21	24
	Bank 6	6	15	21	21	24
	Bank 7	5	7	9	9	15
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		28	60	60	108	108
Total		256	900	900	1020	1152

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
F14	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
E15	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
E14	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
D9	VCCJ	-	
C16	TDO	-	TDO
B15	TMS	-	
B16	TCK	-	
E13	TDI	-	
C14	PROGRAMN	1	
C15	CCLK	1	
A15	PT43D	1	HDC/SI
A14	PT43C	1	LDCN/SCS
B14	PT41A	1	CS1
E12	PT39B	1	CS0N
D13	PT39A	1	RDN
D12	PT37D	1	WRN
E10	PT37C	1	D7
C11	PT37B	1	D6
D10	PT37A	1	D5
A13	PT36D	1	D4
B12	PT36C	1	D3
A12	PT35B	1	D2
C12	PT35A	1	D1
A11	PT33B	1	D0
B11	PT33A	1	QOUT/CEON
E9	PT32D	1	VREF2_1
E8	PT32B	1	DOUT
D8	PT28C	1	BUSYN/RCLK/SCK
A10	PT27B	1	PCLKC1_0
C10	PT27A	1	PCLKT1_0
E7	PT21C	1	VREF1_1
C9	A_VDDIB3_L	-	
A9	A_HDINP3_L	-	PCS 360 CH 3 IN P
B9	A_HDINN3_L	-	PCS 360 CH 3 IN N
A8	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B8	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
C8	A_VDDOB3_L	-	
B7	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
C7	A_VDDOB2_L	-	
A7	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
B6	A_HDINN2_L	-	PCS 360 CH 2 IN N
A6	A_HDINP2_L	-	PCS 360 CH 2 IN P
C6	A_VDDIB2_L	-	

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
C5	A_VDDIB1_L	-	
A5	A_HDINP1_L	-	PCS 360 CH 1 IN P
B5	A_HDINN1_L	-	PCS 360 CH 1 IN N
A4	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B4	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
C4	A_VDDOB1_L	-	
B3	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
C3	A_VDDOB0_L	-	
A3	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
B2	A_HDINN0_L	-	PCS 360 CH 0 IN N
A2	A_HDINP0_L	-	PCS 360 CH 0 IN P
C2	A_VDDIB0_L	-	
A1	GND	-	
A16	GND	-	
B10	GND	-	
C13	GND	-	
D15	GND	-	
D3	GND	-	
E11	GND	-	
F13	GND	-	
G14	GND	-	
G2	GND	-	
G8	GND	-	
H10	GND	-	
J7	GND	-	
K15	GND	-	
K3	GND	-	
K9	GND	-	
M6	GND	-	
N11	GND	-	
N14	GND	-	
N2	GND	-	
P10	GND	-	
P4	GND	-	
R13	GND	-	
R7	GND	-	
G10	VCC	-	
G7	VCC	-	
G9	VCC	-	
H7	VCC	-	
H8	VCC	-	
H9	VCC	-	
J10	VCC	-	
J8	VCC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2]

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C28	A_REFCLKP_L	-		A_REFCLKP_L	-	
D28	A_REFCLKN_L	-		A_REFCLKN_L	-	
B28	VCC12	-		VCC12	-	
F28	RESP_ULC	-		RESP_ULC	-	
J21	RESETN	1		RESETN	1	
J20	TSALLN	1		TSALLN	1	
K20	DONE	1		DONE	1	
K21	INITN	1		INITN	1	
K23	M0	1		M0	1	
J23	M1	1		M1	1	
J24	M2	1		M2	1	
K24	M3	1		M3	1	
K25	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J25	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
K26	PL16C	7		PL16C	7	
K27	PL16D	7		PL16D	7	
D32	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
D31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
M23	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
N23	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
E32	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E31	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
J28	PL18C	7		PL18C	7	
K28	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F32	PL20A	7		PL21A	7	
F31	PL20B	7		PL21B	7	
L25	PL20C	7		PL21C	7	
L26	PL20D	7		PL21D	7	
G31	PL21A	7		PL22A	7	
G32	PL21B	7		PL22B	7	
J29	PL22A	7		PL25A	7	
H29	PL22B	7		PL25B	7	
M25	PL22C	7		PL25C	7	
N25	PL22D	7		PL25D	7	
H31	PL25A	7		PL23A	7	
H32	PL25B	7		PL23B	7	
M24	PL25C	7	VREF1_7	PL23C	7	VREF1_7
N24	PL25D	7	DIFFR_7	PL23D	7	DIFFR_7
L32	PL26A	7	PCLKT7_1	PL35A	7	PCLKT7_1
M32	PL26B	7	PCLKC7_1	PL35B	7	PCLKC7_1
R25	PL26C	7	PCLKT7_3	PL35C	7	PCLKT7_3
R24	PL26D	7	PCLKC7_3	PL35D	7	PCLKC7_3
N31	PL27A	7	PCLKT7_0	PL36A	7	PCLKT7_0
N32	PL27B	7	PCLKC7_0	PL36B	7	PCLKC7_0
P27	PL27C	7	PCLKT7_2	PL36C	7	PCLKT7_2
P28	PL27D	7	PCLKC7_2	PL36D	7	PCLKC7_2
P30	PL29A	6	PCLKT6_0	PL38A	6	PCLKT6_0
P29	PL29B	6	PCLKC6_0	PL38B	6	PCLKC6_0
T23	PL29C	6	PCLKT6_1	PL38C	6	PCLKT6_1
T24	PL29D	6	PCLKC6_1	PL38D	6	PCLKC6_1

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG18	PB42C	5		PB61C	5	
AF18	PB42D	5		PB61D	5	
AP19	PB43A	5		PB63A	5	
AP18	PB43B	5		PB63B	5	
AJ18	PB43C	5		PB63C	5	
AH18	PB43D	5		PB63D	5	
AP17	PB45A	4		PB65A	4	
AP16	PB45B	4		PB65B	4	
AJ17	PB45C	4		PB65C	4	
AH17	PB45D	4		PB65D	4	
AN17	PB46A	4		PB66A	4	
AN16	PB46B	4		PB66B	4	
AE17	PB46C	4		PB66C	4	
AD17	PB46D	4		PB66D	4	
AK17	PB47A	4		PB67A	4	
AK16	PB47B	4		PB67B	4	
AG17	PB47C	4		PB67C	4	
AF17	PB47D	4		PB67D	4	
AM16	PB49A	4		PB69A	4	
AM15	PB49B	4		PB69B	4	
AJ15	PB49C	4		PB69C	4	
AJ14	PB49D	4		PB69D	4	
AL16	PB50A	4		PB70A	4	
AL15	PB50B	4		PB70B	4	
AG16	PB50C	4		PB70C	4	
AF16	PB50D	4		PB70D	4	
AP15	PB51A	4		PB71A	4	
AP14	PB51B	4		PB71B	4	
AH15	PB51C	4		PB71C	4	
AH14	PB51D	4		PB71D	4	
AN15	PB53A	4	PCLKT4_2	PB74A	4	PCLKT4_2
AN14	PB53B	4	PCLKC4_2	PB74B	4	PCLKC4_2
AE16	PB53C	4	PCLKT4_7	PB74C	4	PCLKT4_7
AD16	PB53D	4	PCLKC4_7	PB74D	4	PCLKC4_7
AK15	PB54A	4	PCLKT4_1	PB75A	4	PCLKT4_1
AK14	PB54B	4	PCLKC4_1	PB75B	4	PCLKC4_1
AG15	PB54C	4	PCLKT4_6	PB75C	4	PCLKT4_6
AG14	PB54D	4	PCLKC4_6	PB75D	4	PCLKC4_6
AM13	PB55A	4	PCLKT4_0	PB77A	4	PCLKT4_0
AM12	PB55B	4	PCLKC4_0	PB77B	4	PCLKC4_0
AJ12	PB55C	4	VREF2_4	PB77C	4	VREF2_4
AJ11	PB55D	4		PB77D	4	
AL13	PB57A	4	PCLKT4_5	PB79A	4	PCLKT4_5
AL12	PB57B	4	PCLKC4_5	PB79B	4	PCLKC4_5
AH12	PB57C	4		PB79C	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AJ34	PL98A	6	
AK34	PL98B	6	
AB27	PL98C	6	
AC27	PL98D	6	
AF33	PL99A	6	
AG33	PL99B	6	
AC29	PL99C	6	
AD29	PL99D	6	
AE31	PL103A	6	
AF31	PL103B	6	
AF30	PL103C	6	
AF29	PL103D	6	
AH33	PL104A	6	
AJ33	PL104B	6	
AC28	PL104C	6	
AD28	PL104D	6	
AH32	PL107A	6	
AJ32	PL107B	6	
AD27	PL107C	6	
AE27	PL107D	6	VREF2_6
AG34	PL109A	6	
AH34	PL109B	6	
AC26	PL109C	6	
AB26	PL109D	6	
AK33	PL112A	6	
AL33	PL112B	6	
AG30	PL112C	6	
AH30	PL112D	6	
AL34	PL115A	6	
AM34	PL115B	6	
AJ30	PL115C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL115D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL116A	6	
AH31	PL116B	6	
AD26	PL116C	6	
AD25	PL116D	6	
AL32	PL117A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL117B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL117C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL117D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-	
AF27	TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP27	PB26A	5	
AP26	PB26B	5	
AK25	PB26C	5	
AK24	PB26D	5	
AN25	PB29A	5	
AN24	PB29B	5	
AE22	PB29C	5	
AE21	PB29D	5	
AM26	PB31A	5	
AM25	PB31B	5	
AF22	PB31C	5	
AF21	PB31D	5	
AN23	PB47A	5	
AN22	PB47B	5	
AP23	PB57A	5	
AP22	PB57B	5	
AG21	PB57C	5	
AG20	PB57D	5	
AP25	PB50A	5	PCLKT5_3
AP24	PB50B	5	PCLKC5_3
AD21	PB50C	5	PCLKT5_4
AD20	PB50D	5	PCLKC5_4
AL23	PB51A	5	PCLKT5_5
AL22	PB51B	5	PCLKC5_5
AH24	PB51C	5	
AH23	PB51D	5	
AM23	PB53A	5	PCLKT5_0
AM22	PB53B	5	PCLKC5_0
AJ24	PB53C	5	
AJ23	PB53D	5	VREF2_5
AN21	PB54A	5	PCLKT5_1
AN20	PB54B	5	PCLKC5_1
AE19	PB54C	5	PCLKT5_6
AD19	PB54D	5	PCLKC5_6
AK21	PB55A	5	PCLKT5_2
AK20	PB55B	5	PCLKC5_2
AK23	PB55C	5	PCLKT5_7
AK22	PB55D	5	PCLKC5_7
AL20	PB58A	5	
AL19	PB58B	5	
AG19	PB58C	5	
AF19	PB58D	5	
AP21	PB61A	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2]

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G34	A_REFCLKP_L	-		A_REFCLKP_L	-	
H34	A_REFCLKN_L	-		A_REFCLKN_L	-	
N30	VCC12	-		VCC12	-	
H33	RESP_ULC	-		RESP_ULC	-	
P25	RESETN	1		RESETN	1	
P26	TSALLN	1		TSALLN	1	
P31	DONE	1		DONE	1	
P23	INITN	1		INITN	1	
P30	M0	1		M0	1	
P22	M1	1		M1	1	
P24	M2	1		M2	1	
R22	M3	1		M3	1	
J37	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J38	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
P32	PL16C	7		PL15C	7	
R32	PL16D	7		PL15D	7	
G40	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
H40	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N33	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P33	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
G41	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
H41	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
T29	PL18C	7		PL18C	7	
U29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
G42	PL20A	7		PL19A	7	
H42	PL20B	7		PL19B	7	
M34	PL20C	7		PL19C	7	
M35	PL20D	7		PL19D	7	
K37	PL21A	7		PL26A	7	
L37	PL21B	7		PL26B	7	
N34	PL21C	7		PL26C	7	
P34	PL21D	7		PL26D	7	
K38	PL22A	7		PL30A	7	
L38	PL22B	7		PL30B	7	
T33	PL22C	7		PL30C	7	
R33	PL22D	7		PL30D	7	
J41	PL24A	7		PL34A	7	
K41	PL24B	7		PL34B	7	
U31	PL24C	7		PL34C	7	
V31	PL24D	7		PL34D	7	
K42	PL25A	7		PL38A	7	
J42	PL25B	7		PL38B	7	
J36	PL25C	7		PL38C	7	
K36	PL25D	7		PL38D	7	
N38	PL26A	7		PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD33	PL59D	6		PL73D	6	
AA38	PL60A	6		PL74A	6	
AB38	PL60B	6		PL74B	6	
AC29	PL60C	6		PL74C	6	
AD29	PL60D	6		PL74D	6	
AA41	PL61A	6		PL75A	6	
AB41	PL61B	6		PL75B	6	
AC34	PL61C	6		PL75C	6	
AD34	PL61D	6		PL75D	6	
AA42	PL63A	6		PL77A	6	
AB42	PL63B	6		PL77B	6	
AC37	PL63C	6		PL77C	6	
AD37	PL63D	6		PL77D	6	
AC38	PL64A	6		PL78A	6	
AD38	PL64B	6		PL78B	6	
AD36	PL64C	6		PL78C	6	
AE36	PL64D	6		PL78D	6	
AC39	PL65A	6		PL79A	6	
AD39	PL65B	6		PL79B	6	
AD35	PL65C	6		PL79C	6	
AE35	PL65D	6		PL79D	6	
AC40	PL67A	6		PL81A	6	
AD40	PL67B	6		PL81B	6	
AE37	PL67C	6		PL81C	6	
AF37	PL67D	6		PL81D	6	
AC41	PL68A	6		PL82A	6	
AD41	PL68B	6		PL82B	6	
AE34	PL68C	6		PL82C	6	
AF34	PL68D	6		PL82D	6	
AC42	PL69A	6		PL83A	6	
AD42	PL69B	6		PL83B	6	
AE33	PL69C	6		PL83C	6	
AF33	PL69D	6		PL83D	6	
AE38	PL72A	6		PL86A	6	
AF38	PL72B	6		PL86B	6	
AE32	PL72C	6		PL86C	6	
AF32	PL72D	6		PL86D	6	
AE41	PL73A	6		PL87A	6	
AF41	PL73B	6		PL87B	6	
AE31	PL73C	6		PL87C	6	
AF31	PL73D	6		PL87D	6	
AE42	PL74A	6		PL88A	6	
AF42	PL74B	6		PL88B	6	
AG37	PL74C	6		PL88C	6	
AH37	PL74D	6		PL88D	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL23	PB56D	5		PB58D	5	
AW24	PB57A	5		PB61A	5	
AW23	PB57B	5		PB61B	5	
AN23	PB57C	5		PB61C	5	
AP23	PB57D	5		PB61D	5	
AY23	PB59A	5		PB63A	5	
AY24	PB59B	5		PB63B	5	
AU23	PB59C	5		PB63C	5	
AU22	PB59D	5		PB63D	5	
AV23	PB60A	5		PB66A	5	
AV22	PB60B	5		PB66B	5	
AM22	PB60C	5		PB66C	5	
AL22	PB60D	5		PB66D	5	
BA23	PB61A	5		PB69A	5	
BA22	PB61B	5		PB69B	5	
AN22	PB61C	5		PB69C	5	
AP22	PB61D	5		PB69D	5	
BB23	PB63A	5		PB71A	5	
BB22	PB63B	5		PB71B	5	
AT22	PB63C	5		PB71C	5	
AR22	PB63D	5		PB71D	5	
BB21	PB65A	4		PB73A	4	
BB20	PB65B	4		PB73B	4	
AR21	PB65C	4		PB73C	4	
AT21	PB65D	4		PB73D	4	
BA21	PB66A	4		PB75A	4	
BA20	PB66B	4		PB75B	4	
AP21	PB66C	4		PB75C	4	
AN21	PB66D	4		PB75D	4	
AV21	PB67A	4		PB78A	4	
AV20	PB67B	4		PB78B	4	
AM21	PB67C	4		PB78C	4	
AL21	PB67D	4		PB78D	4	
AY20	PB69A	4		PB81A	4	
AY19	PB69B	4		PB81B	4	
AU21	PB69C	4		PB81C	4	
AU20	PB69D	4		PB81D	4	
AW20	PB70A	4		PB83A	4	
AW19	PB70B	4		PB83B	4	
AP20	PB70C	4		PB83C	4	
AN20	PB70D	4		PB83D	4	
BB19	PB71A	4		PB86A	4	
BB18	PB71B	4		PB86B	4	
AM20	PB71C	4		PB86C	4	
AL20	PB71D	4		PB86D	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AU9	PB103C	4		PB117C	4	
AU8	PB103D	4		PB117D	4	
AY8	PB104A	4		PB118A	4	
AY7	PB104B	4		PB118B	4	
AU7	PB104C	4		PB118C	4	
AU6	PB104D	4		PB118D	4	
BA7	PB105A	4		PB119A	4	
BA6	PB105B	4		PB119B	4	
AN13	PB105C	4		PB119C	4	
AN12	PB105D	4		PB119D	4	
AV9	PB107A	4		PB121A	4	
AV8	PB107B	4		PB121B	4	
AT10	PB107C	4		PB121C	4	
AT9	PB107D	4		PB121D	4	
AW8	PB108A	4		PB122A	4	
AW7	PB108B	4		PB122B	4	
AP11	PB108C	4		PB122C	4	
AP10	PB108D	4		PB122D	4	
BB5	PB109A	4		PB123A	4	
BB4	PB109B	4		PB123B	4	
AR10	PB109C	4		PB123C	4	
AR9	PB109D	4		PB123D	4	
BA5	PB111A	4		PB125A	4	
BA4	PB111B	4		PB125B	4	
AT7	PB111C	4		PB125C	4	
AT6	PB111D	4		PB125D	4	
BB3	PB112A	4		PB126A	4	
BA3	PB112B	4		PB126B	4	
AM14	PB112C	4		PB126C	4	
AL14	PB112D	4		PB126D	4	
AY5	PB113A	4		PB127A	4	
AY4	PB113B	4		PB127B	4	
AN11	PB113C	4		PB127C	4	
AN10	PB113D	4		PB127D	4	
AV7	PB115A	4		PB129A	4	
AV6	PB115B	4		PB129B	4	
AM12	PB115C	4		PB129C	4	
AM11	PB115D	4		PB129D	4	
AW5	PB116A	4		PB130A	4	
AW4	PB116B	4		PB130B	4	
AT5	PB116C	4		PB130C	4	
AT4	PB116D	4		PB130D	4	
AY2	PB117A	4		PB131A	4	
BA2	PB117B	4		PB131B	4	
AP9	PB117C	4		PB131C	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AC24	GND	-		GND	-	
AC26	GND	-		GND	-	
AC35	GND	-		GND	-	
AC8	GND	-		GND	-	
AD12	GND	-		GND	-	
AD16	GND	-		GND	-	
AD18	GND	-		GND	-	
AD20	GND	-		GND	-	
AD23	GND	-		GND	-	
AD25	GND	-		GND	-	
AD27	GND	-		GND	-	
AD31	GND	-		GND	-	
AE17	GND	-		GND	-	
AE19	GND	-		GND	-	
AE24	GND	-		GND	-	
AE26	GND	-		GND	-	
AE3	GND	-		GND	-	
AE39	GND	-		GND	-	
AF18	GND	-		GND	-	
AF20	GND	-		GND	-	
AF23	GND	-		GND	-	
AF25	GND	-		GND	-	
AF36	GND	-		GND	-	
AF7	GND	-		GND	-	
AG11	GND	-		GND	-	
AG16	GND	-		GND	-	
AG19	GND	-		GND	-	
AG24	GND	-		GND	-	
AG27	GND	-		GND	-	
AG32	GND	-		GND	-	
AH15	GND	-		GND	-	
AH28	GND	-		GND	-	
AH4	GND	-		GND	-	
AH40	GND	-		GND	-	
AJ35	GND	-		GND	-	
AJ8	GND	-		GND	-	
AK12	GND	-		GND	-	
AK31	GND	-		GND	-	
AL13	GND	-		GND	-	
AL19	GND	-		GND	-	
AL24	GND	-		GND	-	
AL3	GND	-		GND	-	
AL30	GND	-		GND	-	
AL39	GND	-		GND	-	
AM16	GND	-		GND	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-7FF1020C[1]	-7	Organic fcBGA	1020	COM	40.4
LFSC3GA40E-6FF1020C[1]	-6	Organic fcBGA	1020	COM	40.4
LFSC3GA40E-5FF1020C[1]	-5	Organic fcBGA	1020	COM	40.4
LFSC3GA40E-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-7FC1152C[2]	-7	Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-6FC1152C[2]	-6	Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-5FC1152C[2]	-5	Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-7FF1152C	-7	Organic fcBGA	1152	COM	40.4
LFSC3GA40E-6FF1152C	-6	Organic fcBGA	1152	COM	40.4
LFSC3GA40E-5FF1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-7FF1020C[1]	-7	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-6FF1020C[1]	-6	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-5FF1020C[1]	-5	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-7FC1152C[2]	-7	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FC1152C[2]	-6	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FC1152C[2]	-5	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-7FF1152C	-7	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FF1152C	-6	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FF1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Industrial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-6F256I	-6	fpBGA	256	IND	15.2
LFSC3GA15E-5F256I	-5	fpBGA	256	IND	15.2
LFSC3GA15E-6F900I	-6	fpBGA	900	IND	15.2
LFSC3GA15E-5F900I	-5	fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-6F256I	-6	fpBGA	256	IND	15.2
LFSCM3GA15EP1-5F256I	-5	fpBGA	256	IND	15.2
LFSCM3GA15EP1-6F900I	-6	fpBGA	900	IND	15.2
LFSCM3GA15EP1-5F900I	-5	fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-6F900I	-6	fpBGA	900	IND	25.4
LFSC3GA25E-5F900I	-5	fpBGA	900	IND	25.4
LFSC3GA25E-6FF1020I[1]	-6	Organic fcBGA	1020	IND	25.4
LFSC3GA25E-5FF1020I[1]	-5	Organic fcBGA	1020	IND	25.4
LFSC3GA25E-6FFA1020I	-6	Organic fcBGA Revision 2	1020	IND	25.4
LFSC3GA25E-5FFA1020I	-5	Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-6F900I	-6	fpBGA	900	IND	25.4
LFSCM3GA25EP1-5F900I	-5	fpBGA	900	IND	25.4
LFSCM3GA25EP1-6FF1020I[1]	-6	Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-5FF1020I[1]	-5	Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-6FFA1020I	-6	Organic fcBGA Revision 2	1020	IND	25.4
LFSCM3GA25EP1-5FFA1020I	-5	Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-6FF1020I[1]	-6	Organic fcBGA	1020	IND	40.4
LFSC3GA40E-5FF1020I[1]	-5	Organic fcBGA	1020	IND	40.4
LFSC3GA40E-6FFA1020I	-6	Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-5FFA1020I	-5	Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-6FC1152I[2]	-6	Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-5FC1152I[2]	-5	Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-6FF1152I	-6	Organic fcBGA	1152	IND	40.4
LFSC3GA40E-5FF1152I	-5	Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.