# Lattice Semiconductor Corporation - LFSC3GA80E-5FF1704C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 20000 |
| Number of Logic Elements/Cells | 80000 |
| Total RAM Bits | 5816320 |
| Number of I/O | 904 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1704-BBGA, FCBGA |
| Supplier Device Package | 1704-OFCBGA (42.5x42.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-5ff1704c |

## Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. Table 2-2 lists the modes and the capability of the Slice blocks.

***Table 2-2. Slice Modes***

| | Logic | Ripple | RAM | ROM |
|---|---|---|---|---|
| PFU Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | SPR 16x2<br>DPR 16x2 | ROM 16x2 |

## Logic Mode

In this mode, the LUTs in each Slice are configured as combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices in the PFU.

## Ripple Mode

Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Up counter 2-bit
- Down counter 2-bit
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

## RAM Mode

In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the Slice. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode, please see details of additional technical documentation at the end of this data sheet.

***Table 2-3. Number of Slices Required For Implementing Distributed RAM***

| | SPR16x2 | DPR16x2 |
|---|---|---|
| Number of Slices | 1 | 2 |

Note: SPR = Single Port RAM, DPR = Dual Port RAM

## ROM Mode

The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

***Figure 2-13. DLL to PLL***

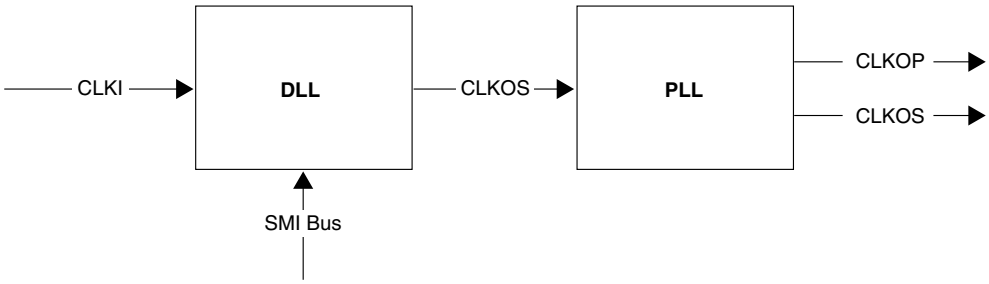



Figure 2-14 shows a shift of only CLKOP out in time.

***Figure 2-14. PLL to DLL***

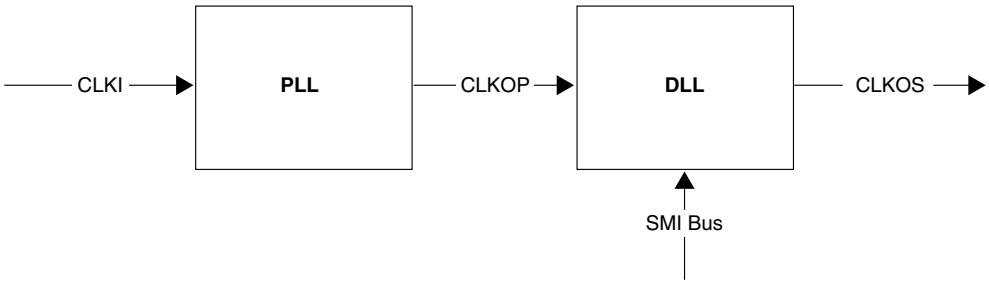
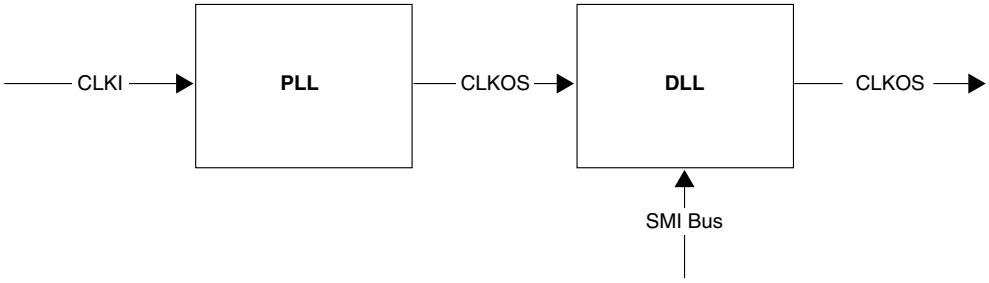



Figure 2-15 shows a shift of only CLKOS out in time.

***Figure 2-15. PLL to DLL***




For further information on the DLL, please see details of additional technical documentation at the end of this data sheet.

## sysMEM Memory Block

The sysMEM block can implement single port, true dual port, pseudo dual port or FIFO memories. Dedicated FIFO support logic allows the LatticeSC devices to efficiently implement FIFOs without consuming LUTs or routing resources for flag generation. Each block can be used in a variety of depths and widths as shown in Table 2-5. Memory with ranges from x1 to x18 in all modes: single port, pseudo-dual port and FIFO also providing x36.

*Table 2-10. Supported Output Standards[4]*

| Output Standard | Drive | $V_{CCIO}$ (Nom) | On-chip Output Termination |
|---|---|---|---|
| **Single-ended Interfaces** | | | |
| LVTTL/D[1] | 8mA, 16mA, 24mA | 3.3 | None. |
| LVCMOS33/D[1] | 8mA, 16mA, 24mA | 3.3 | None |
| LVCMOS25/D[1, 2] | 4mA, 8mA, 12mA, 16mA, | 2.5 | None, series: 25, 33, 50, 100 |
| LVCMOS18/D[1, 2] | 4mA, 8mA, 12mA, 16mA, | 1.8 | None, series: 25, 33, 50, 100 |
| LVCMOS15/D[1, 2] | 4mA, 8mA, 12mA, 16mA, | 1.5 | None, series: 25, 33, 50, 100 |
| LVCMOS12/D[1, 2] | 2mA, 4mA, 8mA, 12mA | 1.2 | None, series: 25, 33, 50, 100 |
| PCIX15 | N/A | 1.5 | None |
| PCI33, PCIX33, AGP1X33, AGP2X33 | N/A | 3.3 | None |
| HSTL18_I | N/A | 1.8 | None, series: 50 |
| HSTL18_II | N/A | 1.8 | None, series: 25, series + parallel to $V_{CCIO}$/2: 25 + 60 |
| HSTL15_I | N/A | 1.5 | None, series: 50 |
| HSTL15_II | N/A | 1.5 | None, series: 25, series + parallel to $V_{CCIO}$/2: 25 + 60 |
| SSTL33_I | N/A | 3.3 | None |
| SSTL33_II | N/A | 3.3 | None |
| SSTL25_I | N/A | 2.5 | None, series: 50 |
| SSTL25_II | N/A | 2.5 | None, series: 33, series + parallel to $V_{CCIO}$/2: 33+ 60 |
| SSTL18_ I | N/A | 1.8 | None, series: 33 |
| SSTL18_II | N/A | 1.8 | None, series: 33, series + parallel to $V_{CCIO}$/2: 33+ 60 |
| **Differential Interfaces** | | | |
| SSTL18D_I | N/A | 1.8 | None, series: 33 |
| SSTL25D_I | N/A | 2.5 | None, series: 50 |
| SSTL18D_II, SSTL25D_II | N/A | 1.2/2.5/3.3 | None, series: 33, series + parallel to $V_{CCIO}$/2: 33+ 60 |
| SSTL33D_I, II | N/A | 3.3 | None |
| HSTL15D_I, HSTL18D_I | N/A | 1.5/1.8 | None, series: 50 |
| HST15D_II, HSTL18D_II | N/A | 1.5/1.8 | None, series: 25, series + parallel to $V_{CCIO}$/2: 25 + 60 |
| LVDS | 2mA, 3.5mA, 4mA, 6mA | N/A | None |
| Mini-LVDS | 3.5mA, 4mA, 6mA | N/A | None |
| BLVDS25 | N/A | N/A | None |
| MLVDS25 | N/A | N/A | None |
| LVPECL33[3] | N/A | 3.3 | None |
| RSDS | 2mA, 3.5mA, 4mA, 6mA | N/A | None |

1. D refers to open drain capability.
2. User can select either drive current or driver impedances but not both.
3. Emulated with external resistors.
4. No GTL or GTL+ support.

## PCI Clamp

A programmable PCI clamp is available on the top and bottom banks of the device. The PCI clamp can be turned “ON” or “OFF” on each pin independently. The PCI clamp is used when implementing a 3.3V PCI interface. The

this allows for easy integration with the rest of the system. These capabilities make the LatticeSC ideal for many multiple power supply and hot-swap applications. The maximum current during hot socketing is 4mA. See Hot Socketing Specifications in Chapter 3 of this data sheet.

## Power-Up Requirements

To prevent high power supply and input pin currents, each VCC, VCC12, VCCAUX, VCCIO and VCCJ power supplies must have a monotonic ramp up time of 75 ms or less to reach its minimum operating voltage. Apart from VCC and VCC12, which have an additional requirement, and VCCIO and VCCAUX, which also have an additional requirement, the VCC, VCC12, VCCAUX, VCCIO and VCCJ power supplies can ramp up in any order, with no restriction on the time between them. However, the ramp time for each must be 75 ms or less. Configuration of the device will not proceed until the last power supply has reached its minimum operating voltage.

**Additional Requirement for VCC and VCC12:**
VCC12 must always be higher than VCC. This condition must be maintained at ALL times, including during power-up and power-down. Note that for 1.2V only operation, it is advisable to source both of these supplies from the same power supply.

**Additional Requirement for VCCIO and VCCAUX:**
If any VCCIOs are 1.2/1.5/1.8V, then VCCAUX MUST be applied before them. If any VCCIO is 1.2/1.5/1.8V and is powered up before VCCAUX, then when VCCAUX is powered up, it may drag VCCIO up with it as it crosses through the VCCIO value. (Note: If the VCCIO supply is capable of sinking current, as well as the more usual sourcing capability, this behavior is eliminated. However, the amount of current that the supply needs to sink is unknown and is likely to be in the hundreds of milliamps range).

## Power-Down Requirements

To prevent high power supply and input pin currents, power must be removed monotonically from either VCC or VCCAUX (and must reach the power-down trip point of 0.5V for VCC, 0.95V for VCCAUX) before power is removed monotonically from VCC12, any of the VCCIOs, or VCCJ. Note that VCC12 can be removed at the same time as VCC, but it cannot be removed earlier. In many applications, VCC and VCC12 will be sourced from the same power supply and so will be removed together. For systems where disturbance of the user pins is a don't care condition, the power supplies can be removed in any order as long as they power down monotonically within 200ms of each other.

Additionally, if any banks have VCCIO=3.3V nominal (potentially banks 1, 4, 5) then VCCIO for those banks must not be lower than VCCAUX during power-down. The normal variation in ramp-up times of power supplies and voltage regulators is not a concern here.

Note: The SERDES power supplies are NOT included in these requirements and have no specific sequencing requirements. However, when using the SERDES with VDDIB or VDDOB that is greater than 1.2V (1.5V nominal for example), the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in the ramp-up times of power supplies and voltage regulators is not a concern here.

## SERDES Power Supply Sequencing Requirements

When using the SERDES with 1.5V VDDIB or VDDOB supplies, the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and the 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in ramp-up times of power supples and voltage regulators is not a concern.

**Additional Requirement for SERDES Power Supply**
All VCC12 pins need to be connected on all devices independent of functionality used on the device. This analog supply is used by both the RX and TX portions of the SERDES and is used to control the core SERDES logic regardless of the SERDES being used in the design. VDDIB and VDDOB are used as supplies for the terminations on the CML input and output buffers. If a particular channel is not used, these can be UNCONNECTED (floating).

## Density Shifting

The LatticeSC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

# Typical Building Block Function Performance

**Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%**

### Pin to Pin Performance (LVCMOS25 12 mA Drive)

| Function | -7* | Units |
|---|---|---|
| **Basic Functions** | | |
| 32-bit Decoder | 6.65 | ns |
| Combinatorial (Pin to LUT to Pin) | 5.58 | ns |
| **Embedded Memory Functions (Single Port RAM)** | | |
| Pin to EBR Input Register Setup (Global Clock) | 1.66 | ns |
| EBR Output Clock to Pin (Global Clock) | 8.54 | ns |
| **Distributed (PFU) RAM (Single Port RAM)** | | |
| Pin to PFU RAM Register Setup (Global Clock) | 1.32 | ns |
| PFU RAM Clock to Pin (Global Clock) | 6.83 | ns |

*Typical performance per function

### Register-to-Register Performance

| Function | -7* | Units |
|---|---|---|
| **Basic Functions** | | |
| 32-Bit Decoder | 539 | MHz |
| 64-Bit Decoder | 517 | MHz |
| 16:1 MUX | 1003 | MHz |
| 32:1 MUX | 798 | MHz |
| 16-Bit Adder | 672 | MHz |
| 64-Bit Adder | 353 | MHz |
| 16-Bit Counter | 719 | MHz |
| 64-Bit Counter | 369 | MHz |
| 32x8 SP RAM (PFU, Output Registered) | 768 | MHz |
| 128x8 SP RAM (PFU, Output Registered) | 545 | MHz |
| **Embedded Memory Functions** | | |
| Single Port RAM (512x36 Bits) | 372 | MHz |
| True Dual Port RAM 1024x18 Bits (No EBR Out Reg) | 326 | MHz |
| True dual port RAM 1024x18 Bits (EBR Reg) | 372 | MHz |
| FIFO port (A: x36 bits, B: x9 Bits, No EBR Out Reg) | 353 | MHz |
| FIFO port (A: x36 bits, B: x9 Bits, EBR Reg) | 375 | MHz |
| True DP RAM Width Cascading (1024x72) | 372 | MHz |
| **DSP Functions** | | |
| 9x9 1-stage Multiplier | 209 | MHz |
| 18x18 1-Stage Multiplier | 155 | MHz |
| 9x9 3-Stage Pipelined Multiplier | 373 | MHz |
| 18x18 4-Stage Pipelined Multiplier | 314 | MHz |
| 9x9 Constant Multiplier | 372 | MHz |

*Typical performance per function

# LatticeSC/M External Switching Characteristics[3]

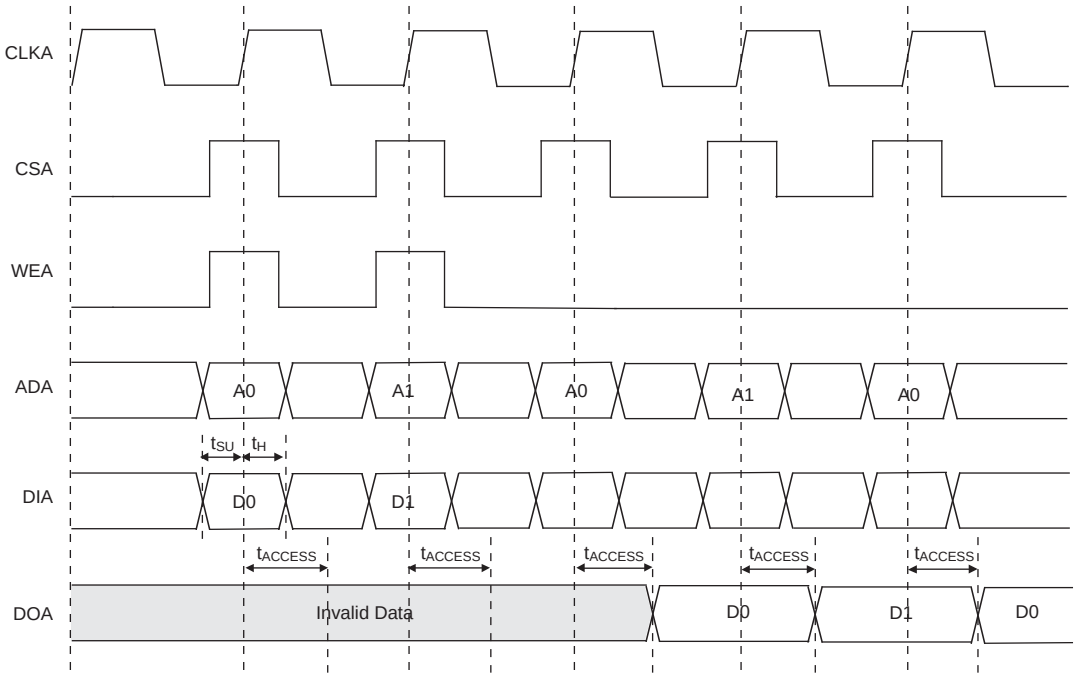
**Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%**

| Parameter | Description | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **General I/O Pin Parameters (using Primary Clock without PLL)[2]** | | | | | | | | |
| $t_{CO}$ | Global Clock Input to Output - PIO Output Register | 2.83 | 5.74 | 2.83 | 6.11 | 2.83 | 6.49 | ns |
| $t_{SU}$ | Global Clock Input Setup - PIO Input Register without fixed input delay | -0.66 | — | -0.66 | — | -0.66 | — | ns |
| $t_{H}$ | Global Clock Input Hold - PIO Input Register without fixed input delay | 1.73 | — | 1.95 | — | 2.16 | — | ns |
| $t_{SU\_IDLY}$ | Global Clock Input Setup - PIO Input Register with input delay | 0.86 | — | 1.03 | — | 1.20 | — | ns |
| $t_{H\_IDLY}$ | Global Clock Input Hold - PIO Input Register with input delay | -0.17 | — | -0.17 | — | -0.17 | — | ns |
| $f_{MAX\_PFU}$ | Global Clock frequency of PFU register | — | 700 | — | 700 | — | 700 | MHz |
| $f_{MAX\_IO}$ | Global Clock frequency of I/O register | — | 1000 | — | 1000 | — | 1000 | MHz |
| $t_{GC\_SKEW}$ | Global Clock skew | — | 89 | — | 103 | — | 116 | ps |
| **General I/O Pin Parameters (using Primary Clock with PLL)[1, 2]** | | | | | | | | |
| $t_{CO}$ | Global Clock Input to Output - PIO Output Register | 2.25 | 4.81 | 2.25 | 5.08 | 2.25 | 5.37 | ns |
| $t_{SU}$ | Global Clock Input Setup - PIO Input Register without fixed input delay | -0.07 | — | -0.07 | — | -0.07 | — | ns |
| $t_{H}$ | Global Clock Input Hold - PIO Input Register without fixed input delay | 0.80 | — | 0.93 | — | 1.04 | — | ns |
| **General I/O Pin Parameters (using Edge Clock without PLL)[2]** | | | | | | | | |
| $t_{CO}$ | Edge Clock Input to Output - PIO Output Register | 2.38 | 4.77 | 2.38 | 5.04 | 2.38 | 5.33 | ns |
| $t_{SU}$ | Edge Clock Input Setup - PIO Input Register without fixed input delay | -0.08 | — | -0.08 | — | -0.08 | — | ns |
| $t_{H}$ | Edge Clock Input Hold - PIO Input Register | 0.49 | — | 0.58 | — | 0.66 | — | ns |
| $t_{SU\_IDLY}$ | Edge Clock Input Setup - PIO Input Register with input delay | 0.81 | — | 0.97 | — | 1.12 | — | ns |
| $t_{H\_IDLY}$ | Edge Clock Input Hold - PIO Input Register with input delay | -0.34 | — | -0.34 | — | -0.34 | — | ns |
| $t_{EC\_SKEW}$ | Edge Clock skew | — | 28 | — | 32 | — | 36 | ps |
| **General I/O Pin Parameters (using Latch FF without PLL)[2]** | | | | | | | | |
| $t_{SU}$ | Latch FF, Input Setup - PIO Input Register without fixed input delay | -0.14 | — | -0.14 | — | -0.14 | — | ns |
| $t_{H}$ | Latch FF, Input Hold - PIO Input Register without fixed input delay | 0.58 | — | 0.68 | — | 0.77 | — | ns |
| $t_{SU\_IDLY}$ | Latch FF, Input Setup - PIO Input Register with input delay | 0.70 | — | 0.68 | — | 0.77 | — | ns |
| $t_{H\_IDLY}$ | Latch FF, Input Hold - PIO Input Register with input delay | -0.30 | — | -0.30 | — | -0.30 | — | ns |

1. No PLL delay tuning (clock injection removal mode, system clock feedback).
2. Using LVCMOS25 12mA I/O. Timing adders for other supported I/O technologies are specified in the LatticeSC Family Timing Adders table.
3. Complete Timing Parameters for a user design are incorporated when running ispLEVER. This is a sampling of the key timing parameters. Timing specs are for non-AIL applications.

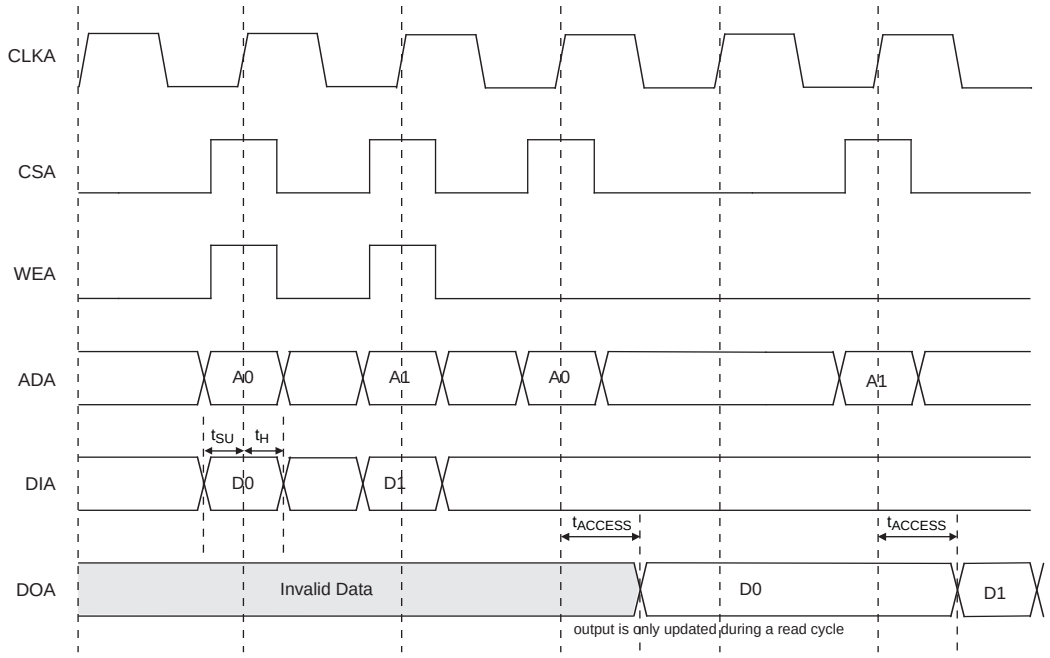
# EBR Memory Timing Diagrams

***Figure 3-6. Read Mode***




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

***Figure 3-7. Read Mode with Input Registers Only***



## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| MPI_STRBN | I | Driven active low indicates the start of a transaction on the PowerPC bus. MPI will strobe the address bus at next rising edge of clock. |
| MPI_ADDR[31:14] | I | Address bus driven by a PowerPC bus master. Only 18-bit width is needed. It has to be the least significant bit of the PowerPC 32-bit address A[31:14]. |
| MPI_DAT[n:0] | I/O | Selectable data bus width from 8, and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction. |
| MPI_PAR[m:0] | I/O | Selectable parity bus width from 1, 2, and 3-bit. MPI_DP[0] for MPI_D[7:0], MPI_DP[1] for MPI_D[15:8] and MPI_DP[2] for MPI_D[23:16]. |
| MPI_TA | O | Transfer acknowledge. Driven active low indicates that MPI received the data on the write cycle or returned data on the read cycle. |
| MPI_TEA | O | Transfer Error Acknowledge. Driven active low indicates that MPI detects a bus error on the internal system bus for current transaction. |
| MPI_RETRY | O | Active low MPI Retry requests the MPC860 to relinquish the bus and retry the cycle. |
| **Multi-chip Alignment (User I/O if not used.)** | | |
| MCA_DONE_OUT | O | Multi-chip alignment done output (to second MCA chip) |
| MCA_DONE_IN | I | Multi-chip alignment done input (from second MCA chip) |
| MCA_CLK_P[1:2]_OUT | O | Multi-chip alignment clock [1:2] output (sourced by MCA master chip) |
| MCA_CLK_P[1:2]_IN | I | Multi-chip alignment clock [1:2] input (from MCA master chip |
| TEMP | — | Temperature sensing diode pin. Dedicated pin. Accuracy is typically +/- 10°C. |
| **Miscellaneous Dedicated Pins** | | |
| XRES | — | External reference resistor between this pin and ground. The reference resistor is used to calibrate the programmable terminating resistors used in the I/Os. Dedicated pin. Value: 1K ± 1% ohm. |
| DIFFRx | — | Only used if a differential driver is used in a bank. This DIFFRx must be connected to ground via an external 1K ±1% ohm resistor for all banks that have a differential driver. |
| **SERDES Block (Dedicated Pins)** | | |
| [A:D]_HDINPx_[L/R] | I | High-speed input (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table. |
| [A:D]_HDINNx_[L/R] | I | High-speed input (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table. |
| [A:D]_HDOUTPx_[L/R] | O | High-speed output (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table. |
| [A:D]_HDOUTNx_[L/R] | O | High-speed output (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table. |
| [A:D]_REFCLKP_[L/R] | I | Ref clock input (positive), aux channel on left [L] or right [R] side of device. |
| [A:D]_REFCLKN_[L/R] | I | Ref clock input (negative), aux channel on left [L] or right [R] side of device. |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AF4 | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| AE5 | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| AG3 | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C |
| AH2 | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C |
| AD6 | PB4C | 5 | | PB4C | 5 | |
| AJ2 | PB5A | 5 | | PB5A | 5 | |
| AK2 | PB5B | 5 | | PB5B | 5 | |
| AD7 | PB5C | 5 | | PB5C | 5 | |
| AD8 | PB5D | 5 | VREF1_5 | PB5D | 5 | VREF1_5 |
| AH3 | PB7A | 5 | | PB11A | 5 | |
| AJ3 | PB7B | 5 | | PB11B | 5 | |
| AF9 | PB7C | 5 | | PB11C | 5 | |
| AE10 | PB7D | 5 | | PB11D | 5 | |
| AK3 | PB8A | 5 | | PB12A | 5 | |
| AJ4 | PB8B | 5 | | PB12B | 5 | |
| AE11 | PB9A | 5 | | PB13A | 5 | |
| AF10 | PB9B | 5 | | PB13B | 5 | |
| AK4 | PB11A | 5 | | PB16A | 5 | |
| AK5 | PB11B | 5 | | PB16B | 5 | |
| AH10 | PB12A | 5 | PCLKT5_3 | PB20A | 5 | PCLKT5_3 |
| AH11 | PB12B | 5 | PCLKC5_3 | PB20B | 5 | PCLKC5_3 |
| AF13 | PB12C | 5 | PCLKT5_4 | PB20C | 5 | PCLKT5_4 |
| AE14 | PB12D | 5 | PCLKC5_4 | PB20D | 5 | PCLKC5_4 |
| AK6 | PB13A | 5 | PCLKT5_5 | PB21A | 5 | PCLKT5_5 |
| AK7 | PB13B | 5 | PCLKC5_5 | PB21B | 5 | PCLKC5_5 |
| AF14 | PB13C | 5 | | PB21C | 5 | |
| AJ11 | PB15A | 5 | PCLKT5_0 | PB23A | 5 | PCLKT5_0 |
| AJ12 | PB15B | 5 | PCLKC5_0 | PB23B | 5 | PCLKC5_0 |
| AH13 | PB15D | 5 | VREF2_5 | PB23D | 5 | VREF2_5 |
| AK8 | PB16A | 5 | PCLKT5_1 | PB24A | 5 | PCLKT5_1 |
| AK9 | PB16B | 5 | PCLKC5_1 | PB24B | 5 | PCLKC5_1 |
| AH14 | PB17A | 5 | PCLKT5_2 | PB25A | 5 | PCLKT5_2 |
| AG14 | PB17B | 5 | PCLKC5_2 | PB25B | 5 | PCLKC5_2 |
| AK10 | PB19A | 5 | | PB28A | 5 | |
| AK11 | PB19B | 5 | | PB28B | 5 | |
| AH15 | PB20A | 5 | | PB29A | 5 | |
| AG15 | PB20B | 5 | | PB29B | 5 | |
| AH12 | PB21A | 5 | | PB31A | 5 | |
| AJ13 | PB21B | 5 | | PB31B | 5 | |
| AD15 | PB21C | 5 | | PB31C | 5 | |
| AE15 | PB21D | 5 | | PB31D | 5 | |
| AK12 | PB23A | 5 | | PB32A | 5 | |
| AK13 | PB23B | 5 | | PB32B | 5 | |
| AJ14 | PB24A | 5 | | PB33A | 5 | |
| AJ15 | PB24B | 5 | | PB33B | 5 | |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AJ27 | GND | - | | GND | - | |
| AF23 | GND | - | | GND | - | |
| AF22 | GND | - | | GND | - | |
| AE27 | GND | - | | GND | - | |
| AA27 | GND | - | | GND | - | |
| AB29 | GND | - | | GND | - | |
| Y26 | GND | - | | GND | - | |
| AC30 | GND | - | | GND | - | |
| Y29 | GND | - | | GND | - | |
| F30 | GND | - | | GND | - | |
| E27 | GND | - | | GND | - | |
| F27 | GND | - | | GND | - | |
| P25 | GND | - | | GND | - | |
| H29 | GND | - | | GND | - | |
| K29 | GND | - | | GND | - | |
| R24 | GND | - | | GND | - | |
| M28 | GND | - | | GND | - | |
| J27 | GND | - | | GND | - | |
| N26 | GND | - | | GND | - | |
| E20 | GND | - | | GND | - | |
| E21 | GND | - | | GND | - | |
| F21 | GND | - | | GND | - | |
| F23 | GND | - | | GND | - | |
| G23 | GND | - | | GND | - | |
| D21 | GND | - | | GND | - | |
| D20 | GND | - | | GND | - | |
| E18 | GND | - | | GND | - | |
| C20 | GND | - | | GND | - | |
| C11 | GND | - | | GND | - | |
| A12 | GND | - | | GND | - | |
| E11 | GND | - | | GND | - | |
| F8 | GND | - | | GND | - | |
| G8 | GND | - | | GND | - | |
| D11 | GND | - | | GND | - | |
| D10 | GND | - | | GND | - | |
| H7 | GND | - | | GND | - | |
| F10 | GND | - | | GND | - | |
| E10 | GND | - | | GND | - | |
| AC16 | NC | - | | NC | - | |
| J22 | VCC | - | | VCC | - | |
| J9 | VCC | - | | VCC | - | |
| B2 | NC | - | | NC | - | |
| C2 | RESPN_ULC | - | | RESPN_ULC | - | |
| C29 | RESPN_URC | - | | RESPN_URC | - | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| Y4 | PR48B | 3 | | PR63B | 3 | |
| W4 | PR48A | 3 | | PR63A | 3 | |
| W11 | PR47D | 3 | | PR60D | 3 | |
| V11 | PR47C | 3 | | PR60C | 3 | |
| W2 | PR47B | 3 | | PR60B | 3 | |
| V2 | PR47A | 3 | | PR60A | 3 | |
| W9 | PR45D | 3 | | PR57D | 3 | |
| V9 | PR45C | 3 | | PR57C | 3 | |
| V1 | PR45B | 3 | | PR57B | 3 | |
| U1 | PR45A | 3 | | PR57A | 3 | |
| W10 | PR44D | 3 | | PR56D | 3 | |
| V10 | PR44C | 3 | | PR56C | 3 | |
| U2 | PR44B | 3 | | PR56B | 3 | |
| T2 | PR44A | 3 | | PR56A | 3 | |
| Y8 | PR43D | 3 | | PR55D | 3 | |
| W8 | PR43C | 3 | VREF1_3 | PR55C | 3 | VREF1_3 |
| W5 | PR43B | 3 | | PR55B | 3 | |
| V5 | PR43A | 3 | | PR55A | 3 | |
| V7 | PR40D | 3 | PCLKC3_2 | PR52D | 3 | PCLKC3_2 |
| U7 | PR40C | 3 | PCLKT3_2 | PR52C | 3 | PCLKT3_2 |
| T1 | PR40B | 3 | | PR52B | 3 | |
| R1 | PR40A | 3 | | PR52A | 3 | |
| V8 | PR39D | 3 | PCLKC3_3 | PR51D | 3 | PCLKC3_3 |
| U8 | PR39C | 3 | PCLKT3_3 | PR51C | 3 | PCLKT3_3 |
| U5 | PR39B | 3 | | PR51B | 3 | |
| T5 | PR39A | 3 | | PR51A | 3 | |
| V6 | PR38D | 3 | PCLKC3_1 | PR50D | 3 | PCLKC3_1 |
| U6 | PR38C | 3 | PCLKT3_1 | PR50C | 3 | PCLKT3_1 |
| T4 | PR38B | 3 | PCLKC3_0 | PR50B | 3 | PCLKC3_0 |
| T3 | PR38A | 3 | PCLKT3_0 | PR50A | 3 | PCLKT3_0 |
| U9 | PR36D | 2 | PCLKC2_2 | PR48D | 2 | PCLKC2_2 |
| T9 | PR36C | 2 | PCLKT2_2 | PR48C | 2 | PCLKT2_2 |
| R2 | PR36B | 2 | PCLKC2_0 | PR48B | 2 | PCLKC2_0 |
| P2 | PR36A | 2 | PCLKT2_0 | PR48A | 2 | PCLKT2_0 |
| T11 | PR35D | 2 | PCLKC2_3 | PR47D | 2 | PCLKC2_3 |
| U11 | PR35C | 2 | PCLKT2_3 | PR47C | 2 | PCLKT2_3 |
| R4 | PR35B | 2 | PCLKC2_1 | PR47B | 2 | PCLKC2_1 |
| R3 | PR35A | 2 | PCLKT2_1 | PR47A | 2 | PCLKT2_1 |
| T8 | PR34D | 2 | | PR46D | 2 | |
| R8 | PR34C | 2 | | PR46C | 2 | |
| P1 | PR34B | 2 | | PR46B | 2 | |
| N1 | PR34A | 2 | | PR46A | 2 | |
| R6 | PR31D | 2 | | PR43D | 2 | |
| P6 | PR31C | 2 | | PR43C | 2 | |
| M1 | PR31B | 2 | | PR43B | 2 | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| R7 | NC | - | | PR39D | 2 | |
| P7 | NC | - | | PR39C | 2 | |
| N3 | NC | - | | PR39B | 2 | |
| M3 | NC | - | | PR39A | 2 | |
| H1 | NC | - | | PR26B | 2 | |
| G1 | NC | - | | PR26A | 2 | |
| L5 | NC | - | | PR25B | 2 | |
| K5 | NC | - | | PR25A | 2 | |
| G2 | NC | - | | PR24B | 2 | |
| F2 | NC | - | | PR24A | 2 | |
| F1 | NC | - | | PR22B | 2 | |
| E1 | NC | - | | PR22A | 2 | |
| A2 | GND | - | | GND | - | |
| A33 | GND | - | | GND | - | |
| AA15 | GND | - | | GND | - | |
| AA20 | GND | - | | GND | - | |
| AA32 | GND | - | | GND | - | |
| AA4 | GND | - | | GND | - | |
| AB28 | GND | - | | GND | - | |
| AB6 | GND | - | | GND | - | |
| AC11 | GND | - | | GND | - | |
| AC18 | GND | - | | GND | - | |
| AC25 | GND | - | | GND | - | |
| AD23 | GND | - | | GND | - | |
| AD3 | GND | - | | GND | - | |
| AD31 | GND | - | | GND | - | |
| AE12 | GND | - | | GND | - | |
| AE15 | GND | - | | GND | - | |
| AE29 | GND | - | | GND | - | |
| AE7 | GND | - | | GND | - | |
| AE9 | GND | - | | GND | - | |
| AF20 | GND | - | | GND | - | |
| AF26 | GND | - | | GND | - | |
| AG32 | GND | - | | GND | - | |
| AG4 | GND | - | | GND | - | |
| AH13 | GND | - | | GND | - | |
| AH19 | GND | - | | GND | - | |
| AH25 | GND | - | | GND | - | |
| AH7 | GND | - | | GND | - | |
| AJ10 | GND | - | | GND | - | |
| AJ16 | GND | - | | GND | - | |
| AJ22 | GND | - | | GND | - | |
| AJ28 | GND | - | | GND | - | |
| AK3 | GND | - | | GND | - | |
| AK31 | GND | - | | GND | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| BA19 | PB73A | 4 | | PB87A | 4 | |
| BA18 | PB73B | 4 | | PB87B | 4 | |
| AU19 | PB73C | 4 | | PB87C | 4 | |
| AU18 | PB73D | 4 | | PB87D | 4 | |
| AV19 | PB74A | 4 | PCLKT4_2 | PB89A | 4 | PCLKT4_2 |
| AV18 | PB74B | 4 | PCLKC4_2 | PB89B | 4 | PCLKC4_2 |
| AN19 | PB74C | 4 | PCLKT4_7 | PB89C | 4 | PCLKT4_7 |
| AP19 | PB74D | 4 | PCLKC4_7 | PB89D | 4 | PCLKC4_7 |
| BB17 | PB75A | 4 | PCLKT4_1 | PB90A | 4 | PCLKT4_1 |
| BB16 | PB75B | 4 | PCLKC4_1 | PB90B | 4 | PCLKC4_1 |
| AT19 | PB75C | 4 | PCLKT4_6 | PB90C | 4 | PCLKT4_6 |
| AT18 | PB75D | 4 | PCLKC4_6 | PB90D | 4 | PCLKC4_6 |
| BA17 | PB77A | 4 | PCLKT4_0 | PB91A | 4 | PCLKT4_0 |
| BA16 | PB77B | 4 | PCLKC4_0 | PB91B | 4 | PCLKC4_0 |
| AR19 | PB77C | 4 | VREF2_4 | PB91C | 4 | VREF2_4 |
| AR18 | PB77D | 4 | | PB91D | 4 | |
| AY17 | PB79A | 4 | PCLKT4_5 | PB93A | 4 | PCLKT4_5 |
| AY16 | PB79B | 4 | PCLKC4_5 | PB93B | 4 | PCLKC4_5 |
| AN18 | PB79C | 4 | | PB93C | 4 | |
| AP18 | PB79D | 4 | | PB93D | 4 | |
| AW17 | PB80A | 4 | PCLKT4_3 | PB94A | 4 | PCLKT4_3 |
| AW16 | PB80B | 4 | PCLKC4_3 | PB94B | 4 | PCLKC4_3 |
| AU17 | PB80C | 4 | PCLKT4_4 | PB94C | 4 | PCLKT4_4 |
| AU16 | PB80D | 4 | PCLKC4_4 | PB94D | 4 | PCLKC4_4 |
| AV17 | PB81A | 4 | | PB95A | 4 | |
| AV16 | PB81B | 4 | | PB95B | 4 | |
| AL18 | PB81C | 4 | | PB95C | 4 | |
| AM18 | PB81D | 4 | | PB95D | 4 | |
| BB15 | PB83A | 4 | | PB97A | 4 | |
| BB14 | PB83B | 4 | | PB97B | 4 | |
| AP17 | PB83C | 4 | | PB97C | 4 | |
| AN17 | PB83D | 4 | | PB97D | 4 | |
| BA15 | PB84A | 4 | | PB98A | 4 | |
| BA14 | PB84B | 4 | | PB98B | 4 | |
| AT16 | PB84C | 4 | | PB98C | 4 | |
| AT15 | PB84D | 4 | | PB98D | 4 | |
| AV15 | PB85A | 4 | | PB99A | 4 | |
| AV14 | PB85B | 4 | | PB99B | 4 | |
| AR16 | PB85C | 4 | | PB99C | 4 | |
| AR15 | PB85D | 4 | | PB99D | 4 | |
| AY14 | PB87A | 4 | | PB101A | 4 | |
| AY13 | PB87B | 4 | | PB101B | 4 | |
| AU15 | PB87C | 4 | | PB101C | 4 | |
| AU14 | PB87D | 4 | | PB101D | 4 | |
| BB13 | PB88A | 4 | | PB102A | 4 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AE1 | PR74A | 3 | | PR88A | 3 | |
| AF12 | PR73D | 3 | | PR87D | 3 | |
| AE12 | PR73C | 3 | | PR87C | 3 | |
| AF2 | PR73B | 3 | | PR87B | 3 | |
| AE2 | PR73A | 3 | | PR87A | 3 | |
| AF11 | PR72D | 3 | | PR86D | 3 | |
| AE11 | PR72C | 3 | | PR86C | 3 | |
| AF5 | PR72B | 3 | | PR86B | 3 | |
| AE5 | PR72A | 3 | | PR86A | 3 | |
| AF10 | PR69D | 3 | | PR83D | 3 | |
| AE10 | PR69C | 3 | | PR83C | 3 | |
| AD1 | PR69B | 3 | | PR83B | 3 | |
| AC1 | PR69A | 3 | | PR83A | 3 | |
| AF9 | PR68D | 3 | | PR82D | 3 | |
| AE9 | PR68C | 3 | | PR82C | 3 | |
| AD2 | PR68B | 3 | | PR82B | 3 | |
| AC2 | PR68A | 3 | | PR82A | 3 | |
| AF6 | PR67D | 3 | | PR81D | 3 | |
| AE6 | PR67C | 3 | | PR81C | 3 | |
| AD3 | PR67B | 3 | | PR81B | 3 | |
| AC3 | PR67A | 3 | | PR81A | 3 | |
| AE8 | PR65D | 3 | | PR79D | 3 | |
| AD8 | PR65C | 3 | | PR79C | 3 | |
| AD4 | PR65B | 3 | | PR79B | 3 | |
| AC4 | PR65A | 3 | | PR79A | 3 | |
| AE7 | PR64D | 3 | | PR78D | 3 | |
| AD7 | PR64C | 3 | | PR78C | 3 | |
| AD5 | PR64B | 3 | | PR78B | 3 | |
| AC5 | PR64A | 3 | | PR78A | 3 | |
| AD6 | PR63D | 3 | | PR77D | 3 | |
| AC6 | PR63C | 3 | | PR77C | 3 | |
| AB1 | PR63B | 3 | | PR77B | 3 | |
| AA1 | PR63A | 3 | | PR77A | 3 | |
| AD9 | PR61D | 3 | | PR75D | 3 | |
| AC9 | PR61C | 3 | | PR75C | 3 | |
| AB2 | PR61B | 3 | | PR75B | 3 | |
| AA2 | PR61A | 3 | | PR75A | 3 | |
| AD14 | PR60D | 3 | | PR74D | 3 | |
| AC14 | PR60C | 3 | | PR74C | 3 | |
| AB5 | PR60B | 3 | | PR74B | 3 | |
| AA5 | PR60A | 3 | | PR74A | 3 | |
| AD10 | PR59D | 3 | | PR73D | 3 | |
| AC10 | PR59C | 3 | | PR73C | 3 | |
| Y1 | PR59B | 3 | | PR73B | 3 | |
| W1 | PR59A | 3 | | PR73A | 3 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AG38 | NC | - | | PL95A | 6 | |
| AH38 | NC | - | | PL95B | 6 | |
| AJ39 | NC | - | | PL100A | 6 | |
| AK39 | NC | - | | PL100B | 6 | |
| AL41 | NC | - | | PL105A | 6 | |
| AM41 | NC | - | | PL105B | 6 | |
| AN40 | NC | - | | PL108A | 6 | |
| AM40 | NC | - | | PL108B | 6 | |
| AM39 | NC | - | | PL111A | 6 | |
| AN39 | NC | - | | PL111B | 6 | |
| AR42 | NC | - | | PL113A | 6 | |
| AT42 | NC | - | | PL113B | 6 | |
| AT1 | NC | - | | PR113B | 3 | |
| AR1 | NC | - | | PR113A | 3 | |
| AN4 | NC | - | | PR111B | 3 | |
| AM4 | NC | - | | PR111A | 3 | |
| AM3 | NC | - | | PR108B | 3 | |
| AN3 | NC | - | | PR108A | 3 | |
| AM2 | NC | - | | PR105B | 3 | |
| AL2 | NC | - | | PR105A | 3 | |
| AK4 | NC | - | | PR100B | 3 | |
| AJ4 | NC | - | | PR100A | 3 | |
| AH5 | NC | - | | PR95B | 3 | |
| AG5 | NC | - | | PR95A | 3 | |
| P6 | NC | - | | PR39B | 2 | |
| N6 | NC | - | | PR39A | 2 | |
| L3 | NC | - | | PR36B | 2 | |
| K3 | NC | - | | PR36A | 2 | |
| M5 | NC | - | | PR35A | 2 | |
| L4 | NC | - | | PR32B | 2 | |
| K4 | NC | - | | PR32A | 2 | |
| A2 | GND | - | | GND | - | |
| A41 | GND | - | | GND | - | |
| AA20 | GND | - | | GND | - | |
| AA23 | GND | - | | GND | - | |
| AA3 | GND | - | | GND | - | |
| AA39 | GND | - | | GND | - | |
| AB20 | GND | - | | GND | - | |
| AB23 | GND | - | | GND | - | |
| AB4 | GND | - | | GND | - | |
| AB40 | GND | - | | GND | - | |
| AC17 | GND | - | | GND | - | |
| AC19 | GND | - | | GND | - | |
| AC21 | GND | - | | GND | - | |
| AC22 | GND | - | | GND | - | |

## Lead-Free Packaging

**Commercial**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA15E-7FN256C | -7 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSC3GA15E-6FN256C | -6 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSC3GA15E-5FN256C | -5 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSC3GA15E-7FN900C | -7 | Lead-Free fpBGA | 900 | COM | 15.2 |
| LFSC3GA15E-6FN900C | -6 | Lead-Free fpBGA | 900 | COM | 15.2 |
| LFSC3GA15E-5FN900C | -5 | Lead-Free fpBGA | 900 | COM | 15.2 |

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA15EP1-7FN256C | -7 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSCM3GA15EP1-6FN256C | -6 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSCM3GA15EP1-5FN256C | -5 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSCM3GA15EP1-7FN900C | -7 | Lead-Free fpBGA | 900 | COM | 15.2 |
| LFSCM3GA15EP1-6FN900C | -6 | Lead-Free fpBGA | 900 | COM | 15.2 |
| LFSCM3GA15EP1-5FN900C | -5 | Lead-Free fpBGA | 900 | COM | 15.2 |

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA25E-7FN900C | -7 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSC3GA25E-6FN900C | -6 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSC3GA25E-5FN900C | -5 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSC3GA25E-7FFN1020C[1] | -7 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSC3GA25E-6FFN1020C[1] | -6 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSC3GA25E-5FFN1020C[1] | -5 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSC3GA25E-7FFAN1020C | -7 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSC3GA25E-6FFAN1020C | -6 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSC3GA25E-5FFAN1020C | -5 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA25EP1-7FN900C | -7 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSCM3GA25EP1-6FN900C | -6 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSCM3GA25EP1-5FN900C | -5 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSCM3GA25EP1-7FFN1020C[1] | -7 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-6FFN1020C[1] | -6 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-5FFN1020C[1] | -5 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-7FFAN1020C | -7 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-6FFAN1020C | -6 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-5FFAN1020C | -5 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

**Commercial, Cont.**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA40E-7FFN1020C[1] | -7 | Lead-Free Organic fcBGA | 1020 | COM | 40.4 |
| LFSC3GA40E-6FFN1020C[1] | -6 | Lead-Free Organic fcBGA | 1020 | COM | 40.4 |
| LFSC3GA40E-5FFN1020C[1] | -5 | Lead-Free Organic fcBGA | 1020 | COM | 40.4 |
| LFSC3GA40E-7FFAN1020C | -7 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSC3GA40E-6FFAN1020C | -6 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSC3GA40E-5FFAN1020C | -5 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSC3GA40E-7FCN1152C[2] | -7 | Lead-Free Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSC3GA40E-6FCN1152C[2] | -6 | Lead-Free Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSC3GA40E-5FCN1152C[2] | -5 | Lead-Free Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSC3GA40E-7FFN1152C | -7 | Lead-Free Organic fcBGA | 1152 | COM | 40.4 |
| LFSC3GA40E-6FFN1152C | -6 | Lead-Free Organic fcBGA | 1152 | COM | 40.4 |
| LFSC3GA40E-5FFN1152C | -5 | Lead-Free Organic fcBGA | 1152 | COM | 40.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA40EP1-7FFN1020C[1] | -7 | Organic fcBGA | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-6FFN1020C[1] | -6 | Organic fcBGA | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-5FFN1020C[1] | -5 | Organic fcBGA | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-7FFAN1020C | -7 | Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-6FFAN1020C | -6 | Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-5FFAN1020C | -5 | Organic fcBGA Revision 2 | 1020 | COM | 40.4 |
| LFSCM3GA40EP1-7FCN1152C[2] | -7 | Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSCM3GA40EP1-6FCN1152C[2] | -6 | Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSCM3GA40EP1-5FCN1152C[2] | -5 | Ceramic fcBGA | 1152 | COM | 40.4 |
| LFSCM3GA40EP1-7FFN1152C | -7 | Organic fcBGA | 1152 | COM | 40.4 |
| LFSCM3GA40EP1-6FFN1152C | -6 | Organic fcBGA | 1152 | COM | 40.4 |
| LFSCM3GA40EP1-5FFN1152C | -5 | Organic fcBGA | 1152 | COM | 40.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

**Commercial, Cont.**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA115EP1-6FCN1152C[1] | -6 | Lead-Free Ceramic fcBGA | 1152 | COM | 115.2 |
| LFSCM3GA115EP1-5FCN1152C[1] | -5 | Lead-Free Ceramic fcBGA | 1152 | COM | 115.2 |
| LFSCM3GA115EP1-6FFN1152C | -6 | Lead-Free Organic fcBGA | 1152 | COM | 115.2 |
| LFSCM3GA115EP1-5FFN1152C | -5 | Lead-Free Organic fcBGA | 1152 | COM | 115.2 |
| LFSCM3GA115EP1-6FCN1704C[1] | -6 | Lead-Free Ceramic fcBGA | 1704 | COM | 115.2 |
| LFSCM3GA115EP1-5FCN1704C[1] | -5 | Lead-Free Ceramic fcBGA | 1704 | COM | 115.2 |
| LFSCM3GA115EP1-6FFN1704C | -6 | Lead-Free Organic fcBGA | 1704 | COM | 115.2 |
| LFSCM3GA115EP1-5FFN1704C | -5 | Lead-Free Organic fcBGA | 1704 | COM | 115.2 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

**Industrial**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA15E-6FN256I | -6 | Lead-Free fpBGA | 256 | IND | 15.2 |
| LFSC3GA15E-5FN256I | -5 | Lead-Free fpBGA | 256 | IND | 15.2 |
| LFSC3GA15E-6FN900I | -6 | Lead-Free fpBGA | 900 | IND | 15.2 |
| LFSC3GA15E-5FN900I | -5 | Lead-Free fpBGA | 900 | IND | 15.2 |

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA15EP1-6FN256I | -6 | Lead-Free fpBGA | 256 | IND | 15.2 |
| LFSCM3GA15EP1-5FN256I | -5 | Lead-Free fpBGA | 256 | IND | 15.2 |
| LFSCM3GA15EP1-6FN900I | -6 | Lead-Free fpBGA | 900 | IND | 15.2 |
| LFSCM3GA15EP1-5FN900I | -5 | Lead-Free fpBGA | 900 | IND | 15.2 |

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA25E-6FN900I | -6 | Lead-Free fpBGA | 900 | IND | 25.4 |
| LFSC3GA25E-5FN900I | -5 | Lead-Free fpBGA | 900 | IND | 25.4 |
| LFSC3GA25E-6FFN1020I[1] | -6 | Lead-Free Organic fcBGA | 1020 | IND | 25.4 |
| LFSC3GA25E-5FFN1020I[1] | -5 | Lead-Free Organic fcBGA | 1020 | IND | 25.4 |
| LFSC3GA25E-6FFAN1020I | -6 | Lead-Free Organic fcBGA Revision 2 | 1020 | IND | 25.4 |
| LFSC3GA25E-5FFAN1020I | -5 | Lead-Free Organic fcBGA Revision 2 | 1020 | IND | 25.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA25EP1-6FN900I | -6 | Lead-Free fpBGA | 900 | IND | 25.4 |
| LFSCM3GA25EP1-5FN900I | -5 | Lead-Free fpBGA | 900 | IND | 25.4 |
| LFSCM3GA25EP1-6FFN1020I[1] | -6 | Lead-Free Organic fcBGA | 1020 | IND | 25.4 |
| LFSCM3GA25EP1-5FFN1020I[1] | -5 | Lead-Free Organic fcBGA | 1020 | IND | 25.4 |
| LFSCM3GA25EP1-6FFAN1020I | -6 | Lead-Free Organic fcBGA Revision 2 | 1020 | IND | 25.4 |
| LFSCM3GA25EP1-5FFAN1020I | -5 | Lead-Free Organic fcBGA Revision 2 | 1020 | IND | 25.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA40E-6FFN1020I[1] | -6 | Lead-Free Organic fcBGA | 1020 | IND | 40.4 |
| LFSC3GA40E-5FFN1020I[1] | -5 | Lead-Free Organic fcBGA | 1020 | IND | 40.4 |
| LFSC3GA40E-6FFAN1020I | -6 | Lead-Free Organic fcBGA Revision 2 | 1020 | IND | 40.4 |
| LFSC3GA40E-5FFAN1020I | -5 | Lead-Free Organic fcBGA Revision 2 | 1020 | IND | 40.4 |
| LFSC3GA40E-6FCN1152I[2] | -6 | Lead-Free Ceramic fcBGA | 1152 | IND | 40.4 |
| LFSC3GA40E-5FCN1152I[2] | -5 | Lead-Free Ceramic fcBGA | 1152 | IND | 40.4 |
| LFSC3GA40E-6FFN1152I | -6 | Lead-Free Organic fcBGA | 1152 | IND | 40.4 |
| LFSC3GA40E-5FFN1152I | -5 | Lead-Free Organic fcBGA | 1152 | IND | 40.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.