# Lattice Semiconductor Corporation - LFSC3GA80E-5FFN1704I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 20000 |
| Number of Logic Elements/Cells | 80000 |
| Total RAM Bits | 5816320 |
| Number of I/O | 904 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Package / Case | 1704-BBGA, FCBGA |
| Supplier Device Package | 1704-OFCBGA (42.5x42.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-5ffn1704i |

*Table 1-1. LatticeSC Family Selection Guide*[1]

| Device | SC15 | SC25 | SC40 | SC80 | SC115 |
|---|---|---|---|---|---|
| LUT4s (K) | 15 | 25 | 40 | 80 | 115 |
| sysMEM Blocks (18Kb) | 56 | 104 | 216 | 308 | 424 |
| Embedded Memory (Mbits) | 1.03 | 1.92 | 3.98 | 5.68 | 7.8 |
| Max. Distributed Memory (Mbits) | 0.24 | 0.41 | 0.65 | 1.28 | 1.84 |
| Number of 3.8Gbps SERDES (Max.) | 8 | 16 | 16 | 32 | 32 |
| DLLs | 12 | 12 | 12 | 12 | 12 |
| Analog PLLs | 8 | 8 | 8 | 8 | 8 |
| MACO Blocks | 4 | 6 | 10 | 10 | 12 |
| **Package I/O/SERDES Combinations (1mm ball pitch)** | | | | | |
| 256-ball fpBGA (17 x 17mm) | 139/4 | | | | |
| 900-ball fpBGA (31 x 31mm) | 300/8 | 378/8 | | | |
| 1020-ball fcBGA (33 x 33mm)[2] | | 476/16 | 562/16 | | |
| 1152-ball fcBGA (35 x 35mm)[3] | | | 604/16 | 660/16 | 660/16 |
| 1704-ball fcBGA (42.5 x 42.5mm)[3] | | | | 904/32 | 942/32 |

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per PCN #02A-10.
3. Ceramic fcBGA converted to organic fcBGA per PCN #01A-10.

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

*Table 1-2. LatticeSCM Family*

| Device | SCM15 | SCM25 | SCM40 | SCM80 | SCM115 |
|---|---|---|---|---|---|
| flexiMAC Blocks<br>• 1GbE Mode<br>• 10GbE Mode<br>• PCI Express Mode | 1 | 2 | 2 | 2 | 4 |
| SPI4.2 Blocks | 1 | 2 | 2 | 2 | 2 |
| Memory Controller Blocks<br>• DDR/DDR2 DRAM Mode<br>• QDR II/II+ SRAM Mode<br>• RLDRAM I<br>• RLDRAM II CIO/SIO | 1 | 2 | 2 | 2 | 2 |
| Low-Speed CDR Blocks | 0 | 0 | 2 | 2 | 2 |
| PCI Express LTSSM (PHY) Blocks | 1 | 0 | 2 | 2 | 2 |

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

## Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

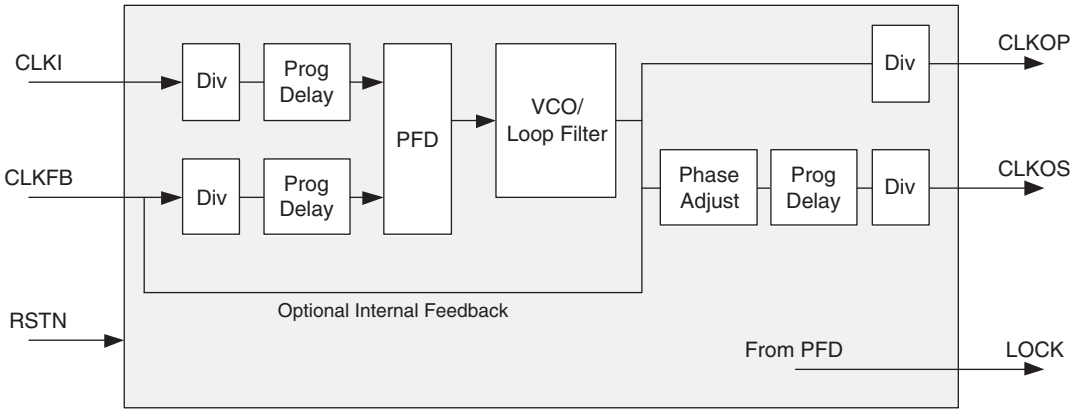
The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically.

The Phase Select block can modify the phase of the clock signal if desired. The Spread Spectrum block supports the modulation of the PLL output frequency. This reduces the peak energy in the fundamental and its harmonics providing for lower EMI (Electro Magnetic Interference).

The sysCLOCK PLL can be configured at power-up and then, if desired, reconfigured dynamically through the serial memory interface bus which connects with the on-chip system bus. For example, the user can select inputs, loop filters, divider setting, delay settings and phase shift settings. The user can also directly access the SMI bus through the routing.

The PLL clock input, from pin or routing, feeds into an input divider. There are four sources of feedback signal to the feedback divider: from the clock net, directly from the voltage controlled oscillator (VCO) output, from the routing or from an external pin. The signal from the input clock divider and the feedback divider are passed through the programmable delay before entering the phase frequency detector (PFD) unit. The output of this PFD is used to control the voltage controlled oscillator. There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

***Figure 2-11. PLL Diagram***




For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

## Spread Spectrum Clocking (SSC)

The PLL supports spread spectrum clocking to reduce peak EMI by using “down-spread” modulation. The spread spectrum operation will vary the output frequency (at 30KHz to 500KHz) in a range that is between its nominal value, down to a frequency that is a programmable 1%, 2%, or 3% lower than normal.

## Digital Locked Loop (DLLs)

In addition to PLLs, the LatticeSC devices have up to 12 DLLs per device. DLLs assist in the management of clocks and strobes. DLLs are well suited to applications where the clock may be stopped or transferring jitter from input to output is important, for example forward clocked interfaces. PLLs are good for applications requiring the lowest output jitter or jitter filtering. All DLL outputs are routed as primary/edge clock sources.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. LOCK output signal is asserted when the DLL is locked. The ALU HOLD signal setting allows users to freeze the DLL at its current delay setting.

*Table 2-10. Supported Output Standards[4]*

| Output Standard | Drive | $V_{CCIO}$ (Nom) | On-chip Output Termination |
|---|---|---|---|
| **Single-ended Interfaces** | | | |
| LVTTL/D[1] | 8mA, 16mA, 24mA | 3.3 | None. |
| LVCMOS33/D[1] | 8mA, 16mA, 24mA | 3.3 | None |
| LVCMOS25/D[1, 2] | 4mA, 8mA, 12mA, 16mA, | 2.5 | None, series: 25, 33, 50, 100 |
| LVCMOS18/D[1, 2] | 4mA, 8mA, 12mA, 16mA, | 1.8 | None, series: 25, 33, 50, 100 |
| LVCMOS15/D[1, 2] | 4mA, 8mA, 12mA, 16mA, | 1.5 | None, series: 25, 33, 50, 100 |
| LVCMOS12/D[1, 2] | 2mA, 4mA, 8mA, 12mA | 1.2 | None, series: 25, 33, 50, 100 |
| PCIX15 | N/A | 1.5 | None |
| PCI33, PCIX33, AGP1X33, AGP2X33 | N/A | 3.3 | None |
| HSTL18_I | N/A | 1.8 | None, series: 50 |
| HSTL18_II | N/A | 1.8 | None, series: 25, series + parallel to $V_{CCIO}$/2: 25 + 60 |
| HSTL15_I | N/A | 1.5 | None, series: 50 |
| HSTL15_II | N/A | 1.5 | None, series: 25, series + parallel to $V_{CCIO}$/2: 25 + 60 |
| SSTL33_I | N/A | 3.3 | None |
| SSTL33_II | N/A | 3.3 | None |
| SSTL25_I | N/A | 2.5 | None, series: 50 |
| SSTL25_II | N/A | 2.5 | None, series: 33, series + parallel to $V_{CCIO}$/2: 33+ 60 |
| SSTL18_ I | N/A | 1.8 | None, series: 33 |
| SSTL18_II | N/A | 1.8 | None, series: 33, series + parallel to $V_{CCIO}$/2: 33+ 60 |
| **Differential Interfaces** | | | |
| SSTL18D_I | N/A | 1.8 | None, series: 33 |
| SSTL25D_I | N/A | 2.5 | None, series: 50 |
| SSTL18D_II, SSTL25D_II | N/A | 1.2/2.5/3.3 | None, series: 33, series + parallel to $V_{CCIO}$/2: 33+ 60 |
| SSTL33D_I, II | N/A | 3.3 | None |
| HSTL15D_I, HSTL18D_I | N/A | 1.5/1.8 | None, series: 50 |
| HST15D_II, HSTL18D_II | N/A | 1.5/1.8 | None, series: 25, series + parallel to $V_{CCIO}$/2: 25 + 60 |
| LVDS | 2mA, 3.5mA, 4mA, 6mA | N/A | None |
| Mini-LVDS | 3.5mA, 4mA, 6mA | N/A | None |
| BLVDS25 | N/A | N/A | None |
| MLVDS25 | N/A | N/A | None |
| LVPECL33[3] | N/A | 3.3 | None |
| RSDS | 2mA, 3.5mA, 4mA, 6mA | N/A | None |

1. D refers to open drain capability.
2. User can select either drive current or driver impedances but not both.
3. Emulated with external resistors.
4. No GTL or GTL+ support.

## PCI Clamp

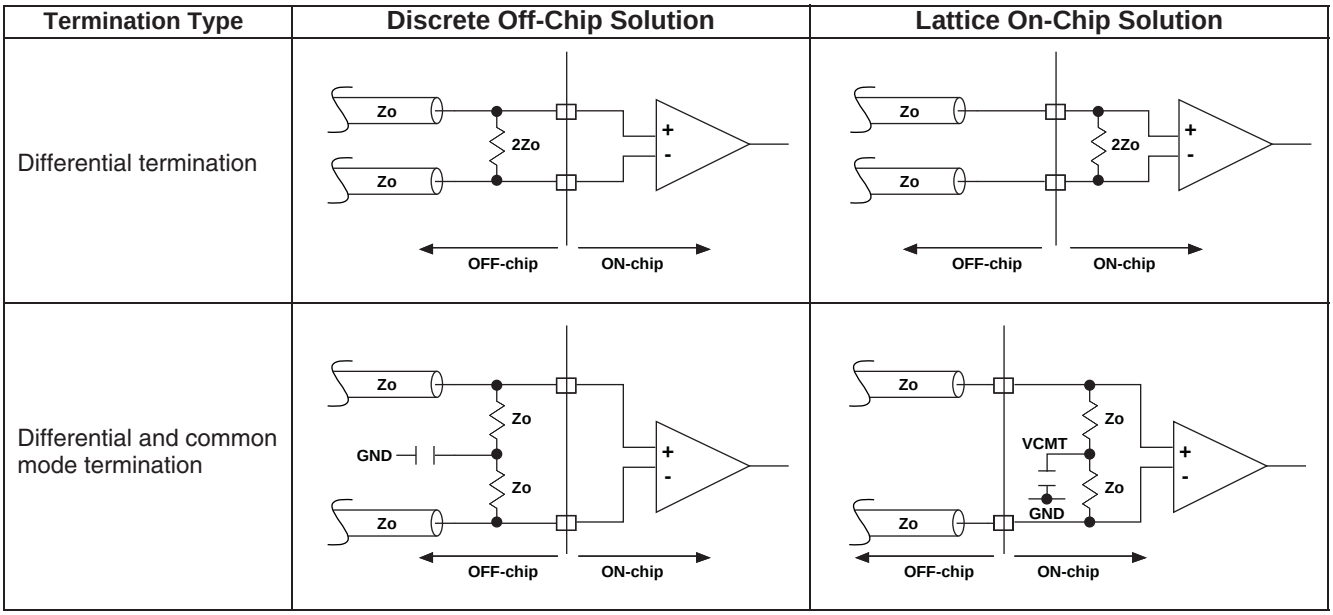
A programmable PCI clamp is available on the top and bottom banks of the device. The PCI clamp can be turned “ON” or “OFF” on each pin independently. The PCI clamp is used when implementing a 3.3V PCI interface. The

**Differential Input Termination**

The LatticeSC device allows two types of differential termination. The first is a single resistor across the differential inputs. The second is a center-tapped system where each input is terminated to the on-chip termination bus $V_{CMT}$. The $V_{CMT}$ bus is DC-coupled through an internal capacitor to ground.

Figure 2-29 shows the differential termination schemes and Table 2-9 shows the nominal values of the termination resistors.

***Figure 2-29. Differential Termination Scheme***




**Calibration**

There are two calibration sources that are associated with the termination scheme used in the LatticeSC devices:

- DIFFR – This pin occurs in each bank that supports differential drivers and must be connected through a 1K+/-1% resistor to ground if differential outputs are used. Note that differential drivers are not supported in banks 1, 4 and 5.
- XRES – There is one of these pins per device. It is used for several functions including calibrating on-chip termination. This pin should always be connected through a 1K+/-1% resistor to ground.

The LatticeSC devices support two modes of calibration:

- Continuous – In this mode the SC devices continually calibrate the termination resistances. Calibration happens several times a second. Using this mode ensures that termination resistances remain calibrated as the silicon junction temperature changes.
- User Request – In this mode the calibration circuit operates continuously. However, the termination resistor values are only updated on the assertion of the calibration_update signal available to the core logic.

For more information on calibration, refer to the details of additional technical documentation at the end of this data sheet.

## Hot Socketing

The LatticeSC devices have been carefully designed to ensure predictable behavior during power-up and power-down. To ensure proper power sequencing, care must be taken during power-up and power-down as described below. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits,

# PURESPEED I/O Differential Electrical Characteristics

## LVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input voltage | | 0 | — | 2.4 | V |
| $V_{THD}$ | Differential input threshold (Q-$\overline{Q}$) | | +/-100 | — | — | mV |
| $V_{CM}$ | Input common mode voltage | | 0.05 | 1.2 | 2.35 | V |
| $I_{IN}$ | Input current | Power on or power off | — | — | +/-10 | µA |
| $V_{OH}$ | Output high voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | — | 1.38 | 1.60 | V |
| $V_{OL}$ | Output low voltage for $V_{OP}$ or $V_{OM}$ | $R_T$ = 100 Ohm | 0.9V | 1.03 | — | V |
| $V_{OD}$ | Output voltage differential | ($V_{OP}$ - $V_{OM}$), $R_T$ = 100 Ohm | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | | — | — | 50 | mV |
| $V_{OS}$ | Output voltage offset | ($V_{OP}$ - $V_{OM}$)/2, $R_T$ = 100 Ohm | 1.125 | 1.20 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between H and L | | — | — | 50 | mV |
| $I_{SAB}$ | Output short circuit current | $V_{OD}$ = 0V Driver outputs shorted | — | — | 12 | mA |
| $T_R$, $T_F$ | Output rise and fall times, 20% to 80% | — | — | 500 | ps | $T_R$, $T_F$ |

Notes:
1. Data is for 3.5mA differential current drive. Other differential driver current options are available.
2. If the low power mode of the input buffer is used, the minimum $V_{CM}$ is 600 mV.

## Mini-LVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $Z_O$ | Single-ended PCB trace impedance | 30 | 50 | 75 | ohms |
| $R_T$ | Differential termination resistance | 60 | 100 | 150 | ohms |
| $V_{OD}$ | Output voltage, differential, $\|V_{OP} - V_{OM}\|$ | 300 | — | 600 | mV |
| $V_{OS}$ | Output voltage, common mode, $\|V_{OP} + V_{OM}\|/2$ | 1 | 1.2 | 1.4 | V |
| $\Delta V_{OD}$ | Change in $V_{OD}$, between H and L | — | — | 50 | mV |
| $\Delta V_{ID}$ | Change in $V_{OS}$, between H and L | — | — | 50 | mV |
| $V_{THD}$ | Input voltage, differential, $\|V_{INP} - V_{INM}\|$ | 200 | — | 600 | mV |
| $V_{CM}$ | Input voltage, common mode, $\|V_{INP} + V_{INM}\|/2$ | 0.3+($V_{THD}$/2) | — | 2.1-($V_{THD}$/2) | |
| $T_R$, $T_F$ | Output rise and fall times, 20% to 80% | — | — | 500 | ps |
| $T_{ODUTY}$ | Output clock duty cycle | 45 | — | 55 | % |
| $T_{IDUTY}$ | Input clock duty cycle | 40 | — | 60 | % |

Note: Data is for 6mA differential current drive. Other differential driver current options are available.

*Figure 3-12. Waveforms First Read after Full Flag*

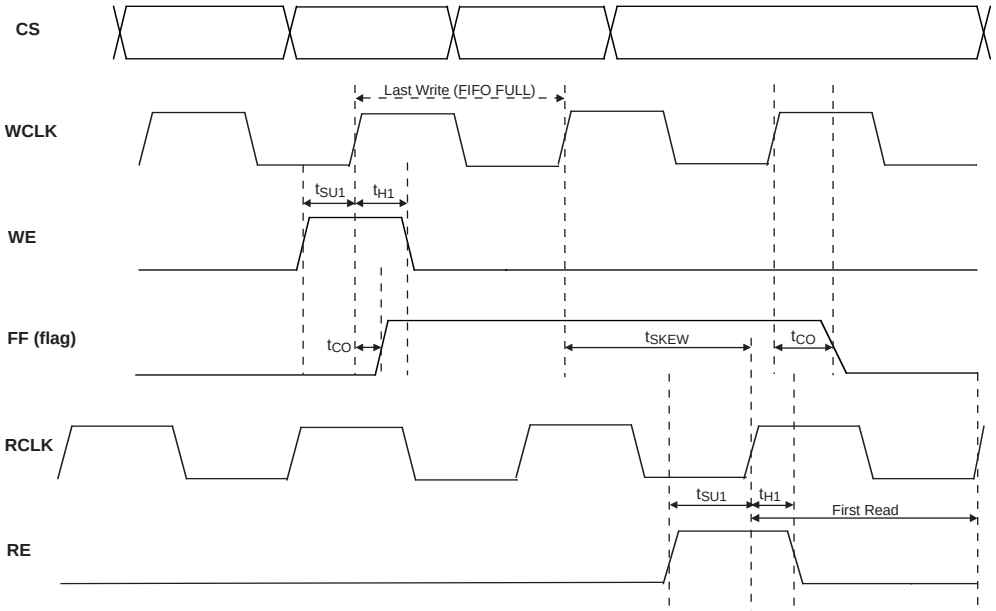
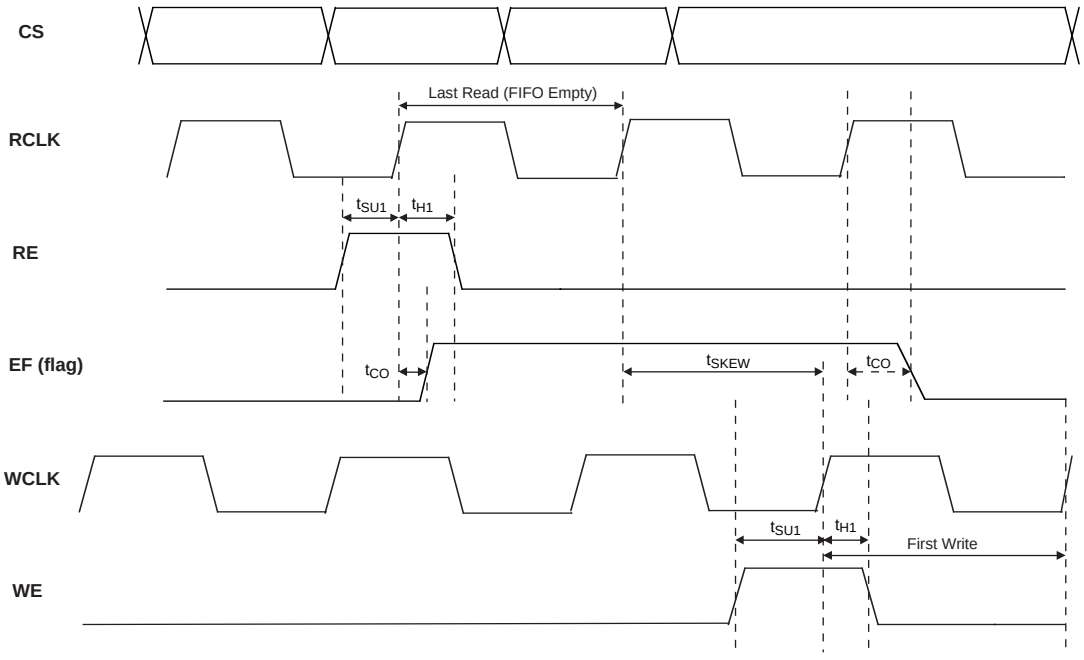



*Figure 3-13. Waveform First Write after Empty Flag*



## Signal Descriptions

| Signal Name | I/O | Description |
|---|---|---|
| **General Purpose** | | |
| P[Edge] [Row/Column Number*]_[A/B/C/D] | I/O | [Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).<br><br>[Row/Column Number] indicates the PIC row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.<br><br>[A/B/C/D] indicates the PIO within the PIC to which the pad is connected.<br><br>Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic.<br><br>During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. |
| VREF1_x, VREF2_x | — | The reference supply pins for I/O bank x. Any I/O pin in a bank can be assigned as a reference supply pin, but software defaults use designated pin. |
| NC | — | No connect. NC pins should not be connected to any active signals, VCC or GND. |
| **Non-SERDES Power Supplies** | | |
| VCCIOx | — | VCCIO - The power supply pins for I/O bank x. Dedicated pins. |
| VCC12[1] | — | 1.2V supply for configuration logic, PLLs and SERDES Rx, Tx and PLL. All VCC12 pins must be connected. As VCC12 supplies power for analog circuitry, VCC12 should be quiet and isolated from noisy digital board supplies. |
| VTT_x | — | Termination voltage for bank x. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float. |
| GND | — | GND - Ground. Dedicated pins. All grounds must be electrically connected at the board level. |
| VCC | — | VCC - The power supply pins for core logic. Dedicated pins (1.2V/ 1.0V). |
| VCCAUX | — | VCCAUX - Auxiliary power supply pin - powers all differential and referenced input buffers. Dedicated pins (2.5V). |
| VCCJ | — | VCCJ - The power supply pin for JTAG Test Access Port. |
| PROBE_VCC | — | VCC signal - Connected to internal VCC node. Can be used for feedback to control an external board power converter. Can be unconnected if not used. |

## Pin Information Summary

| Pin Type | | 256 fpBGA | 900 fpBGA | | 1020 fcBGA | |
|---|---|---|---|---|---|---|
| | | LFSC/M15 | LFSC/M15 | LFSC/M25 | LFSC/M25 | LFSC/M40 |
| Single Ended User I/O | | 139 | 300 | 378 | 476 | 562 |
| Differential Pair User I/O | | 60 | 141 | 182 | 235 | 277 |
| LVDS Output Pairs | | 22 | 44 | 60 | 60 | 78 |
| Configuration | Dedicated | 9 | 11 | 11 | 11 | 11 |
| | Muxes/MPI sysBus | 0 | 55 | 55 | 55 | 72 |
| JTAG (excluding VCCJ) | | 4 | 4 | 4 | 4 | 4 |
| Dedicated Pins | | 2 | 4 | 4 | 4 | 4 |
| VCC | | 10 | 46 | 46 | 40 | 40 |
| VCC12 | | 10 | 35 | 35 | 36 | 36 |
| VCCAUX | | 10 | 36 | 36 | 32 | 32 |
| VCCIO | Bank 1 | 3 | 18 | 18 | 10 | 10 |
| | Bank 2 | 2 | 14 | 14 | 8 | 8 |
| | Bank 3 | 2 | 15 | 15 | 10 | 10 |
| | Bank 4 | 3 | 15 | 15 | 10 | 10 |
| | Bank 5 | 3 | 15 | 15 | 10 | 10 |
| | Bank 6 | 2 | 15 | 15 | 10 | 10 |
| | Bank 7 | 2 | 16 | 16 | 8 | 8 |
| VTT | Bank 2 | 0 | 2 | 2 | 2 | 2 |
| | Bank 3 | 0 | 3 | 3 | 3 | 3 |
| | Bank 4 | 0 | 3 | 3 | 3 | 3 |
| | Bank 5 | 0 | 3 | 3 | 3 | 3 |
| | Bank 6 | 0 | 3 | 3 | 3 | 3 |
| | Bank 7 | 0 | 2 | 2 | 2 | 2 |
| GND | | 26 | 177 | 177 | 134 | 134 |
| NC | | 0 | 102 | 24 | 92 | 6 |
| Single Ended User / Differential I/O per Bank | Bank 1 | 21/8 | 63/30 | 63/30 | 68/32 | 68/32 |
| | Bank 2 | 15/7 | 26/13 | 30/15 | 34/17 | 54/27 |
| | Bank 3 | 19/8 | 43/20 | 62/29 | 84/42 | 94/47 |
| | Bank 4 | 25/11 | 50/22 | 66/32 | 84/41 | 99/48 |
| | Bank 5 | 25/11 | 49/23 | 65/32 | 88/44 | 99/49 |
| | Bank 6 | 19/8 | 43/20 | 62/29 | 84/42 | 94/47 |
| | Bank 7 | 15/7 | 26/13 | 30/15 | 34/17 | 54/27 |
| LVDS Output Pairs Per Bank | Bank 2 | 5 | 7 | 9 | 9 | 15 |
| | Bank 3 | 6 | 15 | 21 | 21 | 24 |
| | Bank 6 | 6 | 15 | 21 | 21 | 24 |
| | Bank 7 | 5 | 7 | 9 | 9 | 15 |
| VCCJ | | 1 | 1 | 1 | 1 | 1 |
| SERDES (signal + power supply) | | 28 | 60 | 60 | 108 | 108 |
| Total | | 256 | 900 | 900 | 1020 | 1152 |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| Y24 | PL48C | 6 | | PL61C | 6 | |
| Y23 | PL48D | 6 | | PL61D | 6 | |
| AD29 | PL49A | 6 | | PL62A | 6 | |
| AD30 | PL49B | 6 | | PL62B | 6 | |
| AF28 | PL49C | 6 | | PL62C | 6 | |
| AE28 | PL49D | 6 | | PL62D | 6 | |
| AC28 | PL51A | 6 | | PL65A | 6 | |
| AD28 | PL51B | 6 | | PL65B | 6 | |
| AB26 | PL51C | 6 | | PL65C | 6 | |
| AC26 | PL51D | 6 | VREF2_6 | PL65D | 6 | VREF2_6 |
| AC32 | PL52A | 6 | | PL66A | 6 | |
| AD32 | PL52B | 6 | | PL66B | 6 | |
| AA24 | PL52C | 6 | | PL66C | 6 | |
| AA23 | PL52D | 6 | | PL66D | 6 | |
| AE30 | PL53A | 6 | | PL67A | 6 | |
| AE29 | PL53B | 6 | | PL67B | 6 | |
| AC25 | PL53C | 6 | | PL67C | 6 | |
| AB25 | PL53D | 6 | | PL67D | 6 | |
| AE31 | PL55A | 6 | | PL69A | 6 | |
| AE32 | PL55B | 6 | | PL69B | 6 | |
| AE26 | PL55C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F | PL69C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F |
| AE27 | PL55D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F | PL69D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F |
| AF32 | PL56A | 6 | | PL70A | 6 | |
| AF31 | PL56B | 6 | | PL70B | 6 | |
| AC24 | PL56C | 6 | | PL70C | 6 | |
| AD25 | PL56D | 6 | | PL70D | 6 | |
| AG32 | PL57A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E | PL71A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E |
| AG31 | PL57B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E | PL71B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E |
| AC23 | PL57C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A | PL71C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A |
| AD24 | PL57D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A | PL71D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A |
| AH32 | XRES | - | | XRES | - | |
| AH31 | TEMP | 6 | | TEMP | 6 | |
| AJ32 | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B |
| AK32 | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B |
| AF27 | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| AG28 | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| AK31 | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C |
| AL31 | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C |
| AE25 | PB4C | 5 | | PB4C | 5 | |
| AE24 | PB4D | 5 | | PB4D | 5 | |
| AK30 | PB5A | 5 | | PB5A | 5 | |
| AL30 | PB5B | 5 | | PB5B | 5 | |
| AD23 | PB5C | 5 | | PB5C | 5 | |
| AE23 | PB5D | 5 | VREF1_5 | PB5D | 5 | VREF1_5 |
| AK29 | PB7A | 5 | | PB7A | 5 | |
| AL29 | PB7B | 5 | | PB7B | 5 | |
| AF26 | PB7C | 5 | | PB7C | 5 | |
| AF25 | PB7D | 5 | | PB7D | 5 | |
| AJ28 | PB8A | 5 | | PB8A | 5 | |
| AK28 | PB8B | 5 | | PB8B | 5 | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AD29 | PL60D | 6 | | PL84D | 6 | |
| AE31 | PL61A | 6 | | PL85A | 6 | |
| AF31 | PL61B | 6 | | PL85B | 6 | |
| AF30 | PL61C | 6 | | PL85C | 6 | |
| AF29 | PL61D | 6 | | PL85D | 6 | |
| AH33 | PL62A | 6 | | PL86A | 6 | |
| AJ33 | PL62B | 6 | | PL86B | 6 | |
| AC28 | PL62C | 6 | | PL86C | 6 | |
| AD28 | PL62D | 6 | | PL86D | 6 | |
| AH32 | PL65A | 6 | | PL89A | 6 | |
| AJ32 | PL65B | 6 | | PL89B | 6 | |
| AD27 | PL65C | 6 | | PL89C | 6 | |
| AE27 | PL65D | 6 | VREF2_6 | PL89D | 6 | VREF2_6 |
| AG34 | PL66A | 6 | | PL90A | 6 | |
| AH34 | PL66B | 6 | | PL90B | 6 | |
| AC26 | PL66C | 6 | | PL90C | 6 | |
| AB26 | PL66D | 6 | | PL90D | 6 | |
| AK33 | PL67A | 6 | | PL91A | 6 | |
| AL33 | PL67B | 6 | | PL91B | 6 | |
| AG30 | PL67C | 6 | | PL91C | 6 | |
| AH30 | PL67D | 6 | | PL91D | 6 | |
| AL34 | PL69A | 6 | | PL93A | 6 | |
| AM34 | PL69B | 6 | | PL93B | 6 | |
| AJ30 | PL69C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F | PL93C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F |
| AK30 | PL69D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F | PL93D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F |
| AJ31 | PL70A | 6 | | PL94A | 6 | |
| AH31 | PL70B | 6 | | PL94B | 6 | |
| AD26 | PL70C | 6 | | PL94C | 6 | |
| AD25 | PL70D | 6 | | PL94D | 6 | |
| AL32 | PL71A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E | PL95A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E |
| AL31 | PL71B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E | PL95B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E |
| AG29 | PL71C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A | PL95C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A |
| AG28 | PL71D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A | PL95D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A |
| AF28 | XRES | - | | XRES | - | |
| AF27 | TEMP | 6 | | TEMP | 6 | |
| AM33 | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B |
| AN33 | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B |
| AH29 | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| AJ29 | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| AM32 | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C |
| AM31 | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C |
| AG27 | PB4C | 5 | | PB4C | 5 | |
| AG26 | PB4D | 5 | | PB4D | 5 | |
| AL29 | PB5A | 5 | | PB5A | 5 | |
| AL28 | PB5B | 5 | | PB5B | 5 | |

## LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AJ9 | PB78C | 4 | | PB117C | 4 | |
| AJ8 | PB78D | 4 | | PB117D | 4 | |
| AP3 | PB79A | 4 | | PB119A | 4 | |
| AN3 | PB79B | 4 | | PB119B | 4 | |
| AF10 | PB79C | 4 | | PB119C | 4 | |
| AE10 | PB79D | 4 | | PB119D | 4 | |
| AL7 | PB81A | 4 | | PB121A | 4 | |
| AL6 | PB81B | 4 | | PB121B | 4 | |
| AK7 | PB81C | 4 | | PB121C | 4 | |
| AK6 | PB81D | 4 | | PB121D | 4 | |
| AN5 | PB82A | 4 | | PB123A | 4 | |
| AN4 | PB82B | 4 | | PB123B | 4 | |
| AH9 | PB82C | 4 | VREF1_4 | PB123C | 4 | VREF1_4 |
| AH8 | PB82D | 4 | | PB123D | 4 | |
| AM3 | PB83A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D | PB124A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D |
| AM4 | PB83B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D | PB124B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D |
| AG9 | PB83C | 4 | | PB124C | 4 | |
| AG8 | PB83D | 4 | | PB124D | 4 | |
| AN2 | PB85A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B | PB125A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B |
| AM2 | PB85B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B | PB125B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B |
| AJ6 | PB85C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C | PB125C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C |
| AH6 | PB85D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C | PB125D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C |
| AF7 | PROBE_VCC | - | | PROBE_VCC | - | |
| AF8 | PROBE_GND | - | | PROBE_GND | - | |
| AG7 | PR71D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A | PR95D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A |
| AG6 | PR71C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A | PR95C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A |
| AL4 | PR71B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E | PR95B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E |
| AL3 | PR71A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E | PR95A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E |
| AD10 | PR70D | 3 | | PR94D | 3 | |
| AD9 | PR70C | 3 | | PR94C | 3 | |
| AH4 | PR70B | 3 | | PR94B | 3 | |
| AJ4 | PR70A | 3 | | PR94A | 3 | |
| AK5 | PR69D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F | PR93D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F |
| AJ5 | PR69C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F | PR93C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F |
| AM1 | PR69B | 3 | | PR93B | 3 | |
| AL1 | PR69A | 3 | | PR93A | 3 | |
| AH5 | PR67D | 3 | | PR91D | 3 | |
| AG5 | PR67C | 3 | | PR91C | 3 | |
| AL2 | PR67B | 3 | | PR91B | 3 | |
| AK2 | PR67A | 3 | | PR91A | 3 | |
| AB9 | PR66D | 3 | | PR90D | 3 | |
| AC9 | PR66C | 3 | | PR90C | 3 | |
| AH1 | PR66B | 3 | | PR90B | 3 | |
| AG1 | PR66A | 3 | | PR90A | 3 | |
| AE8 | PR65D | 3 | VREF2_3 | PR89D | 3 | VREF2_3 |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| F15 | PT55A | 1 | D5/MPI_DATA5 | PT74A | 1 | D5/MPI_DATA5 |
| K14 | PT54D | 1 | D4/MPI_DATA4 | PT73D | 1 | D4/MPI_DATA4 |
| K13 | PT54C | 1 | D3/MPI_DATA3 | PT73C | 1 | D3/MPI_DATA3 |
| B15 | PT53B | 1 | D2/MPI_DATA2 | PT73B | 1 | D2/MPI_DATA2 |
| A15 | PT53A | 1 | D1/MPI_DATA1 | PT73A | 1 | D1/MPI_DATA1 |
| J14 | PT51D | 1 | D16/PCLKC1_3/MPI_DATA16 | PT71D | 1 | D16/PCLKC1_3/MPI_DATA16 |
| H14 | PT51C | 1 | D17/PCLKT1_3/MPI_DATA17 | PT71C | 1 | D17/PCLKT1_3/MPI_DATA17 |
| A16 | PT51B | 1 | D0/MPI_DATA0 | PT71B | 1 | D0/MPI_DATA0 |
| B16 | PT51A | 1 | QOUT/CEON | PT71A | 1 | QOUT/CEON |
| J13 | PT50D | 1 | VREF2_1 | PT70D | 1 | VREF2_1 |
| H13 | PT50C | 1 | D18/MPI_DATA18 | PT70C | 1 | D18/MPI_DATA18 |
| D15 | PT50B | 1 | DOUT | PT70B | 1 | DOUT |
| E15 | PT50A | 1 | MCA_DONE_IN | PT70A | 1 | MCA_DONE_IN |
| J16 | PT49D | 1 | D19/PCLKC1_2/MPI_DATA19 | PT69D | 1 | D19/PCLKC1_2/MPI_DATA19 |
| J17 | PT49C | 1 | D20/PCLKT1_2/MPI_DATA20 | PT69C | 1 | D20/PCLKT1_2/MPI_DATA20 |
| D16 | PT49B | 1 | MCA_CLK_P1_OUT | PT69B | 1 | MCA_CLK_P1_OUT |
| E16 | PT49A | 1 | MCA_CLK_P1_IN | PT69A | 1 | MCA_CLK_P1_IN |
| H15 | PT47D | 1 | D21/PCLKC1_1/MPI_DATA21 | PT67D | 1 | D21/PCLKC1_1/MPI_DATA21 |
| H16 | PT47C | 1 | D22/PCLKT1_1/MPI_DATA22 | PT67C | 1 | D22/PCLKT1_1/MPI_DATA22 |
| C15 | PT47B | 1 | MCA_CLK_P2_OUT | PT67B | 1 | MCA_CLK_P2_OUT |
| C16 | PT47A | 1 | MCA_CLK_P2_IN | PT67A | 1 | MCA_CLK_P2_IN |
| L17 | PT46D | 1 | MCA_DONE_OUT | PT66D | 1 | MCA_DONE_OUT |
| K17 | PT46C | 1 | BUSYN/RCLK/SCK | PT66C | 1 | BUSYN/RCLK/SCK |
| E17 | PT46B | 1 | DP0/MPI_PAR0 | PT66B | 1 | DP0/MPI_PAR0 |
| F17 | PT46A | 1 | MPI_TA | PT66A | 1 | MPI_TA |
| G17 | PT45D | 1 | D23/MPI_DATA23 | PT65D | 1 | D23/MPI_DATA23 |
| H17 | PT45C | 1 | DP2/MPI_PAR2 | PT65C | 1 | DP2/MPI_PAR2 |
| A17 | PT45B | 1 | PCLKC1_0 | PT65B | 1 | PCLKC1_0 |
| B17 | PT45A | 1 | PCLKT1_0/MPI_CLK | PT65A | 1 | PCLKT1_0/MPI_CLK |
| G18 | PT43D | 1 | DP3/PCLKC1_4/MPI_PAR3 | PT63D | 1 | DP3/PCLKC1_4/MPI_PAR3 |
| H18 | PT43C | 1 | D24/PCLKT1_4/MPI_DATA24 | PT63C | 1 | D24/PCLKT1_4/MPI_DATA24 |
| E18 | PT43B | 1 | MPI_RETRY | PT63B | 1 | MPI_RETRY |
| F18 | PT43A | 1 | A0/MPI_ADDR14 | PT63A | 1 | A0/MPI_ADDR14 |
| J18 | PT42D | 1 | A1/MPI_ADDR15 | PT61D | 1 | A1/MPI_ADDR15 |
| J19 | PT42C | 1 | A2/MPI_ADDR16 | PT61C | 1 | A2/MPI_ADDR16 |
| C20 | PT42B | 1 | A3/MPI_ADDR17 | PT61B | 1 | A3/MPI_ADDR17 |
| C19 | PT42A | 1 | A4/MPI_ADDR18 | PT61A | 1 | A4/MPI_ADDR18 |
| K18 | PT41D | 1 | D25/PCLKC1_5/MPI_DATA25 | PT60D | 1 | D25/PCLKC1_5/MPI_DATA25 |
| L18 | PT41C | 1 | D26/PCLKT1_5/MPI_DATA26 | PT60C | 1 | D26/PCLKT1_5/MPI_DATA26 |
| D19 | PT41B | 1 | A5/MPI_ADDR19 | PT60B | 1 | A5/MPI_ADDR19 |
| E19 | PT41A | 1 | A6/MPI_ADDR20 | PT60A | 1 | A6/MPI_ADDR20 |
| H19 | PT39D | 1 | D27/MPI_DATA27 | PT59D | 1 | D27/MPI_DATA27 |
| H20 | PT39C | 1 | VREF1_1 | PT59C | 1 | VREF1_1 |
| A18 | PT39B | 1 | A7/MPI_ADDR21 | PT59B | 1 | A7/MPI_ADDR21 |
| B18 | PT39A | 1 | A8/MPI_ADDR22 | PT59A | 1 | A8/MPI_ADDR22 |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| W13 | VCCAUX | - | | VCCAUX | - | |
| W22 | VCCAUX | - | | VCCAUX | - | |
| Y21 | GND | - | | GND | - | |
| Y25 | GND | - | | GND | - | |
| C18 | VCCIO1 | - | | VCCIO1 | - | |
| D17 | VCCIO1 | - | | VCCIO1 | - | |
| F16 | VCCIO1 | - | | VCCIO1 | - | |
| G19 | VCCIO1 | - | | VCCIO1 | - | |
| J20 | VCCIO1 | - | | VCCIO1 | - | |
| K12 | VCCIO1 | - | | VCCIO1 | - | |
| K15 | VCCIO1 | - | | VCCIO1 | - | |
| L23 | VCCIO1 | - | | VCCIO1 | - | |
| Y9 | GND | - | | GND | - | |
| J9 | VCCIO1 | - | | VCCIO1 | - | |
| E3 | VCCIO2 | - | | VCCIO2 | - | |
| G6 | VCCIO2 | - | | VCCIO2 | - | |
| H4 | VCCIO2 | - | | VCCIO2 | - | |
| K7 | VCCIO2 | - | | VCCIO2 | - | |
| L3 | VCCIO2 | - | | VCCIO2 | - | |
| M11 | VCCIO2 | - | | VCCIO2 | - | |
| N6 | VCCIO2 | - | | VCCIO2 | - | |
| P4 | VCCIO2 | - | | VCCIO2 | - | |
| R9 | VCCIO2 | - | | VCCIO2 | - | |
| AA3 | VCCIO3 | - | | VCCIO3 | - | |
| AB7 | VCCIO3 | - | | VCCIO3 | - | |
| AC10 | VCCIO3 | - | | VCCIO3 | - | |
| AD4 | VCCIO3 | - | | VCCIO3 | - | |
| AE6 | VCCIO3 | - | | VCCIO3 | - | |
| AG3 | VCCIO3 | - | | VCCIO3 | - | |
| AK4 | VCCIO3 | - | | VCCIO3 | - | |
| T7 | VCCIO3 | - | | VCCIO3 | - | |
| U3 | VCCIO3 | - | | VCCIO3 | - | |
| V4 | VCCIO3 | - | | VCCIO3 | - | |
| W6 | VCCIO3 | - | | VCCIO3 | - | |
| Y10 | VCCIO3 | - | | VCCIO3 | - | |
| AD12 | VCCIO4 | - | | VCCIO4 | - | |
| AF15 | VCCIO4 | - | | VCCIO4 | - | |
| AF9 | VCCIO4 | - | | VCCIO4 | - | |
| AH10 | VCCIO4 | - | | VCCIO4 | - | |
| AH16 | VCCIO4 | - | | VCCIO4 | - | |
| AJ13 | VCCIO4 | - | | VCCIO4 | - | |
| AJ7 | VCCIO4 | - | | VCCIO4 | - | |
| AL14 | VCCIO4 | - | | VCCIO4 | - | |
| AL8 | VCCIO4 | - | | VCCIO4 | - | |
| AM11 | VCCIO4 | - | | VCCIO4 | - | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| AL4 | PR117B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E |
| AL3 | PR117A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E |
| AD10 | PR116D | 3 | |
| AD9 | PR116C | 3 | |
| AH4 | PR116B | 3 | |
| AJ4 | PR116A | 3 | |
| AK5 | PR115D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F |
| AJ5 | PR115C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F |
| AM1 | PR115B | 3 | |
| AL1 | PR115A | 3 | |
| AH5 | PR112D | 3 | |
| AG5 | PR112C | 3 | |
| AL2 | PR112B | 3 | |
| AK2 | PR112A | 3 | |
| AB9 | PR109D | 3 | |
| AC9 | PR109C | 3 | |
| AH1 | PR109B | 3 | |
| AG1 | PR109A | 3 | |
| AE8 | PR107D | 3 | VREF2_3 |
| AD8 | PR107C | 3 | |
| AJ3 | PR107B | 3 | |
| AH3 | PR107A | 3 | |
| AD7 | PR104D | 3 | |
| AC7 | PR104C | 3 | |
| AJ2 | PR104B | 3 | |
| AH2 | PR104A | 3 | |
| AF6 | PR103D | 3 | |
| AF5 | PR103C | 3 | |
| AF4 | PR103B | 3 | |
| AE4 | PR103A | 3 | |
| AD6 | PR99D | 3 | |
| AC6 | PR99C | 3 | |
| AG2 | PR99B | 3 | |
| AF2 | PR99A | 3 | |
| AC8 | PR98D | 3 | |
| AB8 | PR98C | 3 | |
| AK1 | PR98B | 3 | |
| AJ1 | PR98A | 3 | |
| AB10 | PR96D | 3 | |
| AA10 | PR96C | 3 | |
| AF3 | PR96B | 3 | |
| AE3 | PR96A | 3 | |
| AE5 | PR94D | 3 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AF40 | PL76A | 6 | | PL90A | 6 | |
| AG40 | PL76B | 6 | | PL90B | 6 | |
| AG36 | PL76C | 6 | | PL90C | 6 | |
| AH36 | PL76D | 6 | DIFFR_6 | PL90D | 6 | DIFFR_6 |
| AF39 | PL77A | 6 | | PL91A | 6 | |
| AG39 | PL77B | 6 | | PL91B | 6 | |
| AF29 | PL77C | 6 | | PL91C | 6 | |
| AG29 | PL77D | 6 | | PL91D | 6 | |
| AH42 | PL78A | 6 | | PL92A | 6 | |
| AG42 | PL78B | 6 | | PL92B | 6 | |
| AG35 | PL78C | 6 | | PL92C | 6 | |
| AH35 | PL78D | 6 | | PL92D | 6 | |
| AG41 | PL80A | 6 | | PL94A | 6 | |
| AH41 | PL80B | 6 | | PL94B | 6 | |
| AG34 | PL80C | 6 | | PL94C | 6 | |
| AH34 | PL80D | 6 | | PL94D | 6 | |
| AJ42 | PL81A | 6 | | PL96A | 6 | |
| AK42 | PL81B | 6 | | PL96B | 6 | |
| AG33 | PL81C | 6 | | PL96C | 6 | |
| AH33 | PL81D | 6 | | PL96D | 6 | |
| AJ41 | PL82A | 6 | | PL98A | 6 | |
| AK41 | PL82B | 6 | | PL98B | 6 | |
| AJ37 | PL82C | 6 | | PL98C | 6 | |
| AK37 | PL82D | 6 | | PL98D | 6 | |
| AJ40 | PL84A | 6 | | PL99A | 6 | |
| AK40 | PL84B | 6 | | PL99B | 6 | |
| AJ34 | PL84C | 6 | | PL99C | 6 | |
| AK34 | PL84D | 6 | | PL99D | 6 | |
| AJ38 | PL85A | 6 | | PL103A | 6 | |
| AK38 | PL85B | 6 | | PL103B | 6 | |
| AH32 | PL85C | 6 | | PL103C | 6 | |
| AJ32 | PL85D | 6 | | PL103D | 6 | |
| AL42 | PL86A | 6 | | PL104A | 6 | |
| AM42 | PL86B | 6 | | PL104B | 6 | |
| AK36 | PL86C | 6 | | PL104C | 6 | |
| AL36 | PL86D | 6 | | PL104D | 6 | |
| AL38 | PL89A | 6 | | PL107A | 6 | |
| AM38 | PL89B | 6 | | PL107B | 6 | |
| AJ33 | PL89C | 6 | | PL107C | 6 | |
| AK33 | PL89D | 6 | VREF2_6 | PL107D | 6 | VREF2_6 |
| AN42 | PL90A | 6 | | PL109A | 6 | |
| AP42 | PL90B | 6 | | PL109B | 6 | |
| AH31 | PL90C | 6 | | PL109C | 6 | |
| AJ31 | PL90D | 6 | | PL109D | 6 | |
| AN41 | PL91A | 6 | | PL112A | 6 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AP8 | PB117D | 4 | | PB131D | 4 | |
| AY3 | PB119A | 4 | | PB133A | 4 | |
| AW3 | PB119B | 4 | | PB133B | 4 | |
| AR6 | PB119C | 4 | | PB133C | 4 | |
| AR5 | PB119D | 4 | | PB133D | 4 | |
| AU5 | PB120A | 4 | | PB134A | 4 | |
| AV5 | PB120B | 4 | | PB134B | 4 | |
| AL12 | PB120C | 4 | | PB134C | 4 | |
| AL11 | PB120D | 4 | | PB134D | 4 | |
| AV3 | PB121A | 4 | | PB135A | 4 | |
| AV4 | PB121B | 4 | | PB135B | 4 | |
| AN9 | PB121C | 4 | | PB135C | 4 | |
| AN8 | PB121D | 4 | | PB135D | 4 | |
| AW1 | PB123A | 4 | | PB138A | 4 | |
| AY1 | PB123B | 4 | | PB138B | 4 | |
| AK14 | PB123C | 4 | VREF1_4 | PB138C | 4 | VREF1_4 |
| AK13 | PB123D | 4 | | PB138D | 4 | |
| AV2 | PB124A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D | PB139A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D |
| AW2 | PB124B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D | PB139B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D |
| AM10 | PB124C | 4 | | PB139C | 4 | |
| AM9 | PB124D | 4 | | PB139D | 4 | |
| AV1 | PB125A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B | PB141A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B |
| AU1 | PB125B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B | PB141B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B |
| AL10 | PB125C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C | PB141C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C |
| AL9 | PB125D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C | PB141D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C |
| AT3 | PROBE_VCC | - | | PROBE_VCC | - | |
| AU2 | PROBE_GND | - | | PROBE_GND | - | |
| AP7 | PR95D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A | PR117D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A |
| AN7 | PR95C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A | PR117C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A |
| AR3 | PR95B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E | PR117B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E |
| AR4 | PR95A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E | PR117A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E |
| AP6 | PR94D | 3 | | PR116D | 3 | |
| AN6 | PR94C | 3 | | PR116C | 3 | |
| AT2 | PR94B | 3 | | PR116B | 3 | |
| AR2 | PR94A | 3 | | PR116A | 3 | |
| AM6 | PR93D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F | PR115D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F |
| AL6 | PR93C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F | PR115C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F |
| AP5 | PR93B | 3 | | PR115B | 3 | |
| AN5 | PR93A | 3 | | PR115A | 3 | |
| AL8 | PR91D | 3 | | PR112D | 3 | |
| AK8 | PR91C | 3 | | PR112C | 3 | |
| AP2 | PR91B | 3 | | PR112B | 3 | |
| AN2 | PR91A | 3 | | PR112A | 3 | |
| AJ12 | PR90D | 3 | | PR109D | 3 | |
| AH12 | PR90C | 3 | | PR109C | 3 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| H18 | PT77C | 1 | LDCN/SCS | PT93C | 1 | LDCN/SCS |
| F18 | PT77B | 1 | D8/MPI_DATA8 | PT93B | 1 | D8/MPI_DATA8 |
| E18 | PT77A | 1 | CS1/MPI_CS1 | PT93A | 1 | CS1/MPI_CS1 |
| H19 | PT75D | 1 | D9/MPI_DATA9 | PT90D | 1 | D9/MPI_DATA9 |
| G19 | PT75C | 1 | D10/MPI_DATA10 | PT90C | 1 | D10/MPI_DATA10 |
| D19 | PT75B | 1 | CS0N/MPI_CS0N | PT90B | 1 | CS0N/MPI_CS0N |
| D18 | PT75A | 1 | RDN/MPI_STRB_N | PT90A | 1 | RDN/MPI_STRB_N |
| J20 | PT74D | 1 | WRN/MPI_WR_N | PT89D | 1 | WRN/MPI_WR_N |
| K20 | PT74C | 1 | D7/MPI_DATA7 | PT89C | 1 | D7/MPI_DATA7 |
| E19 | PT74B | 1 | D6/MPI_DATA6 | PT89B | 1 | D6/MPI_DATA6 |
| F19 | PT74A | 1 | D5/MPI_DATA5 | PT89A | 1 | D5/MPI_DATA5 |
| K18 | PT73D | 1 | D4/MPI_DATA4 | PT87D | 1 | D4/MPI_DATA4 |
| J18 | PT73C | 1 | D3/MPI_DATA3 | PT87C | 1 | D3/MPI_DATA3 |
| A19 | PT73B | 1 | D2/MPI_DATA2 | PT87B | 1 | D2/MPI_DATA2 |
| B19 | PT73A | 1 | D1/MPI_DATA1 | PT87A | 1 | D1/MPI_DATA1 |
| H17 | PT71D | 1 | D16/PCLKC1_3/MPI_DATA16 | PT86D | 1 | D16/PCLKC1_3/MPI_DATA16 |
| J17 | PT71C | 1 | D17/PCLKT1_3/MPI_DATA17 | PT86C | 1 | D17/PCLKT1_3/MPI_DATA17 |
| B20 | PT71B | 1 | D0/MPI_DATA0 | PT86B | 1 | D0/MPI_DATA0 |
| C20 | PT71A | 1 | QOUT/CEON | PT86A | 1 | QOUT/CEON |
| M20 | PT70D | 1 | VREF2_1 | PT83D | 1 | VREF2_1 |
| L20 | PT70C | 1 | D18/MPI_DATA18 | PT83C | 1 | D18/MPI_DATA18 |
| F20 | PT70B | 1 | DOUT | PT83B | 1 | DOUT |
| G20 | PT70A | 1 | MCA_DONE_IN | PT83A | 1 | MCA_DONE_IN |
| K19 | PT69D | 1 | D19/PCLKC1_2/MPI_DATA19 | PT81D | 1 | D19/PCLKC1_2/MPI_DATA19 |
| J19 | PT69C | 1 | D20/PCLKT1_2/MPI_DATA20 | PT81C | 1 | D20/PCLKT1_2/MPI_DATA20 |
| D20 | PT69B | 1 | MCA_CLK_P1_OUT | PT81B | 1 | MCA_CLK_P1_OUT |
| E20 | PT69A | 1 | MCA_CLK_P1_IN | PT81A | 1 | MCA_CLK_P1_IN |
| H21 | PT67D | 1 | D21/PCLKC1_1/MPI_DATA21 | PT78D | 1 | D21/PCLKC1_1/MPI_DATA21 |
| G21 | PT67C | 1 | D22/PCLKT1_1/MPI_DATA22 | PT78C | 1 | D22/PCLKT1_1/MPI_DATA22 |
| B21 | PT67B | 1 | MCA_CLK_P2_OUT | PT78B | 1 | MCA_CLK_P2_OUT |
| C21 | PT67A | 1 | MCA_CLK_P2_IN | PT78A | 1 | MCA_CLK_P2_IN |
| M21 | PT66D | 1 | MCA_DONE_OUT | PT75D | 1 | MCA_DONE_OUT |
| L21 | PT66C | 1 | BUSYN/RCLK/SCK | PT75C | 1 | BUSYN/RCLK/SCK |
| A21 | PT66B | 1 | DP0/MPI_PAR0 | PT75B | 1 | DP0/MPI_PAR0 |
| A20 | PT66A | 1 | MPI_TA | PT75A | 1 | MPI_TA |
| J21 | PT65D | 1 | D23/MPI_DATA23 | PT73D | 1 | D23/MPI_DATA23 |
| K21 | PT65C | 1 | DP2/MPI_PAR2 | PT73C | 1 | DP2/MPI_PAR2 |
| E21 | PT65B | 1 | PCLKC1_0 | PT73B | 1 | PCLKC1_0 |
| F21 | PT65A | 1 | PCLKT1_0/MPI_CLK | PT73A | 1 | PCLKT1_0/MPI_CLK |
| G22 | PT63D | 1 | DP3/PCLKC1_4/MPI_PAR3 | PT71D | 1 | DP3/PCLKC1_4/MPI_PAR3 |
| H22 | PT63C | 1 | D24/PCLKT1_4/MPI_DATA24 | PT71C | 1 | D24/PCLKT1_4/MPI_DATA24 |
| A23 | PT63B | 1 | MPI_RETRY | PT71B | 1 | MPI_RETRY |
| A22 | PT63A | 1 | A0/MPI_ADDR14 | PT71A | 1 | A0/MPI_ADDR14 |
| L22 | PT61D | 1 | A1/MPI_ADDR15 | PT69D | 1 | A1/MPI_ADDR15 |
| M22 | PT61C | 1 | A2/MPI_ADDR16 | PT69C | 1 | A2/MPI_ADDR16 |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| T16 | GND | - | | GND | - | |
| T19 | GND | - | | GND | - | |
| T24 | GND | - | | GND | - | |
| T27 | GND | - | | GND | - | |
| T32 | GND | - | | GND | - | |
| U18 | GND | - | | GND | - | |
| U20 | GND | - | | GND | - | |
| U23 | GND | - | | GND | - | |
| U25 | GND | - | | GND | - | |
| U36 | GND | - | | GND | - | |
| U7 | GND | - | | GND | - | |
| G36 | GND | - | | GND | - | |
| G7 | GND | - | | GND | - | |
| V17 | GND | - | | GND | - | |
| V19 | GND | - | | GND | - | |
| V24 | GND | - | | GND | - | |
| V26 | GND | - | | GND | - | |
| V4 | GND | - | | GND | - | |
| V40 | GND | - | | GND | - | |
| W12 | GND | - | | GND | - | |
| W16 | GND | - | | GND | - | |
| W18 | GND | - | | GND | - | |
| W20 | GND | - | | GND | - | |
| W23 | GND | - | | GND | - | |
| W25 | GND | - | | GND | - | |
| W27 | GND | - | | GND | - | |
| W31 | GND | - | | GND | - | |
| Y17 | GND | - | | GND | - | |
| Y19 | GND | - | | GND | - | |
| Y21 | GND | - | | GND | - | |
| Y22 | GND | - | | GND | - | |
| AA17 | VCC | - | | VCC | - | |
| AA18 | VCC | - | | VCC | - | |
| AA19 | VCC | - | | VCC | - | |
| AA21 | VCC | - | | VCC | - | |
| AA22 | VCC | - | | VCC | - | |
| AA24 | VCC | - | | VCC | - | |
| AA25 | VCC | - | | VCC | - | |
| AA26 | VCC | - | | VCC | - | |
| AB17 | VCC | - | | VCC | - | |
| AB18 | VCC | - | | VCC | - | |
| AB19 | VCC | - | | VCC | - | |
| AB21 | VCC | - | | VCC | - | |
| AB22 | VCC | - | | VCC | - | |
| AB24 | VCC | - | | VCC | - | |

## Lead-Free Packaging

**Commercial**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA15E-7FN256C | -7 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSC3GA15E-6FN256C | -6 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSC3GA15E-5FN256C | -5 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSC3GA15E-7FN900C | -7 | Lead-Free fpBGA | 900 | COM | 15.2 |
| LFSC3GA15E-6FN900C | -6 | Lead-Free fpBGA | 900 | COM | 15.2 |
| LFSC3GA15E-5FN900C | -5 | Lead-Free fpBGA | 900 | COM | 15.2 |

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA15EP1-7FN256C | -7 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSCM3GA15EP1-6FN256C | -6 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSCM3GA15EP1-5FN256C | -5 | Lead-Free fpBGA | 256 | COM | 15.2 |
| LFSCM3GA15EP1-7FN900C | -7 | Lead-Free fpBGA | 900 | COM | 15.2 |
| LFSCM3GA15EP1-6FN900C | -6 | Lead-Free fpBGA | 900 | COM | 15.2 |
| LFSCM3GA15EP1-5FN900C | -5 | Lead-Free fpBGA | 900 | COM | 15.2 |

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA25E-7FN900C | -7 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSC3GA25E-6FN900C | -6 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSC3GA25E-5FN900C | -5 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSC3GA25E-7FFN1020C[1] | -7 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSC3GA25E-6FFN1020C[1] | -6 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSC3GA25E-5FFN1020C[1] | -5 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSC3GA25E-7FFAN1020C | -7 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSC3GA25E-6FFAN1020C | -6 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSC3GA25E-5FFAN1020C | -5 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA25EP1-7FN900C | -7 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSCM3GA25EP1-6FN900C | -6 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSCM3GA25EP1-5FN900C | -5 | Lead-Free fpBGA | 900 | COM | 25.4 |
| LFSCM3GA25EP1-7FFN1020C[1] | -7 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-6FFN1020C[1] | -6 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-5FFN1020C[1] | -5 | Lead-Free Organic fcBGA | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-7FFAN1020C | -7 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-6FFAN1020C | -6 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-5FFAN1020C | -5 | Lead-Free Organic fcBGA Revision 2 | 1020 | COM | 25.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2007 (cont.) | 01.5 (cont.) | DC and Switching Characteristics (cont.) | Updated LatticeSC Internal Timing Parameters with ispLEVER 6.1 SP1 results. |
| | | | Updated $t_{FDEL}$ and $t_{CDEL}$ specifications. |
| | | | Updated LatticeSC Family Timing Adders with ispLEVER 6.1 SP1 results. |
| | | | Updated PLL specifications to expand frequency range down to 2 MHz and break out jitter for the different ranges. |
| | | | Added footnote to sysCLOCK PLL Timing table specifying the conditions for the jitter measurements. |
| | | | Added $t_{DLL}$ specification to sysCLOCK DLL Timing table. |
| | | | Added footnote to sysCLOCK DLL Timing table specifying the conditions for the jitter measurements. |
| | | | Added sysCONFIG Master Parallel Configuration Mode and sysCONFIG SPI Port to LatticeSC sysCONFIG Port Timing table. |
| | | Pin Information | Updated Pin Information Summary with SC40 information. |
| | | | Updated LFSC25 Logic Signal Connections: FF1020 with SC40 information. |
| | | | Updated LFSC80 Logic Signal Connections: FC1152 with SC40 information. |
| August 2007 | 01.6 | General | Changed references of "HDC" to "HDC/SI". |
| | | | Changed references of "LDCN" to "LDCN/SCS". |
| | | | Changed references of "BUSYN/RCLK" to "BUSYN/RCLK/SCK". |
| | | | Changed references of "RDCFGN" to "TSALLN". |
| | | | Changed references of "TDO/RDDATA" to "TDO". |
| | | Architecture | Updated text in Ripple Mode section. |
| | | | Added information to Global Set/Reset. |
| | | | Added information for Spread Spectrum Clocking |
| | | | Modified information for PLL/DLL Cascading. DLL to PLL is now supported. |
| | | | Modified AIL Block text and figure. |
| | | | Modified Figure 2-20 DDR/Shift Register Block. |
| | | | Added Information to Hot Socketing. |
| | | | Added new information for I/O Architecture Rules. |
| | | | Added information to SERDES Power Supply Sequencing Requirements. |
| | | DC and Switching Characteristics | Added footnote to Hot Socketing Specifications table. |
| | | | Modified Initialization and Standby Supply Current table. |
| | | | Modified GSR Timing table. |
| | | | Modified sysCLOCK DLL Timing table to include $I_{DUTY.}$ |
| | | | Deleted Readback Timing information from sysCONFIG Port Timing table. |
| | | | Modified data in External Switching Characteristics table. |
| | | Pin Information | Added information to the Signal Descriptions table for HDC/SI, LDCN/SCS. |
| | | | Added footnote to Signal Descriptions table. |
| | | | Modified Description for signal BUSYN/RCLK/SCK. |
| | | | Modified data in Pin Information Summary and device-specific Pinout Information tables. |