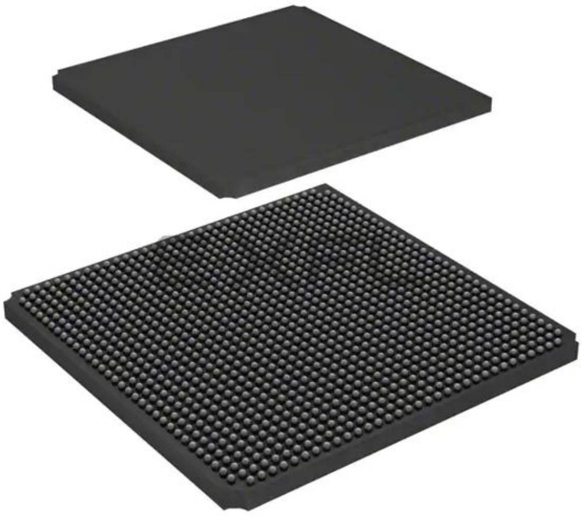

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 20000 |
| Number of Logic Elements/Cells | 80000 |
| Total RAM Bits | 5816320 |
| Number of I/O | 660 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BCBGA, FCBGA |
| Supplier Device Package | 1152-CFCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-6fc1152c |

*Table 1-1. LatticeSC Family Selection Guide[1]*

| Device | SC15 | SC25 | SC40 | SC80 | SC115 |
|---|---|---|---|---|---|
| LUT4s (K) | 15 | 25 | 40 | 80 | 115 |
| sysMEM Blocks (18Kb) | 56 | 104 | 216 | 308 | 424 |
| Embedded Memory (Mbits) | 1.03 | 1.92 | 3.98 | 5.68 | 7.8 |
| Max. Distributed Memory (Mbits) | 0.24 | 0.41 | 0.65 | 1.28 | 1.84 |
| Number of 3.8Gbps SERDES (Max.) | 8 | 16 | 16 | 32 | 32 |
| DLLs | 12 | 12 | 12 | 12 | 12 |
| Analog PLLs | 8 | 8 | 8 | 8 | 8 |
| MACO Blocks | 4 | 6 | 10 | 10 | 12 |
| **Package I/O/SERDES Combinations (1mm ball pitch)** | | | | | |
| 256-ball fpBGA (17 x 17mm) | 139/4 | | | | |
| 900-ball fpBGA (31 x 31mm) | 300/8 | 378/8 | | | |
| 1020-ball fcBGA (33 x 33mm)[2] | | 476/16 | 562/16 | | |
| 1152-ball fcBGA (35 x 35mm)[3] | | | 604/16 | 660/16 | 660/16 |
| 1704-ball fcBGA (42.5 x 42.5mm)[3] | | | | 904/32 | 942/32 |

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per PCN #02A-10.
3. Ceramic fcBGA converted to organic fcBGA per PCN #01A-10.

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

*Table 1-2. LatticeSCM Family*

| Device | SCM15 | SCM25 | SCM40 | SCM80 | SCM115 |
|---|---|---|---|---|---|
| flexiMAC Blocks<br>• 1GbE Mode<br>• 10GbE Mode<br>• PCI Express Mode | 1 | 2 | 2 | 2 | 4 |
| SPI4.2 Blocks | 1 | 2 | 2 | 2 | 2 |
| Memory Controller Blocks<br>• DDR/DDR2 DRAM Mode<br>• QDR II/II+ SRAM Mode<br>• RLDRAM I<br>• RLDRAM II CIO/SIO | 1 | 2 | 2 | 2 | 2 |
| Low-Speed CDR Blocks | 0 | 0 | 2 | 2 | 2 |
| PCI Express LTSSM (PHY) Blocks | 1 | 0 | 2 | 2 | 2 |

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

# Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

*Table 2-6. Input/Output/Tristate Gearing Resource Rules*

| PIO | Input/Output Logic | | | Tri-State/Bidi | |
|---|---|---|---|---|---|
| | x1 | x2 | x4 | x1 | x2/x4 |
| A | ? | ? | ? | ? | N/A |
| B | ? | No I/O Logic | No I/O Logic | ? | N/A |
| C | ? | ? | No I/O Logic | ? | N/A |
| D | ? | No I/O Logic | No I/O Logic | ? | N/A |

Note: Pin can still be used without I/O logic.

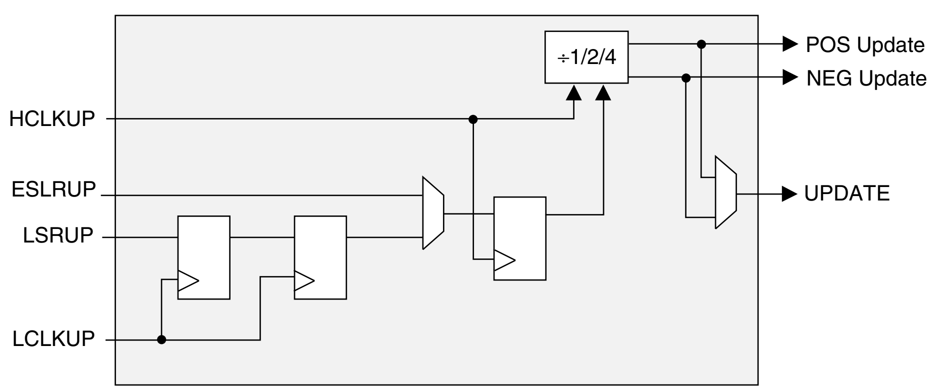
## Control Logic Block

The control logic block allows the modification of control signals selected by the routing before they are used in the PIO. It can optionally invert all signals passing through it except the Global Set/Reset. Global Set/Reset can be enabled or disabled. It can route either the edge clock or the clock to the high-speed clock nets. The clock provided to the PIO by routing is used as the slow-speed clocks. In addition this block contains delays that can be inserted in the clock nets to enable Lattice's unique cycle boosting capability.

## Update Block

The update block is used to generate the POS update and NEG update signals used by the DDR/Shift register blocks within the PIO. Note the update block is only required in shift modes. This is required in order to do the high speed to low speed handoff. One of these update signals is also selected and output from the PIC as the signal UPDATE. It consists of a shift chain that operates off either the high-speed input or output clock. The values of each register in the chain are set or reset depending on the desired mode of operation. The set/reset signal is generated from either the edge reset ELSR or the local reset LSR. These signals are optionally inverted by the Control Logic Block and provided to the update block as ELSRUP and LSRUP. The Lattice design tools automatically configure and connect the update block when one of the DDR or shift register primitives is used.

*Figure 2-25. Update Block*




# PURESPEED I/O Buffer

Each I/O is associated with a flexible buffer referred to as PURESPEED I/O buffer. These buffers are arranged around the periphery of the device in seven groups referred to as Banks. The PURESPEED I/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL. The availability of programmable on-chip termination for both input and output use, further enhances the utility of these buffers.

this allows for easy integration with the rest of the system. These capabilities make the LatticeSC ideal for many multiple power supply and hot-swap applications. The maximum current during hot socketing is 4mA. See Hot Socketing Specifications in Chapter 3 of this data sheet.

## Power-Up Requirements

To prevent high power supply and input pin currents, each VCC, VCC12, VCCAUX, VCCIO and VCCJ power supplies must have a monotonic ramp up time of 75 ms or less to reach its minimum operating voltage. Apart from VCC and VCC12, which have an additional requirement, and VCCIO and VCCAUX, which also have an additional requirement, the VCC, VCC12, VCCAUX, VCCIO and VCCJ power supplies can ramp up in any order, with no restriction on the time between them. However, the ramp time for each must be 75 ms or less. Configuration of the device will not proceed until the last power supply has reached its minimum operating voltage.

### Additional Requirement for VCC and VCC12:

VCC12 must always be higher than VCC. This condition must be maintained at ALL times, including during power-up and power-down. Note that for 1.2V only operation, it is advisable to source both of these supplies from the same power supply.

### Additional Requirement for VCCIO and VCCAUX:

If any VCCIOs are 1.2/1.5/1.8V, then VCCAUX MUST be applied before them. If any VCCIO is 1.2/1.5/1.8V and is powered up before VCCAUX, then when VCCAUX is powered up, it may drag VCCIO up with it as it crosses through the VCCIO value. (Note: If the VCCIO supply is capable of sinking current, as well as the more usual sourcing capability, this behavior is eliminated. However, the amount of current that the supply needs to sink is unknown and is likely to be in the hundreds of milliamps range).

## Power-Down Requirements

To prevent high power supply and input pin currents, power must be removed monotonically from either VCC or VCCAUX (and must reach the power-down trip point of 0.5V for VCC, 0.95V for VCCAUX) before power is removed monotonically from VCC12, any of the VCCIOs, or VCCJ. Note that VCC12 can be removed at the same time as VCC, but it cannot be removed earlier. In many applications, VCC and VCC12 will be sourced from the same power supply and so will be removed together. For systems where disturbance of the user pins is a don't care condition, the power supplies can be removed in any order as long as they power down monotonically within 200ms of each other.

Additionally, if any banks have VCCIO=3.3V nominal (potentially banks 1, 4, 5) then VCCIO for those banks must not be lower than VCCAUX during power-down. The normal variation in ramp-up times of power supplies and voltage regulators is not a concern here.

Note: The SERDES power supplies are NOT included in these requirements and have no specific sequencing requirements. However, when using the SERDES with VDDIB or VDDOB that is greater than 1.2V (1.5V nominal for example), the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in the ramp-up times of power supplies and voltage regulators is not a concern here.

## SERDES Power Supply Sequencing Requirements

When using the SERDES with 1.5V VDDIB or VDDOB supplies, the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and the 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in ramp-up times of power supples and voltage regulators is not a concern.

### Additional Requirement for SERDES Power Supply

All VCC12 pins need to be connected on all devices independent of functionality used on the device. This analog supply is used by both the RX and TX portions of the SERDES and is used to control the core SERDES logic regardless of the SERDES being used in the design. VDDIB and VDDOB are used as supplies for the terminations on the CML input and output buffers. If a particular channel is not used, these can be UNCONNECTED (floating).

## LVPECL

The LatticeSC devices support differential LVPECL standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

***Figure 3-3. Differential LVPECL***

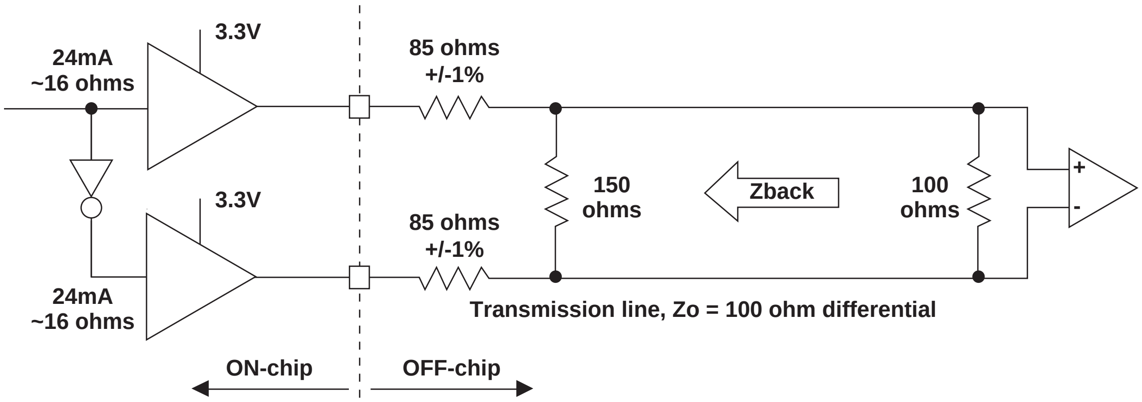



***Table 3-3. LVPECL DC Conditions[1]***

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 16 | ohm |
| $R_S$ | Driver series resistor | 85 | ohm |
| $R_P$ | Driver parallel resistor | 150 | ohm |
| $R_T$ | Receiver termination | 100 | ohm |
| $V_{OH}$ | Output high voltage | 2.03 | V |
| $V_{OL}$ | Output low voltage | 1.27 | V |
| $V_{OD}$ | Output differential voltage | 0.76 | V |
| $V_{CM}$ | Output common mode voltage | 1.65 | V |
| $Z_{BACK}$ | Back impedance | 86 | ohm |
| $I_{DC}$ | DC output current | 12.6 | mA |

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS, MLVDS and other differential interfaces please see details of additional technical documentation at the end of this data sheet.

# On-die Differential Common Mode Termination

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $C_{CMT}$ | Capacitance $V_{CMT}$ to GND | — | 40 | — | pF |

## LatticeSC/M Family Timing Adders (Continued)

**Over Recommended Operating Conditions at VCC = 1.2V +/- 5%**

| Buffer Type | Description | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| GTLPLUS15 | GTLPLUS15 | -0.013 | -0.017 | 0.012 | 0.004 | 0.037 | 0.024 | ns |
| GTL12 | GTL12 | -0.063 | -0.071 | -0.007 | -0.048 | 0.056 | -0.032 | ns |
| **Output Adjusters** | | | | | | | | |
| LVDS | LVDS | 0.708 | 0.854 | 0.856 | 1.021 | 1.005 | 1.189 | ns |
| RSDS | RSDS | 0.708 | 0.854 | 0.856 | 1.021 | 1.005 | 1.189 | ns |
| BLVDS25 | BLVDS | -0.129 | 0.05 | -0.136 | 0.069 | -0.136 | 0.083 | ns |
| MLVDS25 | MLVDS | -0.059 | 0.059 | -0.057 | 0.096 | -0.054 | 0.133 | ns |
| LVPECL33 | LVPECL | -0.334 | -0.181 | -0.325 | -1.389 | -0.315 | -2.598 | ns |
| HSTL18_I | HSTL_18 class I | 0.132 | 0.209 | 0.153 | 0.24 | 0.175 | 0.272 | ns |
| HSTL18_II | HSTL_18 class II | 0.24 | 0.176 | 0.268 | 0.255 | 0.298 | 0.333 | ns |
| HSTL18D_I | Differential HSTL 18 class I | 0.132 | 0.209 | 0.153 | 0.24 | 0.175 | 0.272 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.24 | 0.176 | 0.268 | 0.255 | 0.298 | 0.333 | ns |
| HSTL15_I | HSTL_15 class I | 0.096 | 0.172 | 0.112 | 0.198 | 0.129 | 0.224 | ns |
| HSTL15_II | HSTL_15 class II | 0.208 | 0.131 | 0.233 | 0.203 | 0.259 | 0.275 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.096 | 0.172 | 0.112 | 0.198 | 0.129 | 0.224 | ns |
| HSTL15D_II | Differential HSTL 15 class II | 0.208 | 0.131 | 0.233 | 0.203 | 0.259 | 0.275 | ns |
| SSTL33_I | SSTL_3 class I | 0.133 | 0.177 | 0.11 | 0.166 | 0.088 | 0.154 | ns |
| SSTL33_II | SSTL_3 class II | 0.173 | 0.247 | 0.164 | 0.253 | 0.156 | 0.258 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 0.133 | 0.177 | 0.11 | 0.166 | 0.088 | 0.154 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.173 | 0.247 | 0.164 | 0.253 | 0.156 | 0.258 | ns |
| SSTL25_I | SSTL_2 class I | 0.215 | 0.125 | 0.239 | 0.228 | 0.264 | 0.331 | ns |
| SSTL25_II | SSTL_2 class II | 0.277 | 0.181 | 0.311 | 0.284 | 0.345 | 0.387 | ns |
| SSTL25D_I | Differential SSTL_2 class I | 0.215 | 0.125 | 0.239 | 0.228 | 0.264 | 0.331 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.277 | 0.181 | 0.311 | 0.284 | 0.345 | 0.387 | ns |
| SSTL18_I | SSTL_2 class I | 0.16 | 0.081 | 0.179 | 0.173 | 0.199 | 0.265 | ns |
| SSTL18_II | SSTL_2 class II | 0.238 | 0.15 | 0.263 | 0.244 | 0.295 | 0.338 | ns |
| SSTL18D_I | Differential SSTL_2 class I | 0.16 | 0.081 | 0.179 | 0.173 | 0.199 | 0.265 | ns |
| SSTL18D_II | Differential SSTL_2 class II | 0.238 | 0.15 | 0.263 | 0.244 | 0.295 | 0.338 | ns |
| LVTTL33_8mA | LVTTL 8mA drive | -0.346 | -0.165 | -0.496 | -0.296 | -0.646 | -0.428 | ns |
| LVTTL33_16mA | LVTTL 16mA drive | -0.11 | -0.18 | -0.218 | -0.32 | -0.325 | -0.46 | ns |
| LVTTL33_24mA | LVTTL 24mA drive | -0.012 | -0.18 | -0.099 | -0.321 | -0.185 | -0.463 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8mA drive | -0.346 | -0.165 | -0.496 | -0.296 | -0.646 | -0.428 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16mA drive | -0.11 | -0.18 | -0.218 | -0.32 | -0.325 | -0.46 | ns |
| LVCMOS33_24mA | LVCMOS 3.3 24mA drive | -0.012 | -0.18 | -0.099 | -0.321 | -0.185 | -0.463 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4mA drive | -0.174 | 0.004 | -0.195 | 0.002 | -0.215 | 0 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8mA drive | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12mA drive | 0.094 | -0.025 | 0.107 | 0.096 | 0.12 | 0.216 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16mA drive | 0.145 | -0.054 | 0.162 | 0.063 | 0.181 | 0.179 | ns |
| LVCMOS25_OD | LVCMOS 2.5 open drain | 0.073 | -0.125 | 0.081 | -0.081 | 0.091 | -0.09 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4mA drive | -0.278 | -0.099 | -0.312 | -0.115 | -0.345 | -0.131 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8mA drive | -0.073 | -0.078 | -0.078 | -0.084 | -0.083 | -0.089 | ns |

# LatticeSC/M Internal Timing Parameters[1] (Continued)

**Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%**

| Parameter | Symbol | Description | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **EBR Timing** | | | | | | | | | |
| $t_{CO\_EBR}$ | CK_Q_DEL | Clock (Read) to output from Address or Data | — | 1.900 | — | 2.116 | — | 2.335 | ns |
| $t_{COO\_EBR}$ | CK_Q_DEL | Clock (Write) to output from EBR output Register | 0.390 | — | 0.444 | — | 0.498 | — | ns |
| $t_{SUDATA\_EBR}$ | D_CK_SET | Setup Data to EBR Memory (Write clk) | -0.173 | — | -0.192 | — | -0.210 | — | ns |
| $t_{HDATA\_EBR}$ | D_CK_HLD | Hold Data to EBR Memory (Write clk) | 0.276 | — | 0.305 | — | 0.335 | — | ns |
| $t_{SUADDR\_EBR}$ | A_CK_SET | Setup Address to EBR Memory (Write clk) | -0.165 | — | -0.182 | — | -0.200 | — | ns |
| $t_{HADDR\_EBR}$ | A_CK_HLD | Hold Address to EBR Memory (Write clk) | 0.269 | — | 0.298 | — | 0.327 | — | ns |
| $t_{SUWREN\_EBR}$ | CE_CK_SET | Setup Write/Read Enable to EBR Memory (Write/Read clk) | 0.225 | — | 0.226 | — | 0.226 | — | ns |
| $t_{HWREN\_EBR}$ | CE_CK_HLD | Hold Write/Read Enable to EBR Memory (write/read clk) | 0.073 | — | 0.095 | — | 0.116 | — | ns |
| $t_{SUCE\_EBR}$ | CS_CK_SET | Clock Enable Setup Time to EBR Output Register (Read clk) | 0.261 | — | 0.269 | — | 0.276 | — | ns |
| $t_{HCE\_EBR}$ | CS_CK_HLD | Clock Enable Hold Time to EBR Output Register (Read clk) | 0.023 | — | 0.039 | — | 0.055 | — | ns |
| $t_{RSTO\_EBR}$ | RESET_Q_DEL | Reset To Output Delay Time from EBR Output Register (asynchronous) | — | 0.589 | — | 0.673 | — | 0.757 | ns |
| **Cycle Boosting Timing** | | | | | | | | | |
| $t_{DEL1}$ | DEL1 | Cycle boosting delay 1 applies to PIO, PFU, EBR | — | 0.480 | — | 0.524 | — | 0.570 | ns |
| $t_{DEL2}$ | DEL2 | Cycle boosting delay 2 applies to PIO, PFU, EBR | — | 0.922 | — | 1.005 | — | 1.090 | ns |
| $t_{DEL3}$ | DEL3 | Cycle boosting delay 3 applies to PIO, PFU, EBR | — | 1.366 | — | 1.488 | — | 1.612 | ns |

1. Complete timing parameters for a user design will be incorporated when running ispLEVER. This is a sampling of the key timing parameters.

# LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

| Ball Number | LFSC/M15 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| N12 | PB39C | 4 | |
| T15 | PB40A | 4 | PCLKT4_3 |
| R16 | PB40B | 4 | PCLKC4_3 |
| L12 | PB43A | 4 | |
| M12 | PB43B | 4 | |
| P16 | PB44A | 4 | |
| N16 | PB44B | 4 | |
| R14 | PB47C | 4 | VREF1_4 |
| P15 | PB48A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D |
| M13 | PB48B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D |
| N13 | PB49A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B |
| P14 | PB49B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B |
| M16 | PR45B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E |
| L16 | PR45A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E |
| M14 | PR43B | 3 | |
| M15 | PR43A | 3 | |
| K16 | PR41D | 3 | VREF2_3 |
| J16 | PR37B | 3 | |
| H16 | PR37A | 3 | |
| L13 | PR35D | 3 | DIFFR_3 |
| L14 | PR35B | 3 | |
| L15 | PR35A | 3 | |
| K12 | PR31C | 3 | VREF1_3 |
| J13 | PR28D | 3 | PCLKC3_2 |
| K13 | PR28C | 3 | PCLKT3_2 |
| H15 | PR28B | 3 | |
| F16 | PR28A | 3 | |
| J11 | PR26D | 3 | PCLKC3_1 |
| J12 | PR26C | 3 | PCLKT3_1 |
| J15 | PR26B | 3 | PCLKC3_0 |
| J14 | PR26A | 3 | PCLKT3_0 |
| E16 | PR24D | 2 | PCLKC2_2 |
| D16 | PR24C | 2 | PCLKT2_2 |
| H11 | PR24B | 2 | PCLKC2_0 |
| H12 | PR24A | 2 | PCLKT2_0 |
| H13 | PR23B | 2 | PCLKC2_1 |
| H14 | PR23A | 2 | PCLKT2_1 |
| G12 | PR22D | 2 | DIFFR_2 |
| G13 | PR22C | 2 | VREF1_2 |
| F8 | PR22B | 2 | |
| F9 | PR22A | 2 | |
| G16 | PR18D | 2 | VREF2_2 |
| F15 | PR17B | 2 | URC_DLLC_IN_C/URC_DLLC_FB_D |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AF4 | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| AE5 | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| AG3 | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C |
| AH2 | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C |
| AD6 | PB4C | 5 | | PB4C | 5 | |
| AJ2 | PB5A | 5 | | PB5A | 5 | |
| AK2 | PB5B | 5 | | PB5B | 5 | |
| AD7 | PB5C | 5 | | PB5C | 5 | |
| AD8 | PB5D | 5 | VREF1_5 | PB5D | 5 | VREF1_5 |
| AH3 | PB7A | 5 | | PB11A | 5 | |
| AJ3 | PB7B | 5 | | PB11B | 5 | |
| AF9 | PB7C | 5 | | PB11C | 5 | |
| AE10 | PB7D | 5 | | PB11D | 5 | |
| AK3 | PB8A | 5 | | PB12A | 5 | |
| AJ4 | PB8B | 5 | | PB12B | 5 | |
| AE11 | PB9A | 5 | | PB13A | 5 | |
| AF10 | PB9B | 5 | | PB13B | 5 | |
| AK4 | PB11A | 5 | | PB16A | 5 | |
| AK5 | PB11B | 5 | | PB16B | 5 | |
| AH10 | PB12A | 5 | PCLKT5_3 | PB20A | 5 | PCLKT5_3 |
| AH11 | PB12B | 5 | PCLKC5_3 | PB20B | 5 | PCLKC5_3 |
| AF13 | PB12C | 5 | PCLKT5_4 | PB20C | 5 | PCLKT5_4 |
| AE14 | PB12D | 5 | PCLKC5_4 | PB20D | 5 | PCLKC5_4 |
| AK6 | PB13A | 5 | PCLKT5_5 | PB21A | 5 | PCLKT5_5 |
| AK7 | PB13B | 5 | PCLKC5_5 | PB21B | 5 | PCLKC5_5 |
| AF14 | PB13C | 5 | | PB21C | 5 | |
| AJ11 | PB15A | 5 | PCLKT5_0 | PB23A | 5 | PCLKT5_0 |
| AJ12 | PB15B | 5 | PCLKC5_0 | PB23B | 5 | PCLKC5_0 |
| AH13 | PB15D | 5 | VREF2_5 | PB23D | 5 | VREF2_5 |
| AK8 | PB16A | 5 | PCLKT5_1 | PB24A | 5 | PCLKT5_1 |
| AK9 | PB16B | 5 | PCLKC5_1 | PB24B | 5 | PCLKC5_1 |
| AH14 | PB17A | 5 | PCLKT5_2 | PB25A | 5 | PCLKT5_2 |
| AG14 | PB17B | 5 | PCLKC5_2 | PB25B | 5 | PCLKC5_2 |
| AK10 | PB19A | 5 | | PB28A | 5 | |
| AK11 | PB19B | 5 | | PB28B | 5 | |
| AH15 | PB20A | 5 | | PB29A | 5 | |
| AG15 | PB20B | 5 | | PB29B | 5 | |
| AH12 | PB21A | 5 | | PB31A | 5 | |
| AJ13 | PB21B | 5 | | PB31B | 5 | |
| AD15 | PB21C | 5 | | PB31C | 5 | |
| AE15 | PB21D | 5 | | PB31D | 5 | |
| AK12 | PB23A | 5 | | PB32A | 5 | |
| AK13 | PB23B | 5 | | PB32B | 5 | |
| AJ14 | PB24A | 5 | | PB33A | 5 | |
| AJ15 | PB24B | 5 | | PB33B | 5 | |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| G1 | NC | - | | PL20B | 7 | |
| M4 | NC | - | | NC | - | |
| J3 | NC | - | | NC | - | |
| P5 | NC | - | | NC | - | |
| W5 | NC | - | | PL48C | 6 | |
| T6 | NC | - | | PL35C | 6 | |
| U3 | NC | - | | PL36A | 6 | |
| V3 | NC | - | | PL36B | 6 | |
| T5 | NC | - | | PL39A | 6 | |
| T4 | NC | - | | PL39B | 6 | |
| V5 | NC | - | | PL43C | 6 | |
| U6 | NC | - | | PL42C | 6 | |
| U4 | NC | - | | PL40A | 6 | |
| U5 | NC | - | | PL40B | 6 | |
| V4 | NC | - | | PL43D | 6 | |
| Y2 | NC | - | | PL47A | 6 | |
| AA2 | NC | - | | PL47B | 6 | |
| W3 | NC | - | | PL47D | 6 | |
| Y3 | NC | - | | PL47C | 6 | |
| AB3 | NC | - | | NC | - | |
| AC4 | NC | - | | PL53A | 6 | |
| AD4 | NC | - | | PL53B | 6 | |
| AE3 | NC | - | | PL56A | 6 | |
| AF3 | NC | - | | PL56B | 6 | |
| AF7 | NC | - | | PB7A | 5 | |
| AF6 | NC | - | | PB7B | 5 | |
| AH4 | NC | - | | PB8A | 5 | |
| AG5 | NC | - | | PB8B | 5 | |
| AF8 | NC | - | | PB9A | 5 | |
| AG8 | NC | - | | PB9B | 5 | |
| AG7 | NC | - | | NC | - | |
| AG10 | NC | - | | NC | - | |
| AF12 | NC | - | | NC | - | |
| AH7 | NC | - | | PB15A | 5 | |
| AE13 | NC | - | | PB15D | 5 | |
| AG13 | NC | - | | PB23C | 5 | |
| AH8 | NC | - | | PB15B | 5 | |
| AJ5 | NC | - | | PB17A | 5 | |
| AJ6 | NC | - | | PB17B | 5 | |
| AF15 | NC | - | | PB21D | 5 | |
| AJ7 | NC | - | | PB19A | 5 | |
| AJ8 | NC | - | | PB19B | 5 | |
| AE12 | NC | - | | PB15C | 5 | |
| AF16 | NC | - | | PB38D | 4 | |
| AF19 | NC | - | | PB49D | 4 | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| Ball Number | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| V25 | PL44C | 6 | | PL56C | 6 | |
| W25 | PL44D | 6 | | PL56D | 6 | |
| U34 | PL45A | 6 | | PL57A | 6 | |
| V34 | PL45B | 6 | | PL57B | 6 | |
| V26 | PL45C | 6 | | PL57C | 6 | |
| W26 | PL45D | 6 | | PL57D | 6 | |
| V33 | PL47A | 6 | | PL60A | 6 | |
| W33 | PL47B | 6 | | PL60B | 6 | |
| V24 | PL47C | 6 | | PL60C | 6 | |
| W24 | PL47D | 6 | | PL60D | 6 | |
| W31 | PL48A | 6 | | PL63A | 6 | |
| Y31 | PL48B | 6 | | PL63B | 6 | |
| Y29 | PL48C | 6 | | PL63C | 6 | |
| AA29 | PL48D | 6 | | PL63D | 6 | |
| Y33 | PL49A | 6 | | PL65A | 6 | |
| AA33 | PL49B | 6 | | PL65B | 6 | |
| Y28 | PL49C | 6 | | PL65C | 6 | |
| AA28 | PL49D | 6 | | PL65D | 6 | |
| AB32 | PL51A | 6 | | PL76A | 6 | |
| AC32 | PL51B | 6 | | PL76B | 6 | |
| AA26 | PL51C | 6 | | PL76C | 6 | |
| AA27 | PL51D | 6 | DIFFR_6 | PL76D | 6 | DIFFR_6 |
| AB31 | PL52A | 6 | | PL77A | 6 | |
| AC31 | PL52B | 6 | | PL77B | 6 | |
| Y24 | PL52C | 6 | | PL77C | 6 | |
| AA24 | PL52D | 6 | | PL77D | 6 | |
| AE34 | PL53A | 6 | | PL78A | 6 | |
| AF34 | PL53B | 6 | | PL78B | 6 | |
| AB30 | PL53C | 6 | | PL78C | 6 | |
| AC30 | PL53D | 6 | | PL78D | 6 | |
| AD33 | PL56A | 6 | | PL80A | 6 | |
| AE33 | PL56B | 6 | | PL80B | 6 | |
| AD30 | PL56C | 6 | | PL80C | 6 | |
| AE30 | PL56D | 6 | | PL80D | 6 | |
| AE32 | PL57A | 6 | | PL81A | 6 | |
| AF32 | PL57B | 6 | | PL81B | 6 | |
| AA25 | PL57C | 6 | | PL81C | 6 | |
| AB25 | PL57D | 6 | | PL81D | 6 | |
| AJ34 | PL58A | 6 | | PL82A | 6 | |
| AK34 | PL58B | 6 | | PL82B | 6 | |
| AB27 | PL58C | 6 | | PL82C | 6 | |
| AC27 | PL58D | 6 | | PL82D | 6 | |
| AF33 | PL60A | 6 | | PL84A | 6 | |
| AG33 | PL60B | 6 | | PL84B | 6 | |
| AC29 | PL60C | 6 | | PL84C | 6 | |

## LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| Ball Number | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| L1 | PR31A | 2 | | PR43A | 2 | |
| T10 | PR30D | 2 | | PR42D | 2 | |
| U10 | PR30C | 2 | | PR42C | 2 | |
| N2 | PR30B | 2 | | PR42B | 2 | |
| M2 | PR30A | 2 | | PR42A | 2 | |
| R11 | PR29D | 2 | | PR37D | 2 | |
| P11 | PR29C | 2 | | PR37C | 2 | |
| N4 | PR29B | 2 | | PR37B | 2 | |
| M4 | PR29A | 2 | | PR37A | 2 | |
| N5 | PR27D | 2 | | PR35D | 2 | |
| M5 | PR27C | 2 | | PR35C | 2 | |
| L2 | PR27B | 2 | | PR35B | 2 | |
| K2 | PR27A | 2 | | PR35A | 2 | |
| P8 | PR26D | 2 | | PR33D | 2 | |
| N8 | PR26C | 2 | | PR33C | 2 | |
| J2 | PR26B | 2 | | PR33B | 2 | |
| H2 | PR26A | 2 | | PR33A | 2 | |
| M6 | PR25D | 2 | | PR31D | 2 | |
| L6 | PR25C | 2 | | PR31C | 2 | |
| K3 | PR25B | 2 | | PR31B | 2 | |
| J3 | PR25A | 2 | | PR31A | 2 | |
| M8 | PR23D | 2 | DIFFR_2 | PR29D | 2 | DIFFR_2 |
| L8 | PR23C | 2 | VREF1_2 | PR29C | 2 | VREF1_2 |
| K4 | PR23B | 2 | | PR29B | 2 | |
| J4 | PR23A | 2 | | PR29A | 2 | |
| M7 | PR22D | 2 | | PR21D | 2 | |
| L7 | PR22C | 2 | | PR21C | 2 | |
| J5 | PR22B | 2 | | PR21B | 2 | |
| H5 | PR22A | 2 | | PR21A | 2 | |
| N9 | PR21D | 2 | | PR20D | 2 | |
| P9 | PR21C | 2 | | PR20C | 2 | |
| G3 | PR21B | 2 | | PR20B | 2 | |
| F3 | PR21A | 2 | | PR20A | 2 | |
| J6 | PR18D | 2 | VREF2_2 | PR18D | 2 | VREF2_2 |
| H6 | PR18C | 2 | | PR18C | 2 | |
| E2 | PR18B | 2 | URC_DLLC_IN_D/URC_DLLC_FB_C | PR18B | 2 | URC_DLLC_IN_D/URC_DLLC_FB_C |
| D2 | PR18A | 2 | URC_DLLT_IN_D/URC_DLLT_FB_C | PR18A | 2 | URC_DLLT_IN_D/URC_DLLT_FB_C |
| P10 | PR17D | 2 | URC_PLLC_IN_B/URC_PLLC_FB_A | PR17D | 2 | URC_PLLC_IN_B/URC_PLLC_FB_A |
| N10 | PR17C | 2 | URC_PLLT_IN_B/URC_PLLT_FB_A | PR17C | 2 | URC_PLLT_IN_B/URC_PLLT_FB_A |
| G4 | PR17B | 2 | URC_DLLC_IN_C/URC_DLLC_FB_D | PR17B | 2 | URC_DLLC_IN_C/URC_DLLC_FB_D |
| F4 | PR17A | 2 | URC_DLLT_IN_C/URC_DLLT_FB_D | PR17A | 2 | URC_DLLT_IN_C/URC_DLLT_FB_D |
| J7 | PR16D | 2 | | PR16D | 2 | |
| H7 | PR16C | 2 | | PR16C | 2 | |
| G5 | PR16B | 2 | URC_PLLC_IN_A/URC_PLLC_FB_B | PR16B | 2 | URC_PLLC_IN_A/URC_PLLC_FB_B |
| F5 | PR16A | 2 | URC_PLLT_IN_A/URC_PLLT_FB_B | PR16A | 2 | URC_PLLT_IN_A/URC_PLLT_FB_B |

# LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| | LFSC/M115 | | |
|---|---|---|---|
| Ball Number | Ball Function | VCCIO Bank | Dual Function |
| AN15 | PB89A | 4 | PCLKT4_2 |
| AN14 | PB89B | 4 | PCLKC4_2 |
| AE16 | PB89C | 4 | PCLKT4_7 |
| AD16 | PB89D | 4 | PCLKC4_7 |
| AK15 | PB90A | 4 | PCLKT4_1 |
| AK14 | PB90B | 4 | PCLKC4_1 |
| AG15 | PB90C | 4 | PCLKT4_6 |
| AG14 | PB90D | 4 | PCLKC4_6 |
| AM13 | PB91A | 4 | PCLKT4_0 |
| AM12 | PB91B | 4 | PCLKC4_0 |
| AJ12 | PB91C | 4 | VREF2_4 |
| AJ11 | PB91D | 4 | |
| AL13 | PB93A | 4 | PCLKT4_5 |
| AL12 | PB93B | 4 | PCLKC4_5 |
| AH12 | PB93C | 4 | |
| AH11 | PB93D | 4 | |
| AN13 | PB94A | 4 | PCLKT4_3 |
| AN12 | PB94B | 4 | PCLKC4_3 |
| AD14 | PB94C | 4 | PCLKT4_4 |
| AD15 | PB94D | 4 | PCLKC4_4 |
| AP13 | PB87A | 4 | |
| AP12 | PB87B | 4 | |
| AK13 | PB87C | 4 | |
| AK12 | PB87D | 4 | |
| AP11 | PB97A | 4 | |
| AP10 | PB97B | 4 | |
| AN11 | PB113A | 4 | |
| AN10 | PB113B | 4 | |
| AF14 | PB113C | 4 | |
| AF13 | PB113D | 4 | |
| AM10 | PB115A | 4 | |
| AM9 | PB115B | 4 | |
| AE14 | PB115C | 4 | |
| AE13 | PB115D | 4 | |
| AP9 | PB118A | 4 | |
| AP8 | PB118B | 4 | |
| AK11 | PB118C | 4 | |
| AK10 | PB118D | 4 | |
| AL10 | PB121A | 4 | |
| AL9 | PB121B | 4 | |
| AF12 | PB121C | 4 | |
| AF11 | PB121D | 4 | |
| AN9 | PB123A | 4 | |

# LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| F25 | B_HDINN0_L | - | PCS 361 CH 0 IN N |
| E25 | B_HDINP0_L | - | PCS 361 CH 0 IN P |
| D28 | B_VDDIB0_L | - | |
| G25 | VCC12 | - | |
| D29 | A_VDDIB3_L | - | |
| C25 | VCC12 | - | |
| A25 | A_HDINP3_L | - | PCS 360 CH 3 IN P |
| B25 | A_HDINN3_L | - | PCS 360 CH 3 IN N |
| A26 | A_HDOUTP3_L | - | PCS 360 CH 3 OUT P |
| E27 | VCC12 | - | |
| B26 | A_HDOUTN3_L | - | PCS 360 CH 3 OUT N |
| F26 | A_VDDOB3_L | - | |
| B27 | A_HDOUTN2_L | - | PCS 360 CH 2 OUT N |
| F27 | A_VDDOB2_L | - | |
| A27 | A_HDOUTP2_L | - | PCS 360 CH 2 OUT P |
| E28 | VCC12 | - | |
| B28 | A_HDINN2_L | - | PCS 360 CH 2 IN N |
| A28 | A_HDINP2_L | - | PCS 360 CH 2 IN P |
| D30 | A_VDDIB2_L | - | |
| C28 | VCC12 | - | |
| D31 | A_VDDIB1_L | - | |
| C29 | VCC12 | - | |
| A29 | A_HDINP1_L | - | PCS 360 CH 1 IN P |
| B29 | A_HDINN1_L | - | PCS 360 CH 1 IN N |
| A30 | A_HDOUTP1_L | - | PCS 360 CH 1 OUT P |
| E29 | VCC12 | - | |
| B30 | A_HDOUTN1_L | - | PCS 360 CH 1 OUT N |
| F28 | A_VDDOB1_L | - | |
| B31 | A_HDOUTN0_L | - | PCS 360 CH 0 OUT N |
| F29 | A_VDDOB0_L | - | |
| A31 | A_HDOUTP0_L | - | PCS 360 CH 0 OUT P |
| E30 | VCC12 | - | |
| B32 | A_HDINN0_L | - | PCS 360 CH 0 IN N |
| A32 | A_HDINP0_L | - | PCS 360 CH 0 IN P |
| D32 | A_VDDIB0_L | - | |
| C32 | VCC12 | - | |
| E34 | PL30A | 7 | |
| F34 | PL30B | 7 | |
| F33 | PL34A | 7 | |
| G33 | PL34B | 7 | |
| K30 | PL38A | 7 | |
| L30 | PL38B | 7 | |
| G34 | PL40A | 7 | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| H34 | PL40B | 7 | |
| M32 | PL53A | 7 | |
| N32 | PL53B | 7 | |
| P28 | PL53C | 7 | |
| R28 | PL53D | 7 | |
| J34 | PL55A | 7 | |
| K34 | PL55B | 7 | |
| P30 | PL55C | 7 | |
| R30 | PL55D | 7 | |
| W34 | PL73A | 6 | |
| Y34 | PL73B | 6 | |
| W32 | PL75A | 6 | |
| Y32 | PL75B | 6 | |
| AA34 | PL78A | 6 | |
| AB34 | PL78B | 6 | |
| AC34 | PL81A | 6 | |
| AD34 | PL81B | 6 | |
| Y30 | PL82A | 6 | |
| AA30 | PL82B | 6 | |
| AB33 | PL83A | 6 | |
| AC33 | PL83B | 6 | |
| AC2 | PR83B | 3 | |
| AB2 | PR83A | 3 | |
| AA5 | PR82B | 3 | |
| Y5 | PR82A | 3 | |
| AD1 | PR81B | 3 | |
| AC1 | PR81A | 3 | |
| AB1 | PR78B | 3 | |
| AA1 | PR78A | 3 | |
| Y3 | PR75B | 3 | |
| W3 | PR75A | 3 | |
| Y1 | PR73B | 3 | |
| W1 | PR73A | 3 | |
| R5 | PR55D | 2 | |
| P5 | PR55C | 2 | |
| K1 | PR55B | 2 | |
| J1 | PR55A | 2 | |
| R7 | PR53D | 2 | |
| P7 | PR53C | 2 | |
| N3 | PR53B | 2 | |
| M3 | PR53A | 2 | |
| H1 | PR40B | 2 | |
| G1 | PR40A | 2 | |

# LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| | LFSC/M115 | | |
|---|---|---|---|
| Ball Number | Ball Function | VCCIO Bank | Dual Function |
| AL5 | GND | - | |
| AM14 | GND | - | |
| AM18 | GND | - | |
| AM24 | GND | - | |
| AM30 | GND | - | |
| AM8 | GND | - | |
| AN1 | GND | - | |
| AN34 | GND | - | |
| AP2 | GND | - | |
| AP33 | GND | - | |
| B1 | GND | - | |
| B34 | GND | - | |
| C11 | GND | - | |
| C12 | GND | - | |
| C13 | GND | - | |
| C14 | GND | - | |
| C17 | GND | - | |
| C21 | GND | - | |
| C22 | GND | - | |
| C23 | GND | - | |
| C24 | GND | - | |
| C26 | GND | - | |
| C27 | GND | - | |
| C30 | GND | - | |
| C31 | GND | - | |
| C4 | GND | - | |
| C5 | GND | - | |
| C8 | GND | - | |
| C9 | GND | - | |
| D18 | GND | - | |
| E32 | GND | - | |
| E4 | GND | - | |
| F19 | GND | - | |
| G16 | GND | - | |
| G29 | GND | - | |
| G7 | GND | - | |
| H3 | GND | - | |
| H31 | GND | - | |
| J10 | GND | - | |
| J15 | GND | - | |
| J26 | GND | - | |
| K20 | GND | - | |
| K23 | GND | - | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| W7 | GND | - | |
| AA14 | VCC | - | |
| AA16 | VCC | - | |
| AA17 | VCC | - | |
| AA18 | VCC | - | |
| AA19 | VCC | - | |
| AA21 | VCC | - | |
| AB13 | VCC | - | |
| AB22 | VCC | - | |
| N13 | VCC | - | |
| N22 | VCC | - | |
| P14 | VCC | - | |
| P16 | VCC | - | |
| P17 | VCC | - | |
| P18 | VCC | - | |
| P19 | VCC | - | |
| P21 | VCC | - | |
| R15 | VCC | - | |
| R17 | VCC | - | |
| R18 | VCC | - | |
| R20 | VCC | - | |
| T14 | VCC | - | |
| T16 | VCC | - | |
| T19 | VCC | - | |
| T21 | VCC | - | |
| U14 | VCC | - | |
| U15 | VCC | - | |
| U17 | VCC | - | |
| U18 | VCC | - | |
| U20 | VCC | - | |
| U21 | VCC | - | |
| V14 | VCC | - | |
| V15 | VCC | - | |
| V17 | VCC | - | |
| V18 | VCC | - | |
| V20 | VCC | - | |
| V21 | VCC | - | |
| W14 | VCC | - | |
| W16 | VCC | - | |
| W19 | VCC | - | |
| W21 | VCC | - | |
| Y15 | VCC | - | |
| Y17 | VCC | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| W33 | PL42C | 7 | | PL56C | 7 | |
| Y33 | PL42D | 7 | | PL56D | 7 | |
| W37 | PL43A | 7 | | PL57A | 7 | |
| Y37 | PL43B | 7 | | PL57B | 7 | |
| Y32 | PL43C | 7 | | PL57C | 7 | |
| AA32 | PL43D | 7 | | PL57D | 7 | |
| U38 | PL46A | 7 | | PL60A | 7 | |
| V38 | PL46B | 7 | | PL60B | 7 | |
| W34 | PL46C | 7 | | PL60C | 7 | |
| Y34 | PL46D | 7 | | PL60D | 7 | |
| T40 | PL47A | 7 | PCLKT7_1 | PL61A | 7 | PCLKT7_1 |
| U40 | PL47B | 7 | PCLKC7_1 | PL61B | 7 | PCLKC7_1 |
| AA33 | PL47C | 7 | PCLKT7_3 | PL61C | 7 | PCLKT7_3 |
| AB33 | PL47D | 7 | PCLKC7_3 | PL61D | 7 | PCLKC7_3 |
| R42 | PL48A | 7 | PCLKT7_0 | PL62A | 7 | PCLKT7_0 |
| T42 | PL48B | 7 | PCLKC7_0 | PL62B | 7 | PCLKC7_0 |
| AA34 | PL48C | 7 | PCLKT7_2 | PL62C | 7 | PCLKT7_2 |
| AB34 | PL48D | 7 | PCLKC7_2 | PL62D | 7 | PCLKC7_2 |
| U41 | PL50A | 6 | PCLKT6_0 | PL64A | 6 | PCLKT6_0 |
| V41 | PL50B | 6 | PCLKC6_0 | PL64B | 6 | PCLKC6_0 |
| V36 | PL50C | 6 | PCLKT6_1 | PL64C | 6 | PCLKT6_1 |
| W36 | PL50D | 6 | PCLKC6_1 | PL64D | 6 | PCLKC6_1 |
| U42 | PL51A | 6 | | PL65A | 6 | |
| V42 | PL51B | 6 | | PL65B | 6 | |
| AB31 | PL51C | 6 | PCLKT6_3 | PL65C | 6 | PCLKT6_3 |
| AC31 | PL51D | 6 | PCLKC6_3 | PL65D | 6 | PCLKC6_3 |
| W38 | PL52A | 6 | | PL66A | 6 | |
| Y38 | PL52B | 6 | | PL66B | 6 | |
| AA35 | PL52C | 6 | PCLKT6_2 | PL66C | 6 | PCLKT6_2 |
| AB35 | PL52D | 6 | PCLKC6_2 | PL66D | 6 | PCLKC6_2 |
| W39 | PL55A | 6 | | PL69A | 6 | |
| Y39 | PL55B | 6 | | PL69B | 6 | |
| AB32 | PL55C | 6 | VREF1_6 | PL69C | 6 | VREF1_6 |
| AC32 | PL55D | 6 | | PL69D | 6 | |
| W40 | PL56A | 6 | | PL70A | 6 | |
| Y40 | PL56B | 6 | | PL70B | 6 | |
| AA36 | PL56C | 6 | | PL70C | 6 | |
| AB36 | PL56D | 6 | | PL70D | 6 | |
| W41 | PL57A | 6 | | PL71A | 6 | |
| Y41 | PL57B | 6 | | PL71B | 6 | |
| AA37 | PL57C | 6 | | PL71C | 6 | |
| AB37 | PL57D | 6 | | PL71D | 6 | |
| W42 | PL59A | 6 | | PL73A | 6 | |
| Y42 | PL59B | 6 | | PL73B | 6 | |
| AC33 | PL59C | 6 | | PL73C | 6 | |

# LatticeSC/M Family Data Sheet
# Ordering Information

**January 2010** | **Data Sheet DS1004**

## Part Number Description

LF XXX XXX XX E PX – X XXXXXX X

**LF = Lattice FPGA**

**Device Family**
- LatticeSC FPGA
- LatticeSCM FPGA

**SERDES Speed**
- 3GA = 3.8G

**Logic Capacity**
- 15K LUTs
- 25K LUTs
- 40K LUTs
- 80K LUTs
- 115K LUTs

**Supply Voltage**
- E = 1.2V

**Grade**
- C = Commercial
- I = Industrial

**Package**[1]
- F256 = 256-ball fpBGA
- F900 = 900-ball fpBGA
- FF1020 = 1020-ball Organic fcBGA[2]
- FFA1020 = 1020-ball Organic fcBGA Revision 2
- FC1152 = 1152-ball Ceramic fcBGA[3]
- FF1152 = 1152-ball Organic fcBGA
- FC1704 = 1704-ball Ceramic fcBGA[3]
- FF1704 = 1704-ball Organic fcBGA

- FN256 = 256-ball Lead-Free fpBGA
- FN900 = 900-ball Lead-Free fpBGA
- FFN1020 = 1020-ball Lead-Free Organic fcBGA[2]
- FFAN1020 = 1020-ball Lead-Free Organic fcBGA Revision 2
- FCN1152 = 1152-ball Lead-Free Ceramic fcBGA[3]
- FFN1152 = 1152-ball Lead-Free Organic fcBGA
- FCN1704 = 1704-ball Lead-Free Ceramic fcBGA[3]
- FFN1704 = 1704-ball Lead-Free Organic fcBGA

**Speed Grade**
- -5 (Slowest)
- -6
- -7 (Fastest)[4]

**Predefined Function (LatticeSCM Only)**
- P1 = Initial MACO Option

1. fpBGA = 1.0 mm pitch BGA, fcBGA = 1.0 mm flip-chip BGA (organic and ceramic).
2. Converted to organic fcBGA per PCN #02A-10.
3. Converted to organic fcBGA per PCN #01A-10.
4. Not available in the LatticeSC115 and LatticeSCM115 devices.

## Ordering Information

Depending on the speed and temperature grade, the device can either be dual marked or single marked. The commercial grade is one speed grade faster than the associated dual marked industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

Lattice SC
LFSC3GA25E
6F900C-5I
XXXXXXXX

or

Lattice SC
LFSC3GA25E
7F900C
XXXXXXXX

| Temperature Grade | Speed Grade | Single or Dual Mark? |
|---|---|---|
| Commercial | -7 | Either OK |
| | -6 | Dual Only |
| | -5 | Single Only |
| Industrial | -6 | Either OK |
| | -5 | Dual Only |

**Industrial, Cont.**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA40EP1-6FF1020I[1] | -6 | Organic fcBGA | 1020 | IND | 40.4 |
| LFSCM3GA40EP1-5FF1020I[1] | -5 | Organic fcBGA | 1020 | IND | 40.4 |
| LFSCM3GA40EP1-6FFA1020I | -6 | Organic fcBGA Revision 2 | 1020 | IND | 40.4 |
| LFSCM3GA40EP1-5FFA1020I | -5 | Organic fcBGA Revision 2 | 1020 | IND | 40.4 |
| LFSCM3GA40EP1-6FC1152I[2] | -6 | Ceramic fcBGA | 1152 | IND | 40.4 |
| LFSCM3GA40EP1-5FC1152I[2] | -5 | Ceramic fcBGA | 1152 | IND | 40.4 |
| LFSCM3GA40EP1-6FF1152I | -6 | Organic fcBGA | 1152 | IND | 40.4 |
| LFSCM3GA40EP1-5FF1152I | -5 | Organic fcBGA | 1152 | IND | 40.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA80E-6FC1152I[1] | -6 | Ceramic fcBGA | 1152 | IND | 80.1 |
| LFSC3GA80E-5FC1152I[1] | -5 | Ceramic fcBGA | 1152 | IND | 80.1 |
| LFSC3GA80E-6FF1152I | -6 | Organic fcBGA | 1152 | IND | 80.1 |
| LFSC3GA80E-5FF1152I | -5 | Organic fcBGA | 1152 | IND | 80.1 |
| LFSC3GA80E-6FC1704I[1] | -6 | Ceramic fcBGA | 1704 | IND | 80.1 |
| LFSC3GA80E-5FC1704I[1] | -5 | Ceramic fcBGA | 1704 | IND | 80.1 |
| LFSC3GA80E-6FF1704I | -6 | Organic fcBGA | 1704 | IND | 80.1 |
| LFSC3GA80E-5FF1704I | -5 | Organic fcBGA | 1704 | IND | 80.1 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA80EP1-6FC1152I[1] | -6 | Ceramic fcBGA | 1152 | IND | 80.1 |
| LFSCM3GA80EP1-5FC1152I[1] | -5 | Ceramic fcBGA | 1152 | IND | 80.1 |
| LFSCM3GA80EP1-6FF1152I | -6 | Organic fcBGA | 1152 | IND | 80.1 |
| LFSCM3GA80EP1-5FF1152I | -5 | Organic fcBGA | 1152 | IND | 80.1 |
| LFSCM3GA80EP1-6FC1704I[1] | -6 | Ceramic fcBGA | 1704 | IND | 80.1 |
| LFSCM3GA80EP1-5FC1704I[1] | -5 | Ceramic fcBGA | 1704 | IND | 80.1 |
| LFSCM3GA80EP1-6FF1704I | -6 | Organic fcBGA | 1704 | IND | 80.1 |
| LFSCM3GA80EP1-5FF1704I | -5 | Organic fcBGA | 1704 | IND | 80.1 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| June 2006 (cont.) | 01.2 (cont.) | DC and Switching Characteristics (cont.) | Updated Typical Building Block Performance with ispLEVER 6.0 values. |
| | | | Updated LatticeSC External Switching Characteristics with ispLEVER 6.0 values. |
| | | | Updated Lattice SC Internal Timing Parameters with ispLEVER 6.0 values. |
| | | | Updated Lattice SC Family Timing Adders with ispLEVER 6.0 values |
| | | | Changed % spread from 1 to 0.5 min and from 3 to 1.5 max. |
| | | | Changed conditions to refer to “with multiplication” and “without multiplication”. |
| | | | Changed the formula for $t_{OPJIT}$ with multiplication (same result, different representation). |
| | | Pinout Information | Expanded definition of NC. |
| | | | Expanded definition of GND. |
| | | | Expanded definition of VTT_x. |
| | | | Expanded definition of VCC12. |
| | | | Added accuracy of TEMP pin. |
| | | | Added RESPN_[ULC/URC]. |
| | | | Updated Pin Information Summary with additional devices and packages. |
| | | | Added additional devices and packages pinouts. |
| | | | Removed Power Supply and NC connections table |
| | | | Removed VTT table |
| | | | Removed LFSC25 Logic Signal Connections: 900-Ball ffBGA1 table |
| | | | Changed all VDDP, VDDTX and VDDRX to VCC12. |
| | | Ordering Information | Added dual marking. |
| | | | Added lead free packaging information to part number description. |
| August 2006 | 01.3 | Introduction | Added SC40 1152 information to Table 1-1. |
| | | | Updated Table 1-3 with ispLEVER 6.0 SP1 results. |
| | | Architecture | Added SSTL18 II to Table 2-8. |
| | | | Changed Table 2-10 VCCIO column to “N/A” for LVDS, mini-LVDS, BLVDS25, MLVDS25, HYPT and RSDS. |
| | | | Changed Hypertransport performance to 700 MHz (1400 Mbps) in Table 2-11. |
| | | | Changed SPI4.2 performance to 500 MHz (1000 Mbps) in Table 2-11 |
| | | | Added “On packages that include PROBE_GND, the most accurate measurements will occur between the TEMP pin and the PROBE_GND pin. On packages that do not include PROBE_GND, measurements should be made between the TEMP pin and board ground.” |
| | | | Added VCCIO of 2.5 V for LVPECL33 in table 2-9. |
| | | DC and Switching Characteristics | Updated Typical Building Block Performance with ispLEVER 6.0 SP1 results. |
| | | | Updated Initialization and Standby Supply Current table to break out ICC and ICC12. |
| | | | Updated LatticeSC External Switching Characteristics with ispLEVER 6.0 SP1 results. |
| | | | Updated LatticeSC Internal Timing Parameters with ispLEVER 6.0 SP1 results. |