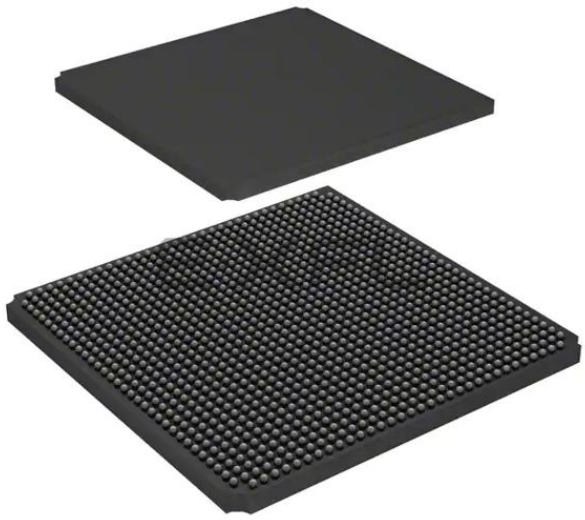
Lattice Semiconductor Corporation - LFSC3GA80E-6FC1152I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BCBGA, FCBGA
Supplier Device Package	1152-CFCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-6fc1152i

DLLs and dynamic glitch free clock MUXs which are required in today's high end system designs. High-speed, high-bandwidth I/O make this family ideal for high-throughput systems.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeSC family of FPGA devices. Synthesis library support for LatticeSC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeSC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeSC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

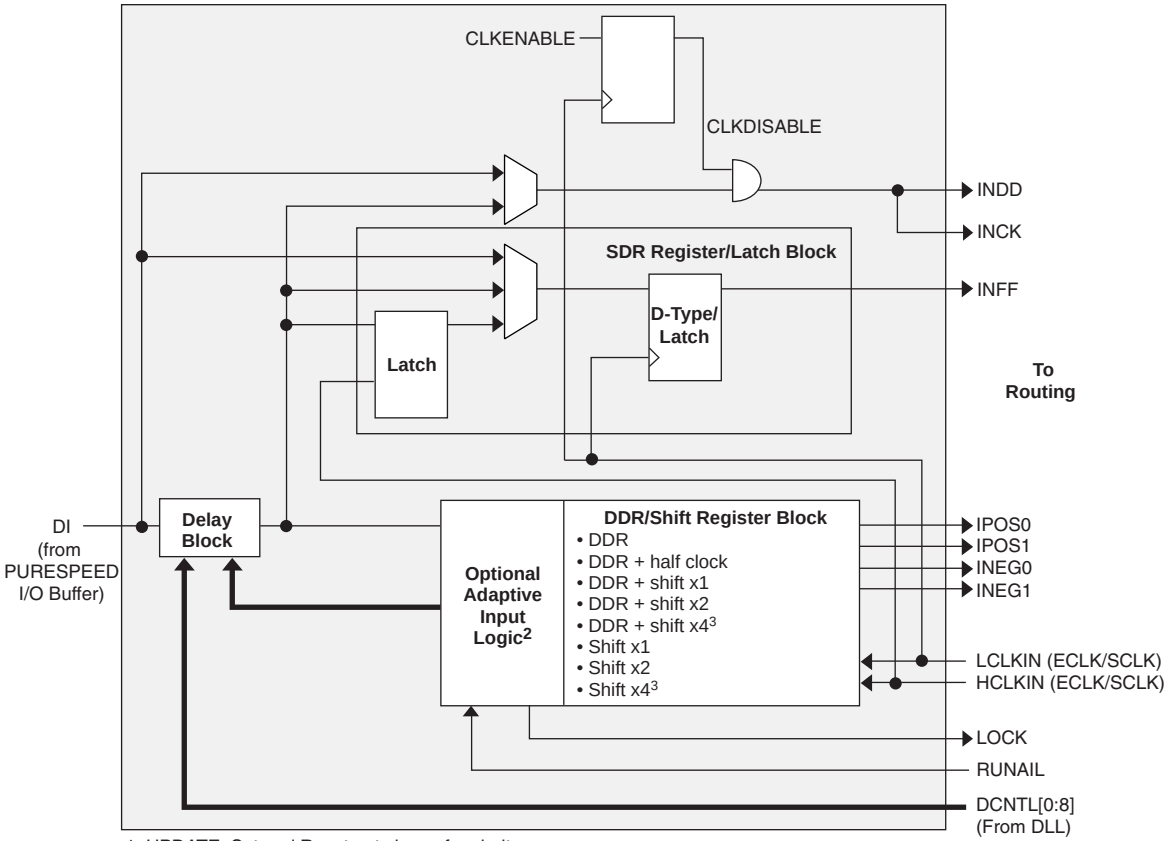
Innovative high-performance FPGA architecture, high-speed SERDES with PCS support, sysMEM embedded memory and high performance I/O are combined in the LatticeSC to provide excellent performance for today's leading edge systems designs. Table 1-3 details the performance of several common functions implemented within the LatticeSC.

Table1-3. Speed Performance for Typical Functions[1]

Functions	Performance (MHz)[2]
32-bit Address Decoder	539
64-bit Address Decoder	517
32:1 Multiplexer	779
64-bit Adder (ripple)	353
32x8 Distributed Single Port (SP) RAM	768
64-bit Counter (up or down counter, non-loadable)	369
True Dual-Port 1024x18 bits	372
FIFO Port A: x36 bits, B: x9 bits	375

1. For additional information, see Typical Building BLock Function Performance table in this data sheet.
2. Advance information (-7 speed grade).

Figure 2-20. Input Register Block[1]



1. UPDATE, Set and Reset not shown for clarity
2. Adaptive input logic is only available in selected PIO
3. By four shift modes utilize DDR/shift register block from paired PIO.
4. CLKDISABLE is used to block the transitions on the DQS pin during post-amble. Its main use is to disable DQS (typically found in DDR memory interfaces) or other clock signals. It can also be used to disable any/all input signals to save power.

PURESPEED I/O Buffer Banks

LatticeSC devices have seven PURESPEED I/O buffer banks; each is capable of supporting multiple I/O standards. Each PURESPEED I/O bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-26 shows the seven banks and their associated supplies. Table 2-7 lists the maximum number of I/Os per bank for the whole LatticeSC family.

In the LatticeSC devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI33 and PCIX33) are powered using V_{CCIO}. In addition to the bank V_{CCIO} supplies, the LatticeSC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers. VCCAUX also powers a predriver of single-ended output buffers to enhance buffer performance.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeSC devices any I/O pin in a bank can be configured to be a dedicated reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Differential drivers have user selectable internal or external bias. External bias is brought in by the VREF1 pin in the bank. External bias for differential buffers is needed for applications that requires tighter than standard output common mode range.

Since a bank can have only one external bias circuit for differential drivers, LVDS and RSDS differential outputs can be mixed in a bank.

If a differential driver is configured in a bank, one pin in that bank becomes a DIFFR pin. This DIFFR pin must be connected to ground via an external 1K +/-1% ohm resistor. Note that differential drivers are not supported in banks 1, 4 and 5.

In addition, there are dedicated Terminating Supply (V_{TT}) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These V_{TT} pins are available in banks 2-7, these pins are not available in some packages. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.

There are further restrictions on the use of V_{TT} pins, for additional details refer to technical information at the end of this data sheet.

Table 2-9. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)	On-chip Termination
Single Ended Interfaces			
LVTTL33[3]	—	3.3	None
LVCMOS 33, 25, 18, 15, 12[3]	—	3.3/2.5/1.8/1.5/1.2	None
PCI33, PCIX33, AGP1X33[3]	—	3.3	None
PCIX15	0.75	1.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
AGP2X33	1.32	—	None
HSTL18_I, II	0.9	1.8[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL18_III, IV	1.08	1.8[2]	None / V_{CCIO}: 50
HSTL15_I, II	0.75	1.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL15_III, IV	0.9	1.5[2]	None / V_{CCIO}: 50
SSTL33_I, II	1.5	3.3	None
SSTL25_I, II	1.25	2.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL18_I, II	0.9	1.8[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
GTL+, GTL	1.0 / 0.8	1.5 / 1.2[2]	None / V_{CCIO}: 50
Differential Interfaces			
SSTL18D_I, II	—	1.8[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL25D_I, II	—	2.5[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL33D_I, II	—	3.3	None
HSTL15D_I, II	—	1.5[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL18D_I, II	—	1.8[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
LVDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240
Mini-LVDS	—	—	None / Diff: 120, 150 / Diff to V_{CMT}: 120, 150
BLVDS25	—	—	None
MLVDS25	—	—	None
RSDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240
LVPECL33	—	≤2.5	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.
2. V_{CCIO} needed for on-chip termination to $V_{CCIO}/2$ or V_{CCIO} only. V_{CCIO} is not specified for off-chip termination or V_{TT} termination.
3. All ratioed input buffers and dedicated pin input buffers include hysteresis with a typical value of 50mV.

Table 2-10. Supported Output Standards[4]

Output Standard	Drive	V_{CCIO} (Nom)	On-chip Output Termination
Single-ended Interfaces			
LVTTL/D[1]	8mA, 16mA, 24mA	3.3	None.
LVCMOS33/D[1]	8mA, 16mA, 24mA	3.3	None
LVCMOS25/D[1, 2]	4mA, 8mA, 12mA, 16mA,	2.5	None, series: 25, 33, 50, 100
LVCMOS18/D[1, 2]	4mA, 8mA, 12mA, 16mA,	1.8	None, series: 25, 33, 50, 100
LVCMOS15/D[1, 2]	4mA, 8mA, 12mA, 16mA,	1.5	None, series: 25, 33, 50, 100
LVCMOS12/D[1, 2]	2mA, 4mA, 8mA, 12mA	1.2	None, series: 25, 33, 50, 100
PCIX15	N/A	1.5	None
PCI33, PCIX33, AGP1X33, AGP2X33	N/A	3.3	None
HSTL18_I	N/A	1.8	None, series: 50
HSTL18_II	N/A	1.8	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
HSTL15_I	N/A	1.5	None, series: 50
HSTL15_II	N/A	1.5	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
SSTL33_I	N/A	3.3	None
SSTL33_II	N/A	3.3	None
SSTL25_I	N/A	2.5	None, series: 50
SSTL25_II	N/A	2.5	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
SSTL18_ I	N/A	1.8	None, series: 33
SSTL18_II	N/A	1.8	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
Differential Interfaces			
SSTL18D_I	N/A	1.8	None, series: 33
SSTL25D_I	N/A	2.5	None, series: 50
SSTL18D_II, SSTL25D_II	N/A	1.2/2.5/3.3	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
SSTL33D_I, II	N/A	3.3	None
HSTL15D_I, HSTL18D_I	N/A	1.5/1.8	None, series: 50
HST15D_II, HSTL18D_II	N/A	1.5/1.8	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
LVDS	2mA, 3.5mA, 4mA, 6mA	N/A	None
Mini-LVDS	3.5mA, 4mA, 6mA	N/A	None
BLVDS25	N/A	N/A	None
MLVDS25	N/A	N/A	None
LVPECL33[3]	N/A	3.3	None
RSDS	2mA, 3.5mA, 4mA, 6mA	N/A	None

1. D refers to open drain capability.
2. User can select either drive current or driver impedances but not both.
3. Emulated with external resistors.
4. No GTL or GTL+ support.

PCI Clamp

A programmable PCI clamp is available on the top and bottom banks of the device. The PCI clamp can be turned “ON” or “OFF” on each pin independently. The PCI clamp is used when implementing a 3.3V PCI interface. The

PURESPEED I/O Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input voltage		0	—	2.4	V
V_{THD}	Differential input threshold (Q-$\overline{Q}$)		+/-100	—	—	mV
V_{CM}	Input common mode voltage		0.05	1.2	2.35	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{SAB}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	12	mA
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	500	ps	T_R, T_F

Notes:
1. Data is for 3.5mA differential current drive. Other differential driver current options are available.
2. If the low power mode of the input buffer is used, the minimum V_{CM} is 600 mV.

Mini-LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	ohms
R_T	Differential termination resistance	60	100	150	ohms
V_{OD}	Output voltage, differential, $\|V_{OP} - V_{OM}\|$	300	—	600	mV
V_{OS}	Output voltage, common mode, $\|V_{OP} + V_{OM}\|/2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD}, between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS}, between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $\|V_{INP} - V_{INM}\|$	200	—	600	mV
V_{CM}	Input voltage, common mode, $\|V_{INP} + V_{INM}\|/2$	0.3+(V_{THD}/2)	—	2.1-(V_{THD}/2)	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	500	ps
T_{ODUTY}	Output clock duty cycle	45	—	55	%
T_{IDUTY}	Input clock duty cycle	40	—	60	%

Note: Data is for 6mA differential current drive. Other differential driver current options are available.

Switching Characteristics

All devices are 100% functionally tested. Listed below are representative values of internal and external timing parameters. For more specific, more precise, and worst-case guaranteed data at a particular temperature and voltage, use the values reported by the static timing analyzer in the ispLEVER design tool from Lattice and back-annotate to the simulation net list.

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
GTLPLUS15	GTLPLUS15	-0.013	-0.017	0.012	0.004	0.037	0.024	ns
GTL12	GTL12	-0.063	-0.071	-0.007	-0.048	0.056	-0.032	ns
Output Adjusters								
LVDS	LVDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
RSDS	RSDS	0.708	0.854	0.856	1.021	1.005	1.189	ns
BLVDS25	BLVDS	-0.129	0.05	-0.136	0.069	-0.136	0.083	ns
MLVDS25	MLVDS	-0.059	0.059	-0.057	0.096	-0.054	0.133	ns
LVPECL33	LVPECL	-0.334	-0.181	-0.325	-1.389	-0.315	-2.598	ns
HSTL18_I	HSTL_18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18_II	HSTL_18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL18D_I	Differential HSTL 18 class I	0.132	0.209	0.153	0.24	0.175	0.272	ns
HSTL18D_II	Differential HSTL 18 class II	0.24	0.176	0.268	0.255	0.298	0.333	ns
HSTL15_I	HSTL_15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15_II	HSTL_15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
HSTL15D_I	Differential HSTL 15 class I	0.096	0.172	0.112	0.198	0.129	0.224	ns
HSTL15D_II	Differential HSTL 15 class II	0.208	0.131	0.233	0.203	0.259	0.275	ns
SSTL33_I	SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33_II	SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL33D_I	Differential SSTL_3 class I	0.133	0.177	0.11	0.166	0.088	0.154	ns
SSTL33D_II	Differential SSTL_3 class II	0.173	0.247	0.164	0.253	0.156	0.258	ns
SSTL25_I	SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25_II	SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL25D_I	Differential SSTL_2 class I	0.215	0.125	0.239	0.228	0.264	0.331	ns
SSTL25D_II	Differential SSTL_2 class II	0.277	0.181	0.311	0.284	0.345	0.387	ns
SSTL18_I	SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18_II	SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
SSTL18D_I	Differential SSTL_2 class I	0.16	0.081	0.179	0.173	0.199	0.265	ns
SSTL18D_II	Differential SSTL_2 class II	0.238	0.15	0.263	0.244	0.295	0.338	ns
LVTTL33_8mA	LVTTL 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVTTL33_16mA	LVTTL 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVTTL33_24mA	LVTTL 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	-0.346	-0.165	-0.496	-0.296	-0.646	-0.428	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive	-0.11	-0.18	-0.218	-0.32	-0.325	-0.46	ns
LVCMOS33_24mA	LVCMOS 3.3 24mA drive	-0.012	-0.18	-0.099	-0.321	-0.185	-0.463	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	-0.174	0.004	-0.195	0.002	-0.215	0	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	0	0	0	0	0	0	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.094	-0.025	0.107	0.096	0.12	0.216	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive	0.145	-0.054	0.162	0.063	0.181	0.179	ns
LVCMOS25_OD	LVCMOS 2.5 open drain	0.073	-0.125	0.081	-0.081	0.091	-0.09	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	-0.278	-0.099	-0.312	-0.115	-0.345	-0.131	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	-0.073	-0.078	-0.078	-0.084	-0.083	-0.089	ns

LatticeSC/M sysCONFIG Port Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
General Configuration Timing				
t_{SMODE}	M[3:0] Setup Time to INITN High	0	—	ns
t_{HMODE}	M[3:0] Hold Time from INITN High	600	—	ns
t_{RW}	RESETN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
t_{PGW}	PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
$f_{ESB\_CLK\_FRQ}$	System Bus ESB_CLK Frequency (No Wait States)	—	133	MHz
sysCONFIG Master Parallel Configuration Mode				
t_{SMB}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMB}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMB}	RCLK Low Time (Non-compressed Bitstreams)	0.5	0.5	CCLK periods
	RCLK Low Time (Compressed Bitstreams)	0.5	7.5	CCLK periods
t_{CHMB}	RCLK High Time	0.5	0.5	CCLK periods
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CSCK Low	—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low	0	2	µs
t_{SCK}	CSCK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CSCK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN Low to CSCK high Setup Time	—	15	ns
f_{MAXSPI}	Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0)	—	50	MHz
t_{SUSPI}	SOSPI/D0 Data Setup Time Before CSCK	7	—	ns
t_{HSPI}	SOSPI/D0 Data Hold Time After CSCK	2	—	ns
	Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
	Duty Cycle	40	60	%
sysCONFIG Master Serial Configuration Mode				
t_{SMS}	DIN Setup Time	4.4	—	ns
t_{HMS}	DIN Hold Time	0	—	ns
f_{CMS}	CCLK Frequency (No Divider)	90	190	MHz
f_{C_DIV}	CCLK Frequency (Div 128)	0.70	1.48	MHz
t_{D}	CCLK to DOUT Delay	—	7.5	ns
sysCONFIG Master Parallel Configuration Mode				
t_{AVMP}	RCLK to Address Valid	—	10	ns
t_{SMP}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMP}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMP}	RCLK Low Time (Non-compressed Bitstream)	7.5	7.5	CCLK periods
	RCLK Low Time (Compressed Bitstream)	0.5	63.5	
t_{CHMP}	RCLK High Time	0.5	0.5	CCLK periods
t_{DMP}	CCLK to DOUT	—	7.5	ns

Pin Information Summary

Pin Type		256 fpBGA	900 fpBGA		1020 fcBGA	
		LFSC/M15	LFSC/M15	LFSC/M25	LFSC/M25	LFSC/M40
Single Ended User I/O		139	300	378	476	562
Differential Pair User I/O		60	141	182	235	277
LVDS Output Pairs		22	44	60	60	78
Configuration	Dedicated	9	11	11	11	11
	Muxes/MPI sysBus	0	55	55	55	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		2	4	4	4	4
VCC		10	46	46	40	40
VCC12		10	35	35	36	36
VCCAUX		10	36	36	32	32
VCCIO	Bank 1	3	18	18	10	10
	Bank 2	2	14	14	8	8
	Bank 3	2	15	15	10	10
	Bank 4	3	15	15	10	10
	Bank 5	3	15	15	10	10
	Bank 6	2	15	15	10	10
	Bank 7	2	16	16	8	8
VTT	Bank 2	0	2	2	2	2
	Bank 3	0	3	3	3	3
	Bank 4	0	3	3	3	3
	Bank 5	0	3	3	3	3
	Bank 6	0	3	3	3	3
	Bank 7	0	2	2	2	2
GND		26	177	177	134	134
NC		0	102	24	92	6
Single Ended User / Differential I/O per Bank	Bank 1	21/8	63/30	63/30	68/32	68/32
	Bank 2	15/7	26/13	30/15	34/17	54/27
	Bank 3	19/8	43/20	62/29	84/42	94/47
	Bank 4	25/11	50/22	66/32	84/41	99/48
	Bank 5	25/11	49/23	65/32	88/44	99/49
	Bank 6	19/8	43/20	62/29	84/42	94/47
	Bank 7	15/7	26/13	30/15	34/17	54/27
LVDS Output Pairs Per Bank	Bank 2	5	7	9	9	15
	Bank 3	6	15	21	21	24
	Bank 6	6	15	21	21	24
	Bank 7	5	7	9	9	15
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		28	60	60	108	108
Total		256	900	900	1020	1152

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P22	VCCIO2	-		VCCIO2	-	
R22	VCCIO2	-		VCCIO2	-	
AA23	VCCIO3	-		VCCIO3	-	
AA24	VCCIO3	-		VCCIO3	-	
AB23	VCCIO3	-		VCCIO3	-	
AB24	VCCIO3	-		VCCIO3	-	
T22	VCCIO3	-		VCCIO3	-	
U22	VCCIO3	-		VCCIO3	-	
V22	VCCIO3	-		VCCIO3	-	
W22	VCCIO3	-		VCCIO3	-	
Y22	VCCIO3	-		VCCIO3	-	
Y23	VCCIO3	-		VCCIO3	-	
Y24	VCCIO3	-		VCCIO3	-	
AB16	VCCIO4	-		VCCIO4	-	
AB17	VCCIO4	-		VCCIO4	-	
AB18	VCCIO4	-		VCCIO4	-	
AB19	VCCIO4	-		VCCIO4	-	
AB20	VCCIO4	-		VCCIO4	-	
AC20	VCCIO4	-		VCCIO4	-	
AC21	VCCIO4	-		VCCIO4	-	
AC22	VCCIO4	-		VCCIO4	-	
AD20	VCCIO4	-		VCCIO4	-	
AD21	VCCIO4	-		VCCIO4	-	
AD22	VCCIO4	-		VCCIO4	-	
AB11	VCCIO5	-		VCCIO5	-	
AB12	VCCIO5	-		VCCIO5	-	
AB13	VCCIO5	-		VCCIO5	-	
AB14	VCCIO5	-		VCCIO5	-	
AB15	VCCIO5	-		VCCIO5	-	
AC10	VCCIO5	-		VCCIO5	-	
AC11	VCCIO5	-		VCCIO5	-	
AC9	VCCIO5	-		VCCIO5	-	
AD10	VCCIO5	-		VCCIO5	-	
AD11	VCCIO5	-		VCCIO5	-	
AD9	VCCIO5	-		VCCIO5	-	
AA7	VCCIO6	-		VCCIO6	-	
AA8	VCCIO6	-		VCCIO6	-	
AB7	VCCIO6	-		VCCIO6	-	
AB8	VCCIO6	-		VCCIO6	-	
T9	VCCIO6	-		VCCIO6	-	
U9	VCCIO6	-		VCCIO6	-	
V9	VCCIO6	-		VCCIO6	-	
W9	VCCIO6	-		VCCIO6	-	
Y7	VCCIO6	-		VCCIO6	-	
Y8	VCCIO6	-		VCCIO6	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH27	PB5C	5		PB5C	5	
AH26	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AN32	PB7A	5		PB7A	5	
AP32	PB7B	5		PB7B	5	
AF25	PB7C	5		PB7C	5	
AE25	PB7D	5		PB7D	5	
AN31	PB8A	5		PB9A	5	
AN30	PB8B	5		PB9B	5	
AK29	PB8C	5		PB9C	5	
AK28	PB8D	5		PB9D	5	
AP31	PB9A	5		PB11A	5	
AP30	PB9B	5		PB11B	5	
AD24	PB9C	5		PB11C	5	
AE24	PB9D	5		PB11D	5	
AM29	PB11A	5		PB13A	5	
AM28	PB11B	5		PB13B	5	
AJ27	PB11C	5		PB13C	5	
AJ26	PB11D	5		PB13D	5	
AP29	PB13A	5		PB15A	5	
AP28	PB13B	5		PB15B	5	
AK27	PB13C	5		PB15C	5	
AK26	PB13D	5		PB15D	5	
AN29	PB15A	5		PB17A	5	
AN28	PB15B	5		PB17B	5	
AG25	PB15C	5		PB17C	5	
AG24	PB15D	5		PB17D	5	
AL26	PB17A	5		PB19A	5	
AL25	PB17B	5		PB19B	5	
AG23	PB17C	5		PB19C	5	
AG22	PB17D	5		PB19D	5	
AN27	PB19A	5		PB21A	5	
AN26	PB19B	5		PB21B	5	
AF24	PB19C	5		PB21C	5	
AF23	PB19D	5		PB21D	5	
AP27	PB22A	5		PB24A	5	
AP26	PB22B	5		PB24B	5	
AK25	PB22C	5		PB24C	5	
AK24	PB22D	5		PB24D	5	
AN25	PB25A	5		PB27A	5	
AN24	PB25B	5		PB27B	5	
AE22	PB25C	5		PB27C	5	
AE21	PB25D	5		PB27D	5	
AM26	PB26A	5		PB29A	5	
AM25	PB26B	5		PB29B	5	
AF22	PB26C	5		PB29C	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD8	PR65C	3		PR89C	3	
AJ3	PR65B	3		PR89B	3	
AH3	PR65A	3		PR89A	3	
AD7	PR62D	3		PR86D	3	
AC7	PR62C	3		PR86C	3	
AJ2	PR62B	3		PR86B	3	
AH2	PR62A	3		PR86A	3	
AF6	PR61D	3		PR85D	3	
AF5	PR61C	3		PR85C	3	
AF4	PR61B	3		PR85B	3	
AE4	PR61A	3		PR85A	3	
AD6	PR60D	3		PR84D	3	
AC6	PR60C	3		PR84C	3	
AG2	PR60B	3		PR84B	3	
AF2	PR60A	3		PR84A	3	
AC8	PR58D	3		PR82D	3	
AB8	PR58C	3		PR82C	3	
AK1	PR58B	3		PR82B	3	
AJ1	PR58A	3		PR82A	3	
AB10	PR57D	3		PR81D	3	
AA10	PR57C	3		PR81C	3	
AF3	PR57B	3		PR81B	3	
AE3	PR57A	3		PR81A	3	
AE5	PR56D	3		PR80D	3	
AD5	PR56C	3		PR80C	3	
AE2	PR56B	3		PR80B	3	
AD2	PR56A	3		PR80A	3	
AC5	PR53D	3		PR78D	3	
AB5	PR53C	3		PR78C	3	
AF1	PR53B	3		PR78B	3	
AE1	PR53A	3		PR78A	3	
AA11	PR52D	3		PR77D	3	
Y11	PR52C	3		PR77C	3	
AC4	PR52B	3		PR77B	3	
AB4	PR52A	3		PR77A	3	
AA8	PR51D	3	DIFFR_3	PR76D	3	DIFFR_3
AA9	PR51C	3		PR76C	3	
AC3	PR51B	3		PR76B	3	
AB3	PR51A	3		PR76A	3	
AA7	PR49D	3		PR65D	3	
Y7	PR49C	3		PR65C	3	
AA2	PR49B	3		PR65B	3	
Y2	PR49A	3		PR65A	3	
AA6	PR48D	3		PR63D	3	
Y6	PR48C	3		PR63C	3	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y4	PR48B	3		PR63B	3	
W4	PR48A	3		PR63A	3	
W11	PR47D	3		PR60D	3	
V11	PR47C	3		PR60C	3	
W2	PR47B	3		PR60B	3	
V2	PR47A	3		PR60A	3	
W9	PR45D	3		PR57D	3	
V9	PR45C	3		PR57C	3	
V1	PR45B	3		PR57B	3	
U1	PR45A	3		PR57A	3	
W10	PR44D	3		PR56D	3	
V10	PR44C	3		PR56C	3	
U2	PR44B	3		PR56B	3	
T2	PR44A	3		PR56A	3	
Y8	PR43D	3		PR55D	3	
W8	PR43C	3	VREF1_3	PR55C	3	VREF1_3
W5	PR43B	3		PR55B	3	
V5	PR43A	3		PR55A	3	
V7	PR40D	3	PCLKC3_2	PR52D	3	PCLKC3_2
U7	PR40C	3	PCLKT3_2	PR52C	3	PCLKT3_2
T1	PR40B	3		PR52B	3	
R1	PR40A	3		PR52A	3	
V8	PR39D	3	PCLKC3_3	PR51D	3	PCLKC3_3
U8	PR39C	3	PCLKT3_3	PR51C	3	PCLKT3_3
U5	PR39B	3		PR51B	3	
T5	PR39A	3		PR51A	3	
V6	PR38D	3	PCLKC3_1	PR50D	3	PCLKC3_1
U6	PR38C	3	PCLKT3_1	PR50C	3	PCLKT3_1
T4	PR38B	3	PCLKC3_0	PR50B	3	PCLKC3_0
T3	PR38A	3	PCLKT3_0	PR50A	3	PCLKT3_0
U9	PR36D	2	PCLKC2_2	PR48D	2	PCLKC2_2
T9	PR36C	2	PCLKT2_2	PR48C	2	PCLKT2_2
R2	PR36B	2	PCLKC2_0	PR48B	2	PCLKC2_0
P2	PR36A	2	PCLKT2_0	PR48A	2	PCLKT2_0
T11	PR35D	2	PCLKC2_3	PR47D	2	PCLKC2_3
U11	PR35C	2	PCLKT2_3	PR47C	2	PCLKT2_3
R4	PR35B	2	PCLKC2_1	PR47B	2	PCLKC2_1
R3	PR35A	2	PCLKT2_1	PR47A	2	PCLKT2_1
T8	PR34D	2		PR46D	2	
R8	PR34C	2		PR46C	2	
P1	PR34B	2		PR46B	2	
N1	PR34A	2		PR46A	2	
R6	PR31D	2		PR43D	2	
P6	PR31C	2		PR43C	2	
M1	PR31B	2		PR43B	2	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
G27	A_REFCLKP_L	-	
H27	A_REFCLKN_L	-	
H25	VCC12	-	
H26	RESP_ULC	-	
B33	RESETN	1	
C34	TSALLN	1	
D34	DONE	1	
C33	INITN	1	
J27	M0	1	
K27	M1	1	
M26	M2	1	
L26	M3	1	
F30	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
G30	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
H28	PL15C	7	
J28	PL15D	7	
F31	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N25	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P25	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
D33	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E33	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
H29	PL18C	7	
J29	PL18D	7	VREF2_7
F32	PL19A	7	
G32	PL19B	7	
P26	PL19C	7	
N26	PL19D	7	
H30	PL26A	7	
J30	PL26B	7	
L28	PL26C	7	
M28	PL26D	7	
J31	PL43A	7	
K31	PL43B	7	
L27	PL43C	7	VREF1_7
M27	PL43D	7	DIFFR_7
J32	PL45A	7	
K32	PL45B	7	
L29	PL45C	7	
M29	PL45D	7	
H33	PL47A	7	
J33	PL47B	7	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
N27	PL47C	7	
P27	PL47D	7	
K33	PL49A	7	
L33	PL49B	7	
M30	PL49C	7	
N30	PL49D	7	
M31	PL51A	7	
N31	PL51B	7	
P24	PL51C	7	
R24	PL51D	7	
M33	PL56A	7	
N33	PL56B	7	
U25	PL56C	7	
T25	PL56D	7	
L34	PL57A	7	
M34	PL57B	7	
P29	PL57C	7	
R29	PL57D	7	
N34	PL60A	7	
P34	PL60B	7	
R27	PL60C	7	
T27	PL60D	7	
R32	PL61A	7	PCLKT7_1
R31	PL61B	7	PCLKC7_1
U24	PL61C	7	PCLKT7_3
T24	PL61D	7	PCLKC7_3
P33	PL62A	7	PCLKT7_0
R33	PL62B	7	PCLKC7_0
T26	PL62C	7	PCLKT7_2
U26	PL62D	7	PCLKC7_2
T32	PL64A	6	PCLKT6_0
T31	PL64B	6	PCLKC6_0
U29	PL64C	6	PCLKT6_1
V29	PL64D	6	PCLKC6_1
T30	PL65A	6	
U30	PL65B	6	
U27	PL65C	6	PCLKT6_3
V27	PL65D	6	PCLKC6_3
R34	PL66A	6	
T34	PL66B	6	
U28	PL66C	6	PCLKT6_2
V28	PL66D	6	PCLKC6_2
V30	PL69A	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W33	PL42C	7		PL56C	7	
Y33	PL42D	7		PL56D	7	
W37	PL43A	7		PL57A	7	
Y37	PL43B	7		PL57B	7	
Y32	PL43C	7		PL57C	7	
AA32	PL43D	7		PL57D	7	
U38	PL46A	7		PL60A	7	
V38	PL46B	7		PL60B	7	
W34	PL46C	7		PL60C	7	
Y34	PL46D	7		PL60D	7	
T40	PL47A	7	PCLKT7_1	PL61A	7	PCLKT7_1
U40	PL47B	7	PCLKC7_1	PL61B	7	PCLKC7_1
AA33	PL47C	7	PCLKT7_3	PL61C	7	PCLKT7_3
AB33	PL47D	7	PCLKC7_3	PL61D	7	PCLKC7_3
R42	PL48A	7	PCLKT7_0	PL62A	7	PCLKT7_0
T42	PL48B	7	PCLKC7_0	PL62B	7	PCLKC7_0
AA34	PL48C	7	PCLKT7_2	PL62C	7	PCLKT7_2
AB34	PL48D	7	PCLKC7_2	PL62D	7	PCLKC7_2
U41	PL50A	6	PCLKT6_0	PL64A	6	PCLKT6_0
V41	PL50B	6	PCLKC6_0	PL64B	6	PCLKC6_0
V36	PL50C	6	PCLKT6_1	PL64C	6	PCLKT6_1
W36	PL50D	6	PCLKC6_1	PL64D	6	PCLKC6_1
U42	PL51A	6		PL65A	6	
V42	PL51B	6		PL65B	6	
AB31	PL51C	6	PCLKT6_3	PL65C	6	PCLKT6_3
AC31	PL51D	6	PCLKC6_3	PL65D	6	PCLKC6_3
W38	PL52A	6		PL66A	6	
Y38	PL52B	6		PL66B	6	
AA35	PL52C	6	PCLKT6_2	PL66C	6	PCLKT6_2
AB35	PL52D	6	PCLKC6_2	PL66D	6	PCLKC6_2
W39	PL55A	6		PL69A	6	
Y39	PL55B	6		PL69B	6	
AB32	PL55C	6	VREF1_6	PL69C	6	VREF1_6
AC32	PL55D	6		PL69D	6	
W40	PL56A	6		PL70A	6	
Y40	PL56B	6		PL70B	6	
AA36	PL56C	6		PL70C	6	
AB36	PL56D	6		PL70D	6	
W41	PL57A	6		PL71A	6	
Y41	PL57B	6		PL71B	6	
AA37	PL57C	6		PL71C	6	
AB37	PL57D	6		PL71D	6	
W42	PL59A	6		PL73A	6	
Y42	PL59B	6		PL73B	6	
AC33	PL59C	6		PL73C	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP26	PB41C	5		PB43C	5	
AN26	PB41D	5		PB43D	5	
AY30	PB43A	5		PB45A	5	
AY29	PB43B	5		PB45B	5	
AU30	PB43C	5		PB45C	5	
AU31	PB43D	5		PB45D	5	
AV27	PB44A	5		PB46A	5	
AV26	PB44B	5		PB46B	5	
AT28	PB44C	5		PB46C	5	
AT27	PB44D	5		PB46D	5	
BA29	PB45A	5		PB47A	5	
BA28	PB45B	5		PB47B	5	
AL25	PB45C	5		PB47C	5	
AM25	PB45D	5		PB47D	5	
BB29	PB47A	5		PB49A	5	
BB28	PB47B	5		PB49B	5	
AN25	PB47C	5		PB49C	5	
AP25	PB47D	5		PB49D	5	
AY27	PB48A	5	PCLKT5_3	PB50A	5	PCLKT5_3
AY26	PB48B	5	PCLKC5_3	PB50B	5	PCLKC5_3
AT25	PB48C	5	PCLKT5_4	PB50C	5	PCLKT5_4
AT24	PB48D	5	PCLKC5_4	PB50D	5	PCLKC5_4
AW27	PB49A	5	PCLKT5_5	PB51A	5	PCLKT5_5
AW26	PB49B	5	PCLKC5_5	PB51B	5	PCLKC5_5
AU29	PB49C	5		PB51C	5	
AU28	PB49D	5		PB51D	5	
BB27	PB51A	5	PCLKT5_0	PB53A	5	PCLKT5_0
BB26	PB51B	5	PCLKC5_0	PB53B	5	PCLKC5_0
AR25	PB51C	5		PB53C	5	
AR24	PB51D	5	VREF2_5	PB53D	5	VREF2_5
BA27	PB52A	5	PCLKT5_1	PB54A	5	PCLKT5_1
BA26	PB52B	5	PCLKC5_1	PB54B	5	PCLKC5_1
AP24	PB52C	5	PCLKT5_6	PB54C	5	PCLKT5_6
AN24	PB52D	5	PCLKC5_6	PB54D	5	PCLKC5_6
AV25	PB53A	5	PCLKT5_2	PB55A	5	PCLKT5_2
AV24	PB53B	5	PCLKC5_2	PB55B	5	PCLKC5_2
AU27	PB53C	5	PCLKT5_7	PB55C	5	PCLKT5_7
AU26	PB53D	5	PCLKC5_7	PB55D	5	PCLKC5_7
BA25	PB55A	5		PB57A	5	
BA24	PB55B	5		PB57B	5	
AU24	PB55C	5		PB57C	5	
AU25	PB55D	5		PB57D	5	
BB24	PB56A	5		PB58A	5	
BB25	PB56B	5		PB58B	5	
AM23	PB56C	5		PB58C	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
A26	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N
C34	D_VDDOB2_L	-		D_VDDOB2_L	-	
B26	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P
C32	VCC12	-		VCC12	-	
E27	D_HDINN2_L	-	PCS 363 CH 2 IN N	D_HDINN2_L	-	PCS 363 CH 2 IN N
D27	D_HDINP2_L	-	PCS 363 CH 2 IN P	D_HDINP2_L	-	PCS 363 CH 2 IN P
G25	D_VDDIB2_L	-		D_VDDIB2_L	-	
F29	VCC12	-		VCC12	-	
H26	D_VDDIB1_L	-		D_VDDIB1_L	-	
F30	VCC12	-		VCC12	-	
D28	D_HDINP1_L	-	PCS 363 CH 1 IN P	D_HDINP1_L	-	PCS 363 CH 1 IN P
E28	D_HDINN1_L	-	PCS 363 CH 1 IN N	D_HDINN1_L	-	PCS 363 CH 1 IN N
B27	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P
F36	VCC12	-		VCC12	-	
A27	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N
F35	D_VDDOB1_L	-		D_VDDOB1_L	-	
A28	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N
M30	D_VDDOB0_L	-		D_VDDOB0_L	-	
B28	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P
F37	VCC12	-		VCC12	-	
E29	D_HDINN0_L	-	PCS 363 CH 0 IN N	D_HDINN0_L	-	PCS 363 CH 0 IN N
D29	D_HDINP0_L	-	PCS 363 CH 0 IN P	D_HDINP0_L	-	PCS 363 CH 0 IN P
H27	D_VDDIB0_L	-		D_VDDIB0_L	-	
G28	VCC12	-		VCC12	-	
J28	C_REFCLKP_L	-		C_REFCLKP_L	-	
K28	C_REFCLKN_L	-		C_REFCLKN_L	-	
F32	VCC12	-		VCC12	-	
G29	C_VDDIB3_L	-		C_VDDIB3_L	-	
C31	VCC12	-		VCC12	-	
D30	C_HDINP3_L	-	PCS 362 CH 3 IN P	C_HDINP3_L	-	PCS 362 CH 3 IN P
E30	C_HDINN3_L	-	PCS 362 CH 3 IN N	C_HDINN3_L	-	PCS 362 CH 3 IN N
B29	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P
F38	VCC12	-		VCC12	-	
A29	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N
J33	C_VDDOB3_L	-		C_VDDOB3_L	-	
A30	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N
K33	C_VDDOB2_L	-		C_VDDOB2_L	-	
B30	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P
J34	VCC12	-		VCC12	-	
F31	C_HDINN2_L	-	PCS 362 CH 2 IN N	C_HDINN2_L	-	PCS 362 CH 2 IN N
E31	C_HDINP2_L	-	PCS 362 CH 2 IN P	C_HDINP2_L	-	PCS 362 CH 2 IN P
G30	C_VDDIB2_L	-		C_VDDIB2_L	-	
H28	VCC12	-		VCC12	-	
C37	C_VDDIB1_L	-		C_VDDIB1_L	-	
H30	VCC12	-		VCC12	-	

Lead-Free Packaging

Commercial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.