Lattice Semiconductor Corporation - LFSC3GA80E-6FC1704I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

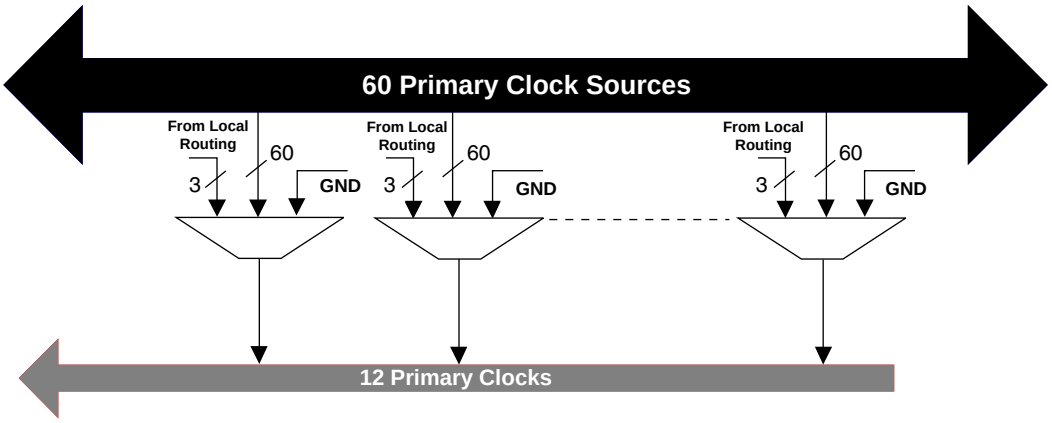
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	904
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1704-BCBGA, FCBGA
Supplier Device Package	1704-CFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-6fc1704i

Figure 2-6. Per Quadrant Clock Selection



Note: GND is available to switch off the network.

Secondary Clocks

In addition to the primary clock network and edge clocks the LatticeSC devices also contain a secondary clock network. Built of X6 style routing elements this secondary clock network is ideal for routing slower speed clock and control signals throughout the device preserving high-speed clock networks for the most timing critical signals.

Edge Clocks

LatticeSC devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per bank for the top and bottom of the device. The left and right sides have eight edge clocks per side for both banks located on that side. Figure 2-7 shows the arrangement of edge clocks.

Edge clock resources can be driven from a variety of sources. Edge clock resources can be driven from:

- Edge clock PIOs in the same bank
- Primary clock PIOs in the same bank
- Routing
- Adjacent PLLs and DLLs
- ELSR output from the clock divider

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
FIFO	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output. A clock is required even in asynchronous read mode.

The EBR memory supports two forms of write behavior for dual port operation:

1. **Normal** — data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output.

2. **Write Through** — a copy of the input data appears at the output of the same port.

FIFO Configuration

The FIFO has a write port with Data-in, WCE, WE and WCLK signals. There is a separate read port with Data-out, RCE, RE and RCLK signals. The FIFO internally generates Almost Full, Full, Almost Empty, and Empty Flags. The Full and Almost Full flags are registered with WCLK. The Empty and Almost Empty flags are registered with RCLK.

Table 2-6. Input/Output/Tristate Gearing Resource Rules

PIO	Input/Output Logic			Tri-State/Bidi	
	x1	x2	x4	x1	x2/x4
A	?	?	?	?	N/A
B	?	No I/O Logic	No I/O Logic	?	N/A
C	?	?	No I/O Logic	?	N/A
D	?	No I/O Logic	No I/O Logic	?	N/A

Note: Pin can still be used without I/O logic.

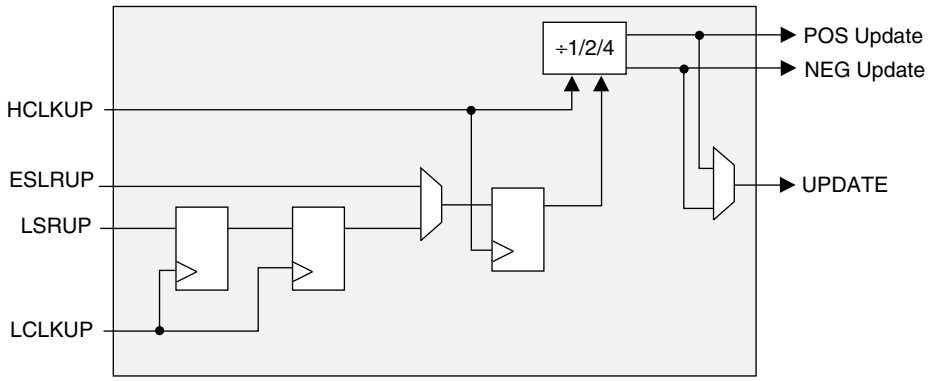
Control Logic Block

The control logic block allows the modification of control signals selected by the routing before they are used in the PIO. It can optionally invert all signals passing through it except the Global Set/Reset. Global Set/Reset can be enabled or disabled. It can route either the edge clock or the clock to the high-speed clock nets. The clock provided to the PIO by routing is used as the slow-speed clocks. In addition this block contains delays that can be inserted in the clock nets to enable Lattice's unique cycle boosting capability.

Update Block

The update block is used to generate the POS update and NEG update signals used by the DDR/Shift register blocks within the PIO. Note the update block is only required in shift modes. This is required in order to do the high speed to low speed handoff. One of these update signals is also selected and output from the PIC as the signal UPDATE. It consists of a shift chain that operates off either the high-speed input or output clock. The values of each register in the chain are set or reset depending on the desired mode of operation. The set/reset signal is generated from either the edge reset ELSR or the local reset LSR. These signals are optionally inverted by the Control Logic Block and provided to the update block as ELSRUP and LSRUP. The Lattice design tools automatically configure and connect the update block when one of the DDR or shift register primitives is used.

Figure 2-25. Update Block



PURESPEED I/O Buffer

Each I/O is associated with a flexible buffer referred to as PURESPEED I/O buffer. These buffers are arranged around the periphery of the device in seven groups referred to as Banks. The PURESPEED I/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL. The availability of programmable on-chip termination for both input and output use, further enhances the utility of these buffers.

Figure 2-26. LatticeSC Banks

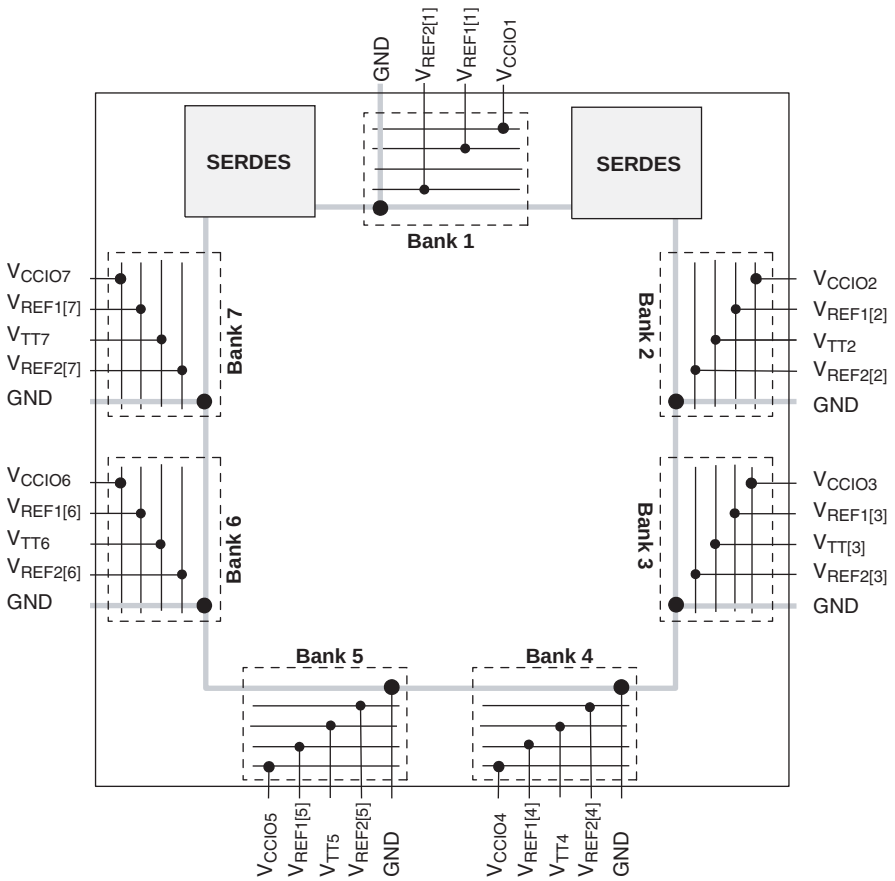


Table 2-7. Maximum Number of I/Os Per Bank in LatticeSC Family

Device	LFSC/M15	LFSC/M25	LFSC/M40	LFSC/M80	LFSC/M115
Bank1	104	80	136	80	136
Bank2	28	36	60	96	136
Bank3	60	84	96	132	156
Bank4	72	100	124	184	208
Bank5	72	100	124	184	208
Bank6	60	84	96	132	156
Bank7	28	36	60	96	136

Note: Not all the I/Os of the Banks are available in all the packages

The LatticeSC devices contain three types of PURESPEED I/O buffers:

1. **Left and Right Sides (Banks 2, 3, 6 and 7)**
   These buffers can support LVCMOS standards up to 2.5V. A differential output driver (for LVDS and RSDS) is provided on all primary PIO pairs (A and B) and differential receivers are available on all pairs. Complimentary drivers are available. Adaptive input logic is available on PIOs A or C.

2. **Top Side (Bank 1)**
   These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but differential drivers for LVDS and RSDS are not available. Adaptive input logic is not available on this side. Complimentary output drivers are available.

- 8-bit SERDES Only
- 10-bit SERDES Only
- SONET (STS-12/STS-48)
- Gigabit Ethernet
- Fibre Channel
- XAUI
- Serial RapidIO
- PCI-Express
- Generic 8b10b

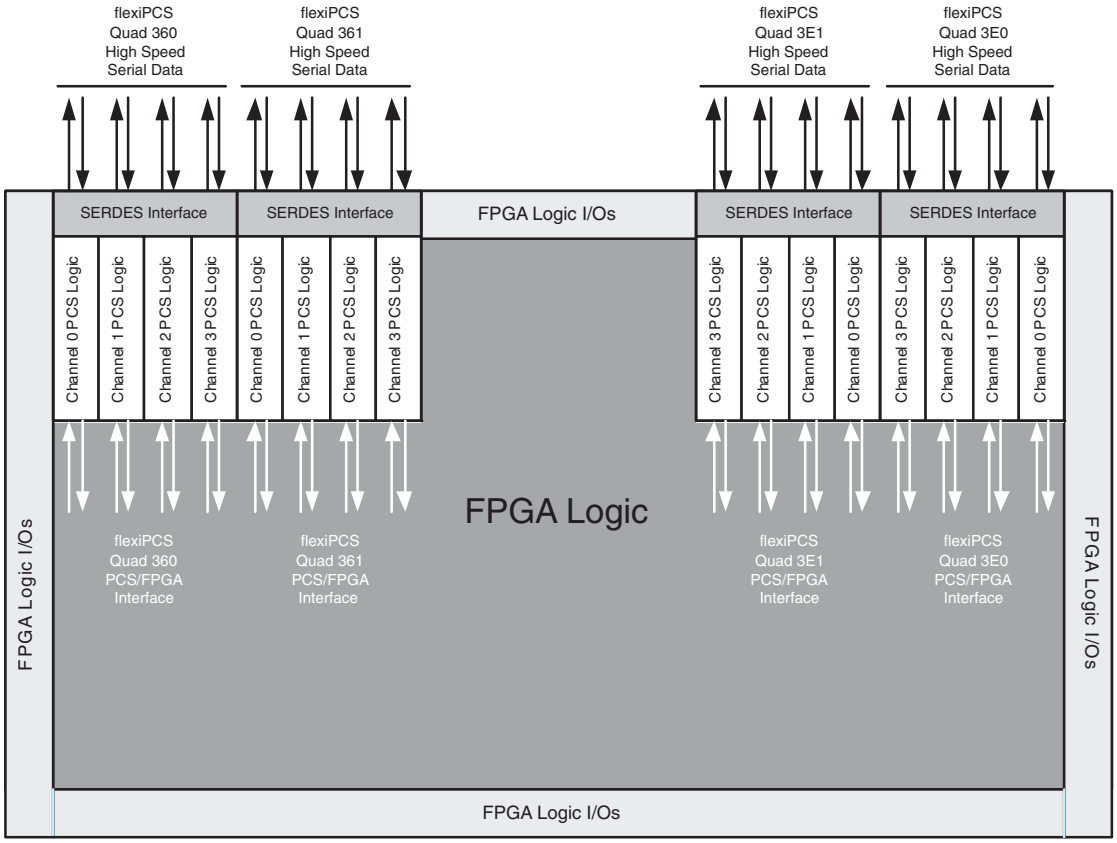
flexiPCS Quad

The flexiPCS logic is arranged in quads containing logic for four independent full-duplex data channels. Each device in the LatticeSC family has up to eight quads of flexiPCS logic. The LatticeSC Family Selection Guide table on the first page of this data sheet contains the number of flexiPCS channels present on the chip. Note that in some packages (particularly lower pin count packages), not all channels from all quads on a given device may be bonded to package pins.

Each quad supports up to four channels of full-duplex data and can be programmed into any one of several protocol based modes. Each quad requires its own reference clock which can be sourced externally or from the FPGA logic. The user can utilize between one and four channels in a quad, depending on the application.

Figure 2-30 shows an example of four flexiPCS quads in a LatticeSC device. Quads are labeled according to the address of their software controlled registers.

Figure 2-30. LatticeSC flexiPCS



Since each quad has its own reference clock, different quads can support different standards on the same chip. This feature makes the LatticeSC family of devices ideal for bridging between different standards.

LatticeSC/M External Switching Characteristics[3]

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL)[2]								
t_{CO}	Global Clock Input to Output - PIO Output Register	2.83	5.74	2.83	6.11	2.83	6.49	ns
t_{SU}	Global Clock Input Setup - PIO Input Register without fixed input delay	-0.66	—	-0.66	—	-0.66	—	ns
t_{H}	Global Clock Input Hold - PIO Input Register without fixed input delay	1.73	—	1.95	—	2.16	—	ns
t_{SU_IDLY}	Global Clock Input Setup - PIO Input Register with input delay	0.86	—	1.03	—	1.20	—	ns
t_{H_IDLY}	Global Clock Input Hold - PIO Input Register with input delay	-0.17	—	-0.17	—	-0.17	—	ns
f_{MAX_PFU}	Global Clock frequency of PFU register	—	700	—	700	—	700	MHz
f_{MAX_IO}	Global Clock frequency of I/O register	—	1000	—	1000	—	1000	MHz
t_{GC_SKEW}	Global Clock skew	—	89	—	103	—	116	ps
General I/O Pin Parameters (using Primary Clock with PLL)[1, 2]								
t_{CO}	Global Clock Input to Output - PIO Output Register	2.25	4.81	2.25	5.08	2.25	5.37	ns
t_{SU}	Global Clock Input Setup - PIO Input Register without fixed input delay	-0.07	—	-0.07	—	-0.07	—	ns
t_{H}	Global Clock Input Hold - PIO Input Register without fixed input delay	0.80	—	0.93	—	1.04	—	ns
General I/O Pin Parameters (using Edge Clock without PLL)[2]								
t_{CO}	Edge Clock Input to Output - PIO Output Register	2.38	4.77	2.38	5.04	2.38	5.33	ns
t_{SU}	Edge Clock Input Setup - PIO Input Register without fixed input delay	-0.08	—	-0.08	—	-0.08	—	ns
t_{H}	Edge Clock Input Hold - PIO Input Register	0.49	—	0.58	—	0.66	—	ns
t_{SU_IDLY}	Edge Clock Input Setup - PIO Input Register with input delay	0.81	—	0.97	—	1.12	—	ns
t_{H_IDLY}	Edge Clock Input Hold - PIO Input Register with input delay	-0.34	—	-0.34	—	-0.34	—	ns
t_{EC_SKEW}	Edge Clock skew	—	28	—	32	—	36	ps
General I/O Pin Parameters (using Latch FF without PLL)[2]								
t_{SU}	Latch FF, Input Setup - PIO Input Register without fixed input delay	-0.14	—	-0.14	—	-0.14	—	ns
t_{H}	Latch FF, Input Hold - PIO Input Register without fixed input delay	0.58	—	0.68	—	0.77	—	ns
t_{SU_IDLY}	Latch FF, Input Setup - PIO Input Register with input delay	0.70	—	0.68	—	0.77	—	ns
t_{H_IDLY}	Latch FF, Input Hold - PIO Input Register with input delay	-0.30	—	-0.30	—	-0.30	—	ns

1. No PLL delay tuning (clock injection removal mode, system clock feedback).
2. Using LVCMOS25 12mA I/O. Timing adders for other supported I/O technologies are specified in the LatticeSC Family Timing Adders table.
3. Complete Timing Parameters for a user design are incorporated when running ispLEVER. This is a sampling of the key timing parameters. Timing specs are for non-AIL applications.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT37D	1	WRN/MPI_WR_N	PT46D	1	WRN/MPI_WR_N
F18	PT37C	1	D7/MPI_DATA7	PT46C	1	D7/MPI_DATA7
C18	PT37B	1	D6/MPI_DATA6	PT46B	1	D6/MPI_DATA6
C17	PT37A	1	D5/MPI_DATA5	PT46A	1	D5/MPI_DATA5
E17	PT36D	1	D4/MPI_DATA4	PT45D	1	D4/MPI_DATA4
E16	PT36C	1	D3/MPI_DATA3	PT45C	1	D3/MPI_DATA3
G18	PT35B	1	D2/MPI_DATA2	PT45B	1	D2/MPI_DATA2
G17	PT35A	1	D1/MPI_DATA1	PT45A	1	D1/MPI_DATA1
B18	PT33B	1	D0/MPI_DATA0	PT43B	1	D0/MPI_DATA0
B17	PT33A	1	QOUT/CEON	PT43A	1	QOUT/CEON
G16	PT32D	1	VREF2_1	PT42D	1	VREF2_1
A18	PT32B	1	DOUT	PT42B	1	DOUT
A17	PT32A	1	MCA_DONE_IN	PT42A	1	MCA_DONE_IN
H18	PT31B	1	MCA_CLK_P1_OUT	PT41B	1	MCA_CLK_P1_OUT
H17	PT31A	1	MCA_CLK_P1_IN	PT41A	1	MCA_CLK_P1_IN
D17	PT29B	1	MCA_CLK_P2_OUT	PT39B	1	MCA_CLK_P2_OUT
D16	PT29A	1	MCA_CLK_P2_IN	PT39A	1	MCA_CLK_P2_IN
F17	PT28D	1	MCA_DONE_OUT	PT38D	1	MCA_DONE_OUT
F16	PT28C	1	BUSYN/RCLK/SCK	PT38C	1	BUSYN/RCLK/SCK
C16	PT28B	1	DP0/MPI_PAR0	PT38B	1	DP0/MPI_PAR0
C15	PT28A	1	MPI_TA	PT38A	1	MPI_TA
B16	PT27B	1	PCLKC1_0	PT37B	1	PCLKC1_0
B15	PT27A	1	PCLKT1_0/MPI_CLK	PT37A	1	PCLKT1_0/MPI_CLK
H16	PT25D	1	DP3/PCLKC1_4/MPI_PAR3	PT35D	1	DP3/PCLKC1_4/MPI_PAR3
A16	PT25B	1	MPI_RETRY	PT35B	1	MPI_RETRY
A15	PT25A	1	A0/MPI_ADDR14	PT35A	1	A0/MPI_ADDR14
G15	PT24D	1	A1/MPI_ADDR15	PT33D	1	A1/MPI_ADDR15
F15	PT24C	1	A2/MPI_ADDR16	PT33C	1	A2/MPI_ADDR16
E15	PT24B	1	A3/MPI_ADDR17	PT33B	1	A3/MPI_ADDR17
D15	PT24A	1	A4/MPI_ADDR18	PT33A	1	A4/MPI_ADDR18
C14	PT23B	1	A5/MPI_ADDR19	PT32B	1	A5/MPI_ADDR19
C13	PT23A	1	A6/MPI_ADDR20	PT32A	1	A6/MPI_ADDR20
H14	PT21C	1	VREF1_1	PT31C	1	VREF1_1
B14	PT21B	1	A7/MPI_ADDR21	PT31B	1	A7/MPI_ADDR21
B13	PT21A	1	A8/MPI_ADDR22	PT31A	1	A8/MPI_ADDR22
G14	PT20B	1	A9/MPI_ADDR23	PT29B	1	A9/MPI_ADDR23
F14	PT20A	1	A10/MPI_ADDR24	PT29A	1	A10/MPI_ADDR24
A14	PT19B	1	A11/MPI_ADDR25	PT28B	1	A11/MPI_ADDR25
A13	PT19A	1	A12/MPI_ADDR26	PT28A	1	A12/MPI_ADDR26
G13	PT17D	1	D11/MPI_DATA11	PT27D	1	D11/MPI_DATA11
H13	PT17C	1	D12/MPI_DATA12	PT27C	1	D12/MPI_DATA12
E14	PT17B	1	A13/MPI_ADDR27	PT27B	1	A13/MPI_ADDR27
E13	PT17A	1	A14/MPI_ADDR28	PT27A	1	A14/MPI_ADDR28
G12	PT15D	1	A16/MPI_ADDR30	PT25D	1	A16/MPI_ADDR30
G11	PT15C	1	D13/MPI_DATA13	PT25C	1	D13/MPI_DATA13

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
U18	GND	-		GND	-	
U19	GND	-		GND	-	
U20	GND	-		GND	-	
V11	GND	-		GND	-	
V12	GND	-		GND	-	
V13	GND	-		GND	-	
V14	GND	-		GND	-	
V15	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V18	GND	-		GND	-	
V19	GND	-		GND	-	
V20	GND	-		GND	-	
W11	GND	-		GND	-	
W12	GND	-		GND	-	
W13	GND	-		GND	-	
W14	GND	-		GND	-	
W15	GND	-		GND	-	
W16	GND	-		GND	-	
W17	GND	-		GND	-	
W18	GND	-		GND	-	
W19	GND	-		GND	-	
W20	GND	-		GND	-	
Y11	GND	-		GND	-	
Y12	GND	-		GND	-	
Y13	GND	-		GND	-	
Y14	GND	-		GND	-	
Y15	GND	-		GND	-	
Y16	GND	-		GND	-	
Y17	GND	-		GND	-	
Y18	GND	-		GND	-	
Y19	GND	-		GND	-	
Y20	GND	-		GND	-	
H2	VCCIO7	-		VCCIO7	-	
N4	VCCIO7	-		VCCIO7	-	
N6	VCCIO7	-		VCCIO7	-	
J2	VCCIO7	-		VCCIO7	-	
L2	VCCIO7	-		VCCIO7	-	
H4	VCCIO7	-		VCCIO7	-	
AB2	VCCIO6	-		VCCIO6	-	
AD1	VCCIO6	-		VCCIO6	-	
W4	VCCIO6	-		VCCIO6	-	
AA4	VCCIO6	-		VCCIO6	-	
AE7	VCCIO5	-		VCCIO5	-	
AH6	VCCIO5	-		VCCIO5	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT24A	1	MPI_TEA	PT30A	1	MPI_TEA
J18	PT23D	1	D14/MPI_DATA14	PT28D	1	D14/MPI_DATA14
K18	PT23C	1	DP1/MPI_PAR1	PT28C	1	DP1/MPI_PAR1
E20	PT23B	1	A21/MPI_BURST	PT27B	1	A21/MPI_BURST
F20	PT23A	1	D15/MPI_DATA15	PT27A	1	D15/MPI_DATA15
C23	B_REFCLKP_L	-		B_REFCLKP_L	-	
D23	B_REFCLKN_L	-		B_REFCLKN_L	-	
B23	VCC12	-		VCC12	-	
H21	B_VDDIB3_L	-		B_VDDIB3_L	-	
F21	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
G21	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D21	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D22	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G22	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
F22	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H22	B_VDDIB2_L	-		B_VDDIB2_L	-	
H24	B_VDDIB1_L	-		B_VDDIB1_L	-	
G23	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
H23	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
A24	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
B24	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-		B_VDDOB1_L	-	
B25	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-		B_VDDOB0_L	-	
A25	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
G25	B_HDINN0_L	-	PCS 361 CH 0 IN N	B_HDINN0_L	-	PCS 361 CH 0 IN N
F25	B_HDINP0_L	-	PCS 361 CH 0 IN P	B_HDINP0_L	-	PCS 361 CH 0 IN P
H25	B_VDDIB0_L	-		B_VDDIB0_L	-	
H26	A_VDDIB3_L	-		A_VDDIB3_L	-	
F26	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
G26	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
D26	A_VDDOB3_L	-		A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
D27	A_VDDOB2_L	-		A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
G27	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
F27	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
H27	A_VDDIB2_L	-		A_VDDIB2_L	-	
F29	A_VDDIB1_L	-		A_VDDIB1_L	-	
G28	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
H28	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A29	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B29	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
D29	A_VDDOB1_L	-		A_VDDOB1_L	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L1	PR31A	2		PR43A	2	
T10	PR30D	2		PR42D	2	
U10	PR30C	2		PR42C	2	
N2	PR30B	2		PR42B	2	
M2	PR30A	2		PR42A	2	
R11	PR29D	2		PR37D	2	
P11	PR29C	2		PR37C	2	
N4	PR29B	2		PR37B	2	
M4	PR29A	2		PR37A	2	
N5	PR27D	2		PR35D	2	
M5	PR27C	2		PR35C	2	
L2	PR27B	2		PR35B	2	
K2	PR27A	2		PR35A	2	
P8	PR26D	2		PR33D	2	
N8	PR26C	2		PR33C	2	
J2	PR26B	2		PR33B	2	
H2	PR26A	2		PR33A	2	
M6	PR25D	2		PR31D	2	
L6	PR25C	2		PR31C	2	
K3	PR25B	2		PR31B	2	
J3	PR25A	2		PR31A	2	
M8	PR23D	2	DIFFR_2	PR29D	2	DIFFR_2
L8	PR23C	2	VREF1_2	PR29C	2	VREF1_2
K4	PR23B	2		PR29B	2	
J4	PR23A	2		PR29A	2	
M7	PR22D	2		PR21D	2	
L7	PR22C	2		PR21C	2	
J5	PR22B	2		PR21B	2	
H5	PR22A	2		PR21A	2	
N9	PR21D	2		PR20D	2	
P9	PR21C	2		PR20C	2	
G3	PR21B	2		PR20B	2	
F3	PR21A	2		PR20A	2	
J6	PR18D	2	VREF2_2	PR18D	2	VREF2_2
H6	PR18C	2		PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
D2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
G4	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
F4	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
J7	PR16D	2		PR16D	2	
H7	PR16C	2		PR16C	2	
G5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
F5	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL11	GND	-		GND	-	
AL17	GND	-		GND	-	
AL21	GND	-		GND	-	
AL27	GND	-		GND	-	
AL5	GND	-		GND	-	
AM14	GND	-		GND	-	
AM18	GND	-		GND	-	
AM24	GND	-		GND	-	
AM30	GND	-		GND	-	
AM8	GND	-		GND	-	
AN1	GND	-		GND	-	
AN34	GND	-		GND	-	
AP2	GND	-		GND	-	
AP33	GND	-		GND	-	
B1	GND	-		GND	-	
B34	GND	-		GND	-	
C11	GND	-		GND	-	
C12	GND	-		GND	-	
C13	GND	-		GND	-	
C14	GND	-		GND	-	
C17	GND	-		GND	-	
C21	GND	-		GND	-	
C22	GND	-		GND	-	
C23	GND	-		GND	-	
C24	GND	-		GND	-	
C26	GND	-		GND	-	
C27	GND	-		GND	-	
C30	GND	-		GND	-	
C31	GND	-		GND	-	
C4	GND	-		GND	-	
C5	GND	-		GND	-	
C8	GND	-		GND	-	
C9	GND	-		GND	-	
D18	GND	-		GND	-	
E32	GND	-		GND	-	
E4	GND	-		GND	-	
F19	GND	-		GND	-	
G16	GND	-		GND	-	
G29	GND	-		GND	-	
G7	GND	-		GND	-	
H3	GND	-		GND	-	
H31	GND	-		GND	-	
J10	GND	-		GND	-	
J15	GND	-		GND	-	
J26	GND	-		GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL4	PR117B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR117A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR116D	3	
AD9	PR116C	3	
AH4	PR116B	3	
AJ4	PR116A	3	
AK5	PR115D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR115C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR115B	3	
AL1	PR115A	3	
AH5	PR112D	3	
AG5	PR112C	3	
AL2	PR112B	3	
AK2	PR112A	3	
AB9	PR109D	3	
AC9	PR109C	3	
AH1	PR109B	3	
AG1	PR109A	3	
AE8	PR107D	3	VREF2_3
AD8	PR107C	3	
AJ3	PR107B	3	
AH3	PR107A	3	
AD7	PR104D	3	
AC7	PR104C	3	
AJ2	PR104B	3	
AH2	PR104A	3	
AF6	PR103D	3	
AF5	PR103C	3	
AF4	PR103B	3	
AE4	PR103A	3	
AD6	PR99D	3	
AC6	PR99C	3	
AG2	PR99B	3	
AF2	PR99A	3	
AC8	PR98D	3	
AB8	PR98C	3	
AK1	PR98B	3	
AJ1	PR98A	3	
AB10	PR96D	3	
AA10	PR96C	3	
AF3	PR96B	3	
AE3	PR96A	3	
AE5	PR94D	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
F6	A_VDDOB0_R	-	
B4	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
F7	A_VDDOB1_R	-	
B5	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
E6	VCC12	-	
A5	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
B6	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
A6	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
C6	VCC12	-	
D4	A_VDDIB1_R	-	
C7	VCC12	-	
D5	A_VDDIB2_R	-	
A7	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
B7	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
E7	VCC12	-	
A8	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
F8	A_VDDOB2_R	-	
B8	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
F9	A_VDDOB3_R	-	
B9	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
E8	VCC12	-	
A9	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
B10	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
A10	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
C10	VCC12	-	
D6	A_VDDIB3_R	-	
G10	VCC12	-	
D7	B_VDDIB0_R	-	
E10	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
F10	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
K10	VCC12	-	
A11	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D10	B_VDDOB0_R	-	
B11	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D11	B_VDDOB1_R	-	
B12	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L10	VCC12	-	
A12	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
F11	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
E11	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
G11	VCC12	-	
D8	B_VDDIB1_R	-	
G12	VCC12	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AH16	VCCIO4	-	
AJ13	VCCIO4	-	
AJ7	VCCIO4	-	
AL14	VCCIO4	-	
AL8	VCCIO4	-	
AM11	VCCIO4	-	
AM17	VCCIO4	-	
AM5	VCCIO4	-	
AE20	VCCIO5	-	
AE23	VCCIO5	-	
AE26	VCCIO5	-	
AH22	VCCIO5	-	
AH28	VCCIO5	-	
AJ19	VCCIO5	-	
AJ25	VCCIO5	-	
AL18	VCCIO5	-	
AL24	VCCIO5	-	
AL30	VCCIO5	-	
AM21	VCCIO5	-	
AM27	VCCIO5	-	
AA31	VCCIO6	-	
AB29	VCCIO6	-	
AC24	VCCIO6	-	
AD32	VCCIO6	-	
AE28	VCCIO6	-	
AG31	VCCIO6	-	
AK32	VCCIO6	-	
T29	VCCIO6	-	
U31	VCCIO6	-	
V32	VCCIO6	-	
W28	VCCIO6	-	
Y26	VCCIO6	-	
E31	VCCIO7	-	
G28	VCCIO7	-	
H32	VCCIO7	-	
K29	VCCIO7	-	
L31	VCCIO7	-	
M25	VCCIO7	-	
N28	VCCIO7	-	
P32	VCCIO7	-	
R25	VCCIO7	-	
J25	VCCIO1	-	
N11	VTT_2	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P38	PL26B	7		PL40B	7	
N35	PL26C	7		PL40C	7	
N36	PL26D	7		PL40D	7	
N39	PL29A	7		PL43A	7	
P39	PL29B	7		PL43B	7	
R34	PL29C	7	VREF1_7	PL43C	7	VREF1_7
T34	PL29D	7	DIFFR_7	PL43D	7	DIFFR_7
L41	PL30A	7		PL44A	7	
M41	PL30B	7		PL44B	7	
W29	PL30C	7		PL44C	7	
Y29	PL30D	7		PL44D	7	
L42	PL31A	7		PL45A	7	
M42	PL31B	7		PL45B	7	
U32	PL31C	7		PL45C	7	
V32	PL31D	7		PL45D	7	
R37	PL33A	7		PL47A	7	
T37	PL33B	7		PL47B	7	
M36	PL33C	7		PL47C	7	
M37	PL33D	7		PL47D	7	
P40	PL34A	7		PL48A	7	
N40	PL34B	7		PL48B	7	
R35	PL34C	7		PL48C	7	
T35	PL34D	7		PL48D	7	
N41	PL35A	7		PL49A	7	
P41	PL35B	7		PL49B	7	
V33	PL35C	7		PL49C	7	
U33	PL35D	7		PL49D	7	
R38	PL37A	7		PL51A	7	
T38	PL37B	7		PL51B	7	
R36	PL37C	7		PL51C	7	
T36	PL37D	7		PL51D	7	
N42	PL38A	7		PL52A	7	
P42	PL38B	7		PL52B	7	
Y31	PL38C	7		PL52C	7	
AA31	PL38D	7		PL52D	7	
U37	PL39A	7		PL53A	7	
V37	PL39B	7		PL53B	7	
U34	PL39C	7		PL53C	7	
V34	PL39D	7		PL53D	7	
U39	PL41A	7		PL55A	7	
T39	PL41B	7		PL55B	7	
V35	PL41C	7		PL55C	7	
W35	PL41D	7		PL55D	7	
R41	PL42A	7		PL56A	7	
T41	PL42B	7		PL56B	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BA19	PB73A	4		PB87A	4	
BA18	PB73B	4		PB87B	4	
AU19	PB73C	4		PB87C	4	
AU18	PB73D	4		PB87D	4	
AV19	PB74A	4	PCLKT4_2	PB89A	4	PCLKT4_2
AV18	PB74B	4	PCLKC4_2	PB89B	4	PCLKC4_2
AN19	PB74C	4	PCLKT4_7	PB89C	4	PCLKT4_7
AP19	PB74D	4	PCLKC4_7	PB89D	4	PCLKC4_7
BB17	PB75A	4	PCLKT4_1	PB90A	4	PCLKT4_1
BB16	PB75B	4	PCLKC4_1	PB90B	4	PCLKC4_1
AT19	PB75C	4	PCLKT4_6	PB90C	4	PCLKT4_6
AT18	PB75D	4	PCLKC4_6	PB90D	4	PCLKC4_6
BA17	PB77A	4	PCLKT4_0	PB91A	4	PCLKT4_0
BA16	PB77B	4	PCLKC4_0	PB91B	4	PCLKC4_0
AR19	PB77C	4	VREF2_4	PB91C	4	VREF2_4
AR18	PB77D	4		PB91D	4	
AY17	PB79A	4	PCLKT4_5	PB93A	4	PCLKT4_5
AY16	PB79B	4	PCLKC4_5	PB93B	4	PCLKC4_5
AN18	PB79C	4		PB93C	4	
AP18	PB79D	4		PB93D	4	
AW17	PB80A	4	PCLKT4_3	PB94A	4	PCLKT4_3
AW16	PB80B	4	PCLKC4_3	PB94B	4	PCLKC4_3
AU17	PB80C	4	PCLKT4_4	PB94C	4	PCLKT4_4
AU16	PB80D	4	PCLKC4_4	PB94D	4	PCLKC4_4
AV17	PB81A	4		PB95A	4	
AV16	PB81B	4		PB95B	4	
AL18	PB81C	4		PB95C	4	
AM18	PB81D	4		PB95D	4	
BB15	PB83A	4		PB97A	4	
BB14	PB83B	4		PB97B	4	
AP17	PB83C	4		PB97C	4	
AN17	PB83D	4		PB97D	4	
BA15	PB84A	4		PB98A	4	
BA14	PB84B	4		PB98B	4	
AT16	PB84C	4		PB98C	4	
AT15	PB84D	4		PB98D	4	
AV15	PB85A	4		PB99A	4	
AV14	PB85B	4		PB99B	4	
AR16	PB85C	4		PB99C	4	
AR15	PB85D	4		PB99D	4	
AY14	PB87A	4		PB101A	4	
AY13	PB87B	4		PB101B	4	
AU15	PB87C	4		PB101C	4	
AU14	PB87D	4		PB101D	4	
BB13	PB88A	4		PB102A	4	

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FCN1152I[1]	-6	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-5FCN1152I[1]	-5	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	115.2
LFSC3GA115E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	115.2
LFSC3GA115E-6FCN1704I[1]	-6	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-5FCN1704I[1]	-5	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	115.2
LFSC3GA115E-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152I[1]	-6	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FCN1152I[1]	-5	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FCN1704I[1]	-6	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FCN1704I[1]	-5	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Date	Version	Section	Change Summary
August 2006 (cont.)	01.3 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Family Timing Adders with ispLEVER 6.0 SP1 results
			Updated PLL Timing Parameters based on PDE testing results
			Removed RDDATA parameter from sysCONFIG readback timing table
		Multiple	Changed TDO/RDDATA to TDO
		Pinout Information	Removed all MPI signals from SC15 256 pin package Dual Function Column
			Added note to SC15, SC25 900 pin package that the package supports a 16 bit MPI
			Added note that pin D3 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note that pin D28 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note to SC25 1020 pin package that the package supports a 16 bit MPI
			Added note to SC80 1152 pin package that the package supports a 32 bit MPI
			Added note to SC80 1704 pin package that the package supports a 32 bit MPI
		Ordering Information	Changed “fcBGA” for the 1020 packages to “ffBGA”
November 2006	01.4	Introduction	LatticeSC Family Selection Guide table – I/O count for SC80 device, 1704 fcBGA package changed to 904/32. I/O count for SC115 device, 1704 fcBGA package changed to 942/32.
		DC and Switching Characteristics	DC Electrical Characteristics table – Updated the initialization and standby supply current values.
			DC Electrical Characteristics table – Updated the sysCONFIG Master Parallel mode RCLK low and RCLK high time specifications.
			DC Electrical Characteristics table – Updated VCCIO values for LVPECL33 I/Os.
		Pin Information	Pin Information Summary table - Changed number of single ended user I/Os from 906 to 904 for 1704 fcBGA.
			Removed the single-ended only output restriction on pins D3 and D28 in an SC15 and SC25 900 pin package.
		Ordering Information	Ordering Information tables - Changed number of I/Os from 906 to 904 for 1704 fcBGA.
			Added ordering part numbers for LatticeSC/SCM 40K and 115K LUT devices.
			Added lead-free ordering part numbers.
		Multiple	Changed number of available SC80 I/O from 906 to 904.
			Changed number of available SC115 I/O from 944 to 942.
January 2007	01.4a	Architecture	Added EBR Asynchronous Reset section.
February 2007	01.4b	Architecture	Updated EBR Asynchronous Reset section.
March 2007	01.5	Architecture	Added EBR asynchronous reset clarification
			Clarified that differential drivers are not supported in banks 1, 4 and 5
		DC and Switching Characteristics	Added clarification for the description of the junction temperature specification in the Absolute Maximum Ratings section.
			Updated Initialization and Standby Current table.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.1 SP1 results.

Date	Version	Section	Change Summary
September 2007	01.7	Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.
November 2007	01.8	Ordering Information	Removed -7 speed grade information for 115K LUT devices in the Ordering Information tables.
January 2008	01.9	Introduction	Corrections/Additions to memory controller list (Tables 1-2).
		Architecture	AIL Overview – Modified power used by AIL block.
			PURESPEED I/O Buffer Banks – Modified VTT termination info. Added info about complimentary drivers for all banks.
			Supported Source Synchronous Interfaces – Modified data for DDRII in Table 2-11.
		DC and Switching Characteristics	Recommended Operating Conditions – Changed footnote 3.
			Initialization and Standby Supply Current – Inserted a paragraph with info regarding the table. Also updated the table.
			Typical Building Block Function Performance – Added VCC=1.2V=1.2V+/-5% above Pin to Pin Performance table.
			LatticeSC External Switching Characteristics – Added VCC=1.2V=1.2V+/-5% above table. Reworded footnote 3.
			LatticeSC Family Timing Adders – Added VCC=1.2V=1.2V+/-5% above table.
			LatticeSC Internal Timing Parameters – Added VCC=1.2V=1.2V+/-5% above table. Reworded footnote 1.
			GSR Timing – Added a new table for Internal System Bus Timing after GSR Timing.
			LatticeSC sysCONFIG Port Timing – Corrected sysCONFIG SPI Port information.
		Pinout Information	Signal Descriptions – Modified info for VTT_x, PROBE_VCC, and PROBE_GND. Modified info for [LOC]_DLL[T,C]_IN[C,D,E,F].
		Supplemental Information	Updated list of technical notes, added reference to LatticeSC/M flexiPCS Data Sheet.
March 2008	02.0	DC and Switching Characteristics	Updated Internal Timing Parameters table.
			Updated Read Mode timing diagram.
			Updated Read Mode with Input Registers Only timing diagram.
June 2008	02.1	—	Data sheet status changed from preliminary to final.
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
		DC and Switching Characteristics	Updated LatticeSC/M External Switching Characteristics table.
			Updated LatticeSC/M Internal Timing Parameters table.
			Removed Read-Before-Write sysMEM EBR mode.
December 2008	02.2	Architecture	Output/Tristate DDR/Shift Register Block Diagram - corrected connection to POS.
		DC and Switching Characteristics	DC and Switching Characteristics table - updated data for $t_{SUI\_PIO.}$
			Added $T_{R,}$ T_F parameter to PURESPEED I/O Differential Electrical Characteristics (LVDS) table.
		Multiple	Removed references to HyperTransport throughout the data sheet.
January 2010	02.3	Introduction	Updated per PCN #01A-10 (ceramic fcBGA conversion to organic fcBGA for the 1152-ball and 1704-ball fcBGA packages) and PCN #02A-10 (1020-ball organic fcBGA conversion to 1020-ball organic fcBGA revision 2 package).
		Ordering Information	