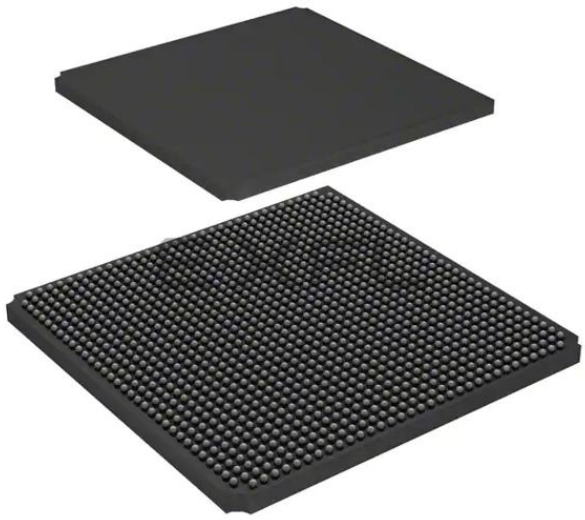
Lattice Semiconductor Corporation - LFSC3GA80E-6FF1152C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-6ff1152c

DLLs and dynamic glitch free clock MUXs which are required in today's high end system designs. High-speed, high-bandwidth I/O make this family ideal for high-throughput systems.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeSC family of FPGA devices. Synthesis library support for LatticeSC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeSC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeSC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Innovative high-performance FPGA architecture, high-speed SERDES with PCS support, sysMEM embedded memory and high performance I/O are combined in the LatticeSC to provide excellent performance for today's leading edge systems designs. Table 1-3 details the performance of several common functions implemented within the LatticeSC.

Table1-3. Speed Performance for Typical Functions[1]

Functions	Performance (MHz)[2]
32-bit Address Decoder	539
64-bit Address Decoder	517
32:1 Multiplexer	779
64-bit Adder (ripple)	353
32x8 Distributed Single Port (SP) RAM	768
64-bit Counter (up or down counter, non-loadable)	369
True Dual-Port 1024x18 bits	372
FIFO Port A: x36 bits, B: x9 bits	375

1. For additional information, see Typical Building BLock Function Performance table in this data sheet.
2. Advance information (-7 speed grade).

LatticeSC/M Family Data Sheet Architecture

December 2008 **Data Sheet DS1004**

Architecture Overview

The LatticeSC architecture contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR). The upper left and upper right corners of the devices contain SERDES blocks and their associated PCS blocks, as show in Figure 2-1.

Top left and top right corner of the device contain blocks of SERDES. Each block of SERDES contains four channels (quad). Each channel contains a single serializer and de-serializer, synchronization and word alignment logic. The SERDES quad connects with the Physical Coding Sub-layer (PCS) blocks that contain logic to simultaneously perform alignment, coding, de-coding and other functions. The SERDES quad block has separate supply, ground and reference voltage pins.

The PICs contain logic to facilitate the conditioning of signals to and from the I/O before they leave or enter the FPGA fabric. The block provides DDR and shift register capabilities that act as a gearbox between high speed I/O and the FPGA fabric. The blocks also contain programmable Adaptive Input Logic that adjusts the delay applied to signals as they enter the device to optimize setup and hold times and ensure robust performance.

sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM, ROM or FIFO. These blocks have dedicated logic to simplify the implementation of FIFOs.

The PFU, PIC and EBR blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. These blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

The corners contain the sysCLOCK Analog Phase Locked Loop (PLL) and Delay Locked Loop (DLL) Blocks. The PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeSC architecture provides eight analog PLLs per device and 12 DLLs. The DLLs provide a simple delay capability and can also be used to calibrate other delays within the device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG™ port which allows for serial or parallel device configuration. The system bus simplifies the connections of the external microprocessor to the device for tasks such as SERDES and PCS configuration or interface to the general FPGA logic. The LatticeSC devices use 1.2V as their core voltage operation with 1.0V operation also possible.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR 16x2 x 4 DPR 16x2 x 2	ROM 16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR 16x4 x 2 DPR 16x4 x 1	ROM 16x2 x 4
LUT 6x2 or MUX 8x1 x 2	2-bit Counter x 4	SPR 16x8 x 1	ROM 16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM 16x8 x1

Routing

There are many resources provided in the LatticeSC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

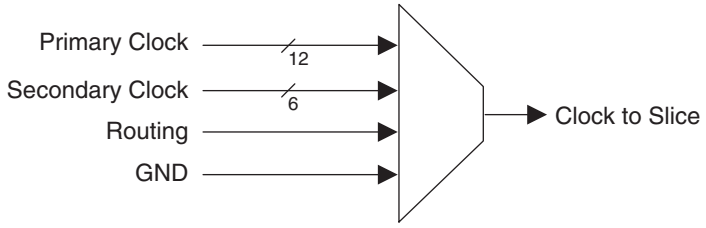
The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU) resources. The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. All connections are buffered to ensure high-speed operation even with long high-fanout connections.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Network

The LatticeSC devices have three distinct clock networks for use in distributing high-performance clocks within the device: primary clocks, secondary clocks and edge clocks. In addition to these dedicated clock networks, users are free to route clocks within the device using the general purpose routing. Figure 2-4 shows the clock resources available to each slice.

Figure 2-4. Slice Clock Selection



Note: GND is available to switch off the network.

Primary Clock Sources

LatticeSC devices have a wide variety of primary clock sources available. Primary clocks sources consists of the following:

- Primary clock input pins
- Edge clock input pins
- Two outputs per DLL

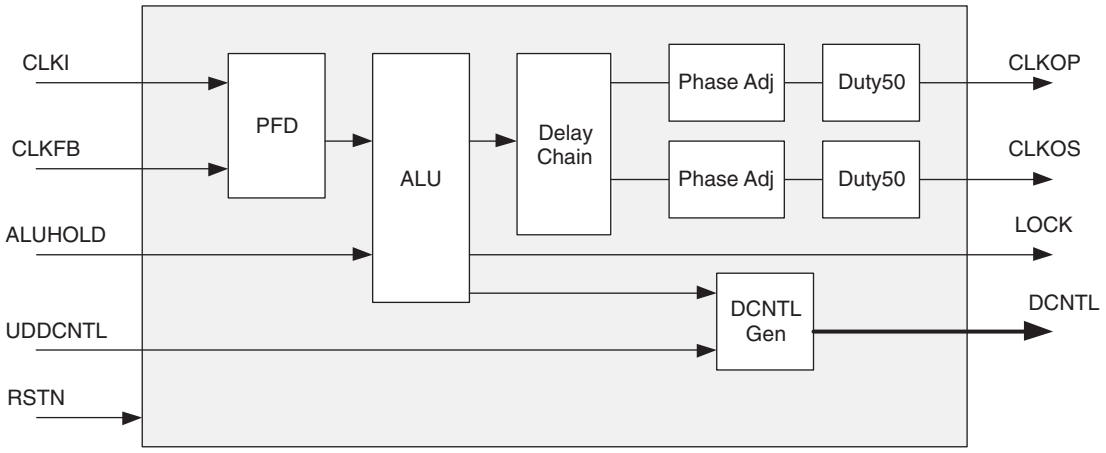
There is a Digital Control (DCNTL) bus available from the DLL block. This Digital Control bus is available to the delay lines in the PIC blocks in the adjacent banks. The UDDCNTL signal allows the user to latch the current value on the digital control bus.

Figure 2-12 shows the DLL block diagram of the DLL inputs and outputs. The output of the phase frequency detector controls an arithmetic logic unit (ALU) to add or subtract one delay tap. The digital output of this ALU is used to control the delay value of the delay chain and this digital code is transmitted via the DCNTL bus.

The sysCLOCK DLL can be configured at power-up, then, if desired, reconfigured dynamically through the Serial Memory Interface bus which interfaces with the on-chip Microprocessor Interface (MPI) bus. In addition, users can drive the SMI interface from routing if desired.

The user can configure the DLL for many common functions such as clock injection match and single delay cell. Lattice provides primitives in its design for time reference delay (DDR memory) and clock injection delay removal.

Figure 2-12. DLL Diagram



PLL/DLL Cascading

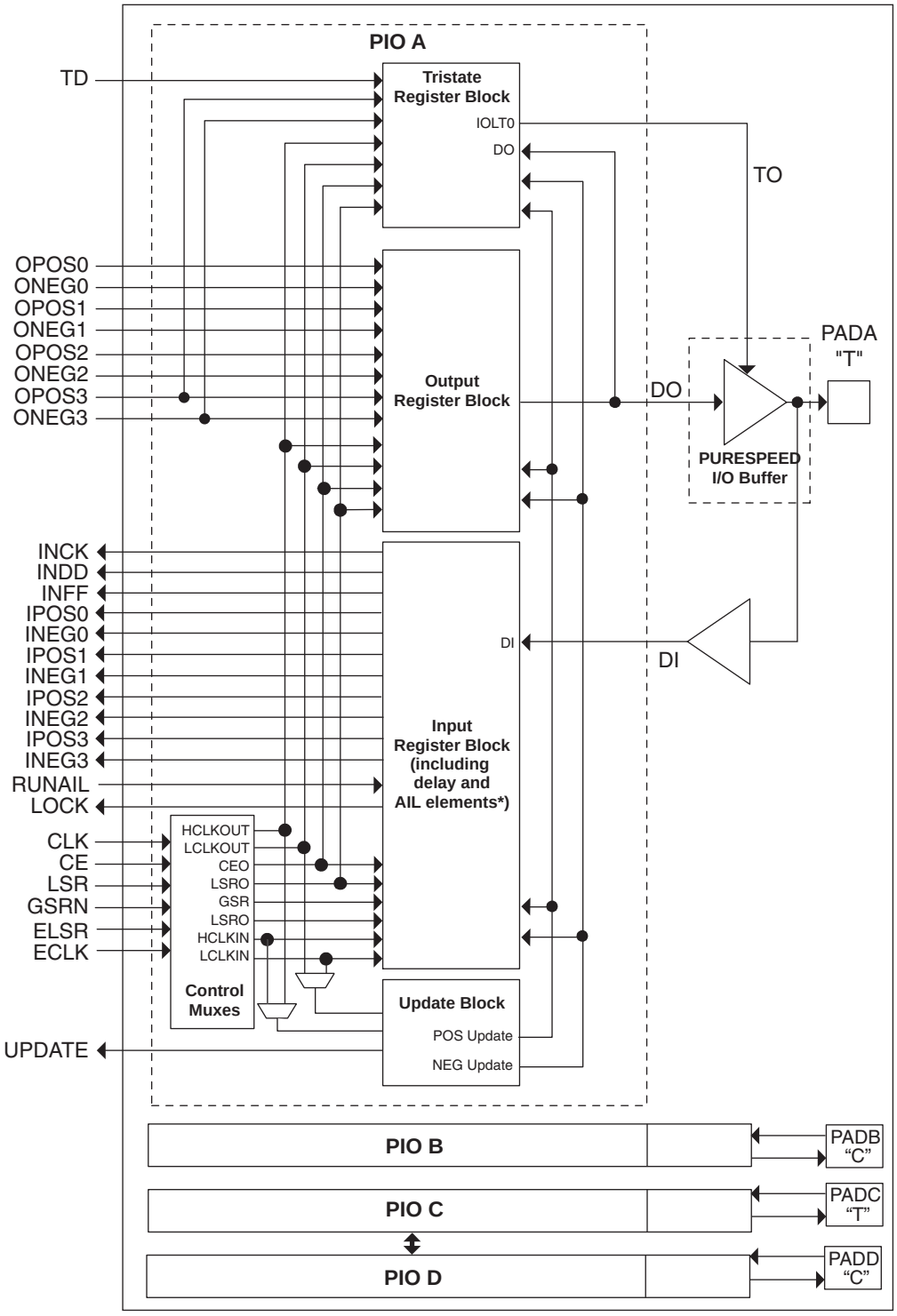
The LatticeSC devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are as follows:

- PLL to PLL
- PLL to DLL
- DLL to DLL
- DLL to PLL

DLLs are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLL and PLLs.

When cascading the DLL to the PLL, the DLL can be used to drive the PLL to create fine phase shifts of an input clock signal. Figure 2-13 shows a shift of all outputs for CLKOP and CLKOS out in time.

Figure 2-17. PIC Diagram



*AIL only on A or C pads located on the left, right and bottom of the device.

The A/B PIOs on the left and the right of the device can be paired to form a differentiated driver. The A/B and C/D PIOs on all sides of the device can be paired to form differential receivers. Either A or C PIOs on all sides except the one on top also provide a connection to an adaptive input logic capability that facilitates the implementation of

3. **Bottom Side (Banks 4 and 5)**
   These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but true HLVDS and RSDS differential drivers are not available. Adaptive input logic is available on PIOs A or C.

Table 2-8 lists the standards supported by each side.

Table 2-8. I/O Standards Supported by Different Banks

Description	Top Side Banks 1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
I/O Buffer Type	Single-ended, Differential Receiver	Single-ended, Differential Receiver and Driver	Single-ended, Differential Receiver	Single-ended, Differential Receiver and Driver
Output Standards Supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II SSTL33_ I, II HSTL15_I, II, III[1], IV[1] HSTL18_I, II,III[1], IV[1] SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL[2], GTL+[2]	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II HSTL15_I,III HSTL18_I,II,III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL[2], GTL+[2]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II SSTL33_ I, II HSTL15_I, II, III[1], IV[1] HSTL18_I, II,III[1], IV[1] SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL[2], GTL+[2]	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II HSTL15_I,III HSTL18_I,II,III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL[2], GTL+[2]
Input Standards Supported	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Clock Inputs	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Differential Output Support via Emulation	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL
AIL Support	No	Yes	Yes	Yes

1. Input only.
2. Input only. Outputs supported by bussing multiple outputs together.

Supported Standards

The LatticeSC PURESPEED I/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 12, 15, 18, 25 and 33 standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, termination resistance, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL, HSTL, GTL (input only), GTL+ (input only), PCI33, PCIX33, PCIX15, AGP-1X33 and AGP-2X33. Differential standards supported include LVDS, RSDS, BLVDS, MLVDS, LVPECL, differential SSTL and differential HSTL. Tables 12 and 13 show the I/O standards (together with their supply and reference voltages) supported by the LatticeSC devices. The tables also provide the available internal termination schemes. For further information on utilizing the PURESPEED I/O buffer to support a variety of standards please see details of additional technical documentation at the end of this data sheet.

- 8-bit SERDES Only
- 10-bit SERDES Only
- SONET (STS-12/STS-48)
- Gigabit Ethernet
- Fibre Channel
- XAUI
- Serial RapidIO
- PCI-Express
- Generic 8b10b

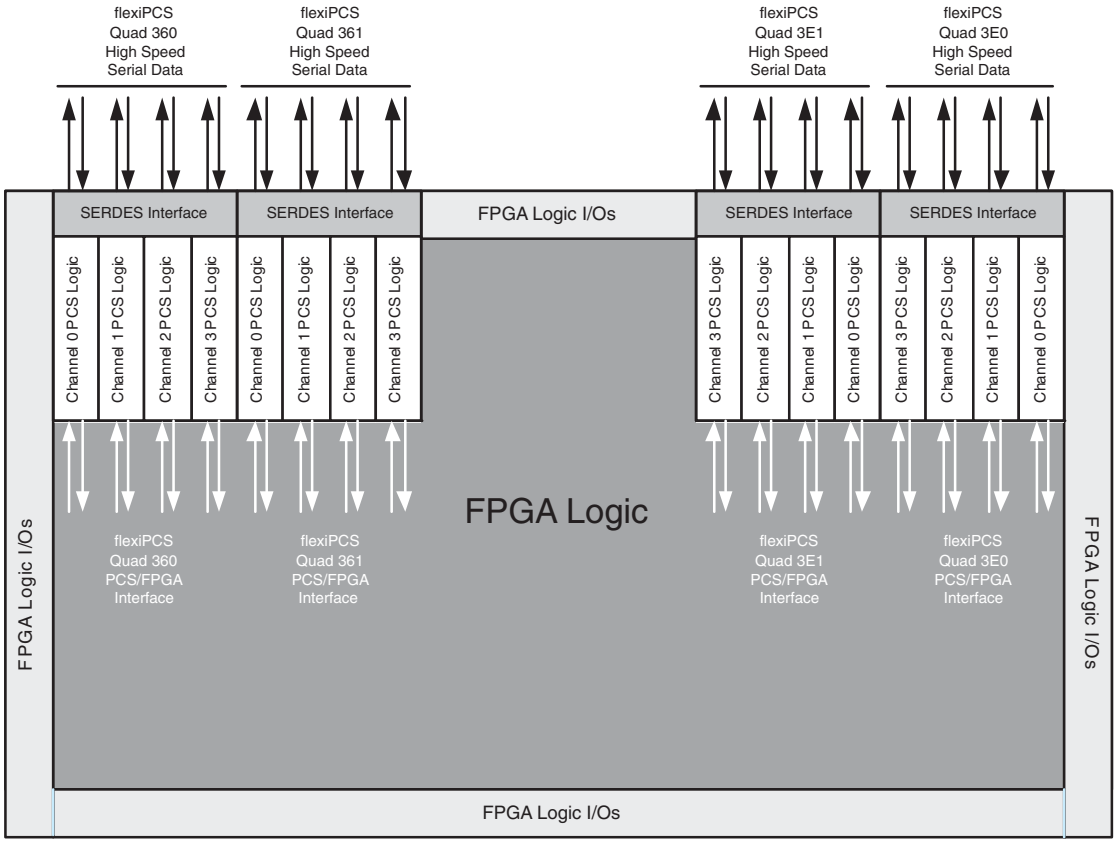
flexiPCS Quad

The flexiPCS logic is arranged in quads containing logic for four independent full-duplex data channels. Each device in the LatticeSC family has up to eight quads of flexiPCS logic. The LatticeSC Family Selection Guide table on the first page of this data sheet contains the number of flexiPCS channels present on the chip. Note that in some packages (particularly lower pin count packages), not all channels from all quads on a given device may be bonded to package pins.

Each quad supports up to four channels of full-duplex data and can be programmed into any one of several protocol based modes. Each quad requires its own reference clock which can be sourced externally or from the FPGA logic. The user can utilize between one and four channels in a quad, depending on the application.

Figure 2-30 shows an example of four flexiPCS quads in a LatticeSC device. Quads are labeled according to the address of their software controlled registers.

Figure 2-30. LatticeSC flexiPCS



Since each quad has its own reference clock, different quads can support different standards on the same chip. This feature makes the LatticeSC family of devices ideal for bridging between different standards.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

MLVDS

The LatticeSC devices support the MLVDS standard. This industry standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. MLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-1 is one possible solution for bi-directional multi-point differential signals.

Figure 3-1. MLVDS Multi-Point Output Example

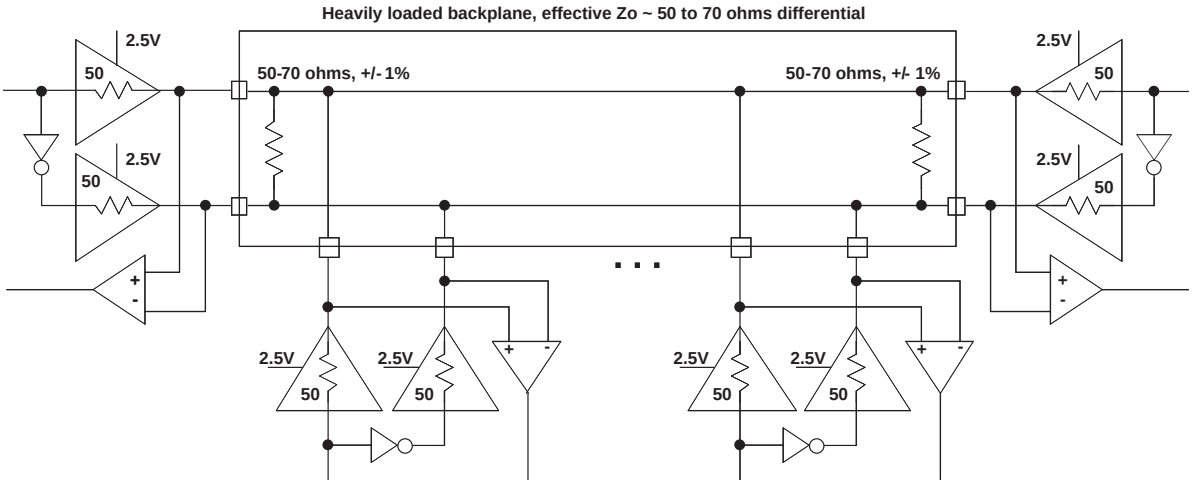


Table 3-1. MLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 50	Zo = 70	
Z_{OUT}	Output impedance	50	50	ohm
R_{TLEFT}	Left end termination	50	70	ohm
R_{TRIGHT}	Right end termination	50	70	ohm
V_{OH}	Output high voltage	1.50	1.575	V
V_{OL}	Output low voltage	1.00	0.925	V
V_{OD}	Output differential voltage	0.50	0.65	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	20.0	18.5	mA

1. For input buffer, see LVDS table.

Pin Information Summary

Pin Type		256 fpBGA	900 fpBGA		1020 fcBGA	
		LFSC/M15	LFSC/M15	LFSC/M25	LFSC/M25	LFSC/M40
Single Ended User I/O		139	300	378	476	562
Differential Pair User I/O		60	141	182	235	277
LVDS Output Pairs		22	44	60	60	78
Configuration	Dedicated	9	11	11	11	11
	Muxes/MPI sysBus	0	55	55	55	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		2	4	4	4	4
VCC		10	46	46	40	40
VCC12		10	35	35	36	36
VCCAUX		10	36	36	32	32
VCCIO	Bank 1	3	18	18	10	10
	Bank 2	2	14	14	8	8
	Bank 3	2	15	15	10	10
	Bank 4	3	15	15	10	10
	Bank 5	3	15	15	10	10
	Bank 6	2	15	15	10	10
	Bank 7	2	16	16	8	8
VTT	Bank 2	0	2	2	2	2
	Bank 3	0	3	3	3	3
	Bank 4	0	3	3	3	3
	Bank 5	0	3	3	3	3
	Bank 6	0	3	3	3	3
	Bank 7	0	2	2	2	2
GND		26	177	177	134	134
NC		0	102	24	92	6
Single Ended User / Differential I/O per Bank	Bank 1	21/8	63/30	63/30	68/32	68/32
	Bank 2	15/7	26/13	30/15	34/17	54/27
	Bank 3	19/8	43/20	62/29	84/42	94/47
	Bank 4	25/11	50/22	66/32	84/41	99/48
	Bank 5	25/11	49/23	65/32	88/44	99/49
	Bank 6	19/8	43/20	62/29	84/42	94/47
	Bank 7	15/7	26/13	30/15	34/17	54/27
LVDS Output Pairs Per Bank	Bank 2	5	7	9	9	15
	Bank 3	6	15	21	21	24
	Bank 6	6	15	21	21	24
	Bank 7	5	7	9	9	15
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		28	60	60	108	108
Total		256	900	900	1020	1152

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B29	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M15 and LatticeSC/M25 in a 900-pin package supports a 16-bit MPI interface.

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P10	GND	-		GND	-	
P13	GND	-		GND	-	
P15	GND	-		GND	-	
P18	GND	-		GND	-	
P20	GND	-		GND	-	
P24	GND	-		GND	-	
R12	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R17	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
R6	GND	-		GND	-	
T15	GND	-		GND	-	
T18	GND	-		GND	-	
T30	GND	-		GND	-	
T4	GND	-		GND	-	
U15	GND	-		GND	-	
U18	GND	-		GND	-	
U29	GND	-		GND	-	
U3	GND	-		GND	-	
V12	GND	-		GND	-	
V14	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V21	GND	-		GND	-	
V27	GND	-		GND	-	
V7	GND	-		GND	-	
W13	GND	-		GND	-	
W15	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W9	GND	-		GND	-	
Y12	GND	-		GND	-	
Y14	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y30	GND	-		GND	-	
Y4	GND	-		GND	-	
N13	VCC	-		VCC	-	
N15	VCC	-		VCC	-	
N16	VCC	-		VCC	-	
N17	VCC	-		VCC	-	
N18	VCC	-		VCC	-	
N20	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD29	PL60D	6		PL84D	6	
AE31	PL61A	6		PL85A	6	
AF31	PL61B	6		PL85B	6	
AF30	PL61C	6		PL85C	6	
AF29	PL61D	6		PL85D	6	
AH33	PL62A	6		PL86A	6	
AJ33	PL62B	6		PL86B	6	
AC28	PL62C	6		PL86C	6	
AD28	PL62D	6		PL86D	6	
AH32	PL65A	6		PL89A	6	
AJ32	PL65B	6		PL89B	6	
AD27	PL65C	6		PL89C	6	
AE27	PL65D	6	VREF2_6	PL89D	6	VREF2_6
AG34	PL66A	6		PL90A	6	
AH34	PL66B	6		PL90B	6	
AC26	PL66C	6		PL90C	6	
AB26	PL66D	6		PL90D	6	
AK33	PL67A	6		PL91A	6	
AL33	PL67B	6		PL91B	6	
AG30	PL67C	6		PL91C	6	
AH30	PL67D	6		PL91D	6	
AL34	PL69A	6		PL93A	6	
AM34	PL69B	6		PL93B	6	
AJ30	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL93C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL93D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL70A	6		PL94A	6	
AH31	PL70B	6		PL94B	6	
AD26	PL70C	6		PL94C	6	
AD25	PL70D	6		PL94D	6	
AL32	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL95A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL95B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL95C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL95D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-		XRES	-	
AF27	TEMP	6		TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AN33	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AH29	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AJ29	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AM32	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AM31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AG27	PB4C	5		PB4C	5	
AG26	PB4D	5		PB4D	5	
AL29	PB5A	5		PB5A	5	
AL28	PB5B	5		PB5B	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ9	PB78C	4		PB117C	4	
AJ8	PB78D	4		PB117D	4	
AP3	PB79A	4		PB119A	4	
AN3	PB79B	4		PB119B	4	
AF10	PB79C	4		PB119C	4	
AE10	PB79D	4		PB119D	4	
AL7	PB81A	4		PB121A	4	
AL6	PB81B	4		PB121B	4	
AK7	PB81C	4		PB121C	4	
AK6	PB81D	4		PB121D	4	
AN5	PB82A	4		PB123A	4	
AN4	PB82B	4		PB123B	4	
AH9	PB82C	4	VREF1_4	PB123C	4	VREF1_4
AH8	PB82D	4		PB123D	4	
AM3	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB124A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB124B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB83C	4		PB124C	4	
AG8	PB83D	4		PB124D	4	
AN2	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB125A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB125B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB125C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB125D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-		PROBE_VCC	-	
AF8	PROBE_GND	-		PROBE_GND	-	
AG7	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR95D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR95C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AL4	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR95B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR95A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR70D	3		PR94D	3	
AD9	PR70C	3		PR94C	3	
AH4	PR70B	3		PR94B	3	
AJ4	PR70A	3		PR94A	3	
AK5	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR93D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR93C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR69B	3		PR93B	3	
AL1	PR69A	3		PR93A	3	
AH5	PR67D	3		PR91D	3	
AG5	PR67C	3		PR91C	3	
AL2	PR67B	3		PR91B	3	
AK2	PR67A	3		PR91A	3	
AB9	PR66D	3		PR90D	3	
AC9	PR66C	3		PR90C	3	
AH1	PR66B	3		PR90B	3	
AG1	PR66A	3		PR90A	3	
AE8	PR65D	3	VREF2_3	PR89D	3	VREF2_3

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C32	VCC12	-		VCC12	-	
E34	NC	-		PL22A	7	
F34	NC	-		PL22B	7	
F33	NC	-		PL24A	7	
G33	NC	-		PL24B	7	
K30	NC	-		PL25A	7	
L30	NC	-		PL25B	7	
G34	NC	-		PL26A	7	
H34	NC	-		PL26B	7	
M32	NC	-		PL39A	7	
N32	NC	-		PL39B	7	
P28	NC	-		PL39C	7	
R28	NC	-		PL39D	7	
J34	NC	-		PL41A	7	
K34	NC	-		PL41B	7	
P30	NC	-		PL41C	7	
R30	NC	-		PL41D	7	
W34	NC	-		PL59A	6	
Y34	NC	-		PL59B	6	
W32	NC	-		PL61A	6	
Y32	NC	-		PL61B	6	
AA34	NC	-		PL64A	6	
AB34	NC	-		PL64B	6	
AC34	NC	-		PL67A	6	
AD34	NC	-		PL67B	6	
Y30	NC	-		PL68A	6	
AA30	NC	-		PL68B	6	
AB33	NC	-		PL69A	6	
AC33	NC	-		PL69B	6	
AC2	NC	-		PR69B	3	
AB2	NC	-		PR69A	3	
AA5	NC	-		PR68B	3	
Y5	NC	-		PR68A	3	
AD1	NC	-		PR67B	3	
AC1	NC	-		PR67A	3	
AB1	NC	-		PR64B	3	
AA1	NC	-		PR64A	3	
Y3	NC	-		PR61B	3	
W3	NC	-		PR61A	3	
Y1	NC	-		PR59B	3	
W1	NC	-		PR59A	3	
R5	NC	-		PR41D	2	
P5	NC	-		PR41C	2	
K1	NC	-		PR41B	2	
J1	NC	-		PR41A	2	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W7	GND	-		GND	-	
AA14	VCC	-		VCC	-	
AA16	VCC	-		VCC	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AB13	VCC	-		VCC	-	
AB22	VCC	-		VCC	-	
N13	VCC	-		VCC	-	
N22	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	
P17	VCC	-		VCC	-	
P18	VCC	-		VCC	-	
P19	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
R15	VCC	-		VCC	-	
R17	VCC	-		VCC	-	
R18	VCC	-		VCC	-	
R20	VCC	-		VCC	-	
T14	VCC	-		VCC	-	
T16	VCC	-		VCC	-	
T19	VCC	-		VCC	-	
T21	VCC	-		VCC	-	
U14	VCC	-		VCC	-	
U15	VCC	-		VCC	-	
U17	VCC	-		VCC	-	
U18	VCC	-		VCC	-	
U20	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V14	VCC	-		VCC	-	
V15	VCC	-		VCC	-	
V17	VCC	-		VCC	-	
V18	VCC	-		VCC	-	
V20	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W14	VCC	-		VCC	-	
W16	VCC	-		VCC	-	
W19	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y15	VCC	-		VCC	-	
Y17	VCC	-		VCC	-	
Y18	VCC	-		VCC	-	
Y20	VCC	-		VCC	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN8	PB123B	4	
AG11	PB123C	4	
AG10	PB123D	4	
AP7	PB125A	4	
AP6	PB125B	4	
AG13	PB125C	4	
AG12	PB125D	4	
AN7	PB127A	4	
AN6	PB127B	4	
AK9	PB127C	4	
AK8	PB127D	4	
AP5	PB129A	4	
AP4	PB129B	4	
AD11	PB129C	4	
AE11	PB129D	4	
AM7	PB131A	4	
AM6	PB131B	4	
AJ9	PB131C	4	
AJ8	PB131D	4	
AP3	PB133A	4	
AN3	PB133B	4	
AF10	PB133C	4	
AE10	PB133D	4	
AL7	PB135A	4	
AL6	PB135B	4	
AK7	PB135C	4	
AK6	PB135D	4	
AN5	PB138A	4	
AN4	PB138B	4	
AH9	PB138C	4	VREF1_4
AH8	PB138D	4	
AM3	PB139A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB139B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB139C	4	
AG8	PB139D	4	
AN2	PB141A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB141B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB141C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB141D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-	
AF8	PROBE_GND	-	
AG7	PR117D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR117C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AD5	PR94C	3	
AE2	PR94B	3	
AD2	PR94A	3	
AC5	PR92D	3	
AB5	PR92C	3	
AF1	PR92B	3	
AE1	PR92A	3	
AA11	PR91D	3	
Y11	PR91C	3	
AC4	PR91B	3	
AB4	PR91A	3	
AA8	PR90D	3	DIFFR_3
AA9	PR90C	3	
AC3	PR90B	3	
AB3	PR90A	3	
AA7	PR79D	3	
Y7	PR79C	3	
AA2	PR79B	3	
Y2	PR79A	3	
AA6	PR77D	3	
Y6	PR77C	3	
Y4	PR77B	3	
W4	PR77A	3	
W11	PR74D	3	
V11	PR74C	3	
W2	PR74B	3	
V2	PR74A	3	
W9	PR71D	3	
V9	PR71C	3	
V1	PR71B	3	
U1	PR71A	3	
W10	PR70D	3	
V10	PR70C	3	
U2	PR70B	3	
T2	PR70A	3	
Y8	PR69D	3	
W8	PR69C	3	VREF1_3
W5	PR69B	3	
V5	PR69A	3	
V7	PR66D	3	PCLKC3_2
U7	PR66C	3	PCLKT3_2
T1	PR66B	3	
R1	PR66A	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
V8	PR65D	3	PCLKC3_3
U8	PR65C	3	PCLKT3_3
U5	PR65B	3	
T5	PR65A	3	
V6	PR64D	3	PCLKC3_1
U6	PR64C	3	PCLKT3_1
T4	PR64B	3	PCLKC3_0
T3	PR64A	3	PCLKT3_0
U9	PR62D	2	PCLKC2_2
T9	PR62C	2	PCLKT2_2
R2	PR62B	2	PCLKC2_0
P2	PR62A	2	PCLKT2_0
T11	PR61D	2	PCLKC2_3
U11	PR61C	2	PCLKT2_3
R4	PR61B	2	PCLKC2_1
R3	PR61A	2	PCLKT2_1
T8	PR60D	2	
R8	PR60C	2	
P1	PR60B	2	
N1	PR60A	2	
R6	PR57D	2	
P6	PR57C	2	
M1	PR57B	2	
L1	PR57A	2	
T10	PR56D	2	
U10	PR56C	2	
N2	PR56B	2	
M2	PR56A	2	
R11	PR51D	2	
P11	PR51C	2	
N4	PR51B	2	
M4	PR51A	2	
N5	PR49D	2	
M5	PR49C	2	
L2	PR49B	2	
K2	PR49A	2	
P8	PR47D	2	
N8	PR47C	2	
J2	PR47B	2	
H2	PR47A	2	
M6	PR45D	2	
L6	PR45C	2	
K3	PR45B	2	

Lead-Free Packaging

Commercial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Date	Version	Section	Change Summary
March 2007 (cont.)	01.5 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Internal Timing Parameters with ispLEVER 6.1 SP1 results.
			Updated t_{FDEL} and t_{CDEL} specifications.
			Updated LatticeSC Family Timing Adders with ispLEVER 6.1 SP1 results.
			Updated PLL specifications to expand frequency range down to 2 MHz and break out jitter for the different ranges.
			Added footnote to sysCLOCK PLL Timing table specifying the conditions for the jitter measurements.
			Added t_{DLL} specification to sysCLOCK DLL Timing table.
			Added footnote to sysCLOCK DLL Timing table specifying the conditions for the jitter measurements.
			Added sysCONFIG Master Parallel Configuration Mode and sysCONFIG SPI Port to LatticeSC sysCONFIG Port Timing table.
		Pin Information	Updated Pin Information Summary with SC40 information.
			Updated LFSC25 Logic Signal Connections: FF1020 with SC40 information.
			Updated LFSC80 Logic Signal Connections: FC1152 with SC40 information.
August 2007	01.6	General	Changed references of "HDC" to "HDC/SI".
			Changed references of "LDCN" to "LDCN/SCS".
			Changed references of "BUSYN/RCLK" to "BUSYN/RCLK/SCK".
			Changed references of "RDCFGN" to "TSALLN".
			Changed references of "TDO/RDDATA" to "TDO".
		Architecture	Updated text in Ripple Mode section.
			Added information to Global Set/Reset.
			Added information for Spread Spectrum Clocking
			Modified information for PLL/DLL Cascading. DLL to PLL is now supported.
			Modified AIL Block text and figure.
			Modified Figure 2-20 DDR/Shift Register Block.
			Added Information to Hot Socketing.
			Added new information for I/O Architecture Rules.
			Added information to SERDES Power Supply Sequencing Requirements.
		DC and Switching Characteristics	Added footnote to Hot Socketing Specifications table.
			Modified Initialization and Standby Supply Current table.
			Modified GSR Timing table.
			Modified sysCLOCK DLL Timing table to include $I_{DUTY.}$
			Deleted Readback Timing information from sysCONFIG Port Timing table.
			Modified data in External Switching Characteristics table.
		Pin Information	Added information to the Signal Descriptions table for HDC/SI, LDCN/SCS.
			Added footnote to Signal Descriptions table.
			Modified Description for signal BUSYN/RCLK/SCK.
			Modified data in Pin Information Summary and device-specific Pinout Information tables.