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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	904
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BBGA, FCBGA
Supplier Device Package	1704-OFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-6ffn1704c

Density Shifting

The LatticeSC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

LatticeSC/M Internal Timing Parameters¹

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Symbol	Description	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
PFU Logic Mode Timing									
t _{LUT4_PFU}	CTOF_DEL	LUT4 delay (A to D inputs to F output)	—	0.045	—	0.050	—	0.054	ns
t _{LUT5_PFU}	MTOOFX_DEL	LUT5 delay (inputs to output)	—	0.152	—	0.172	—	0.192	ns
t _{LSR_PFU}	LSR_DEL	Set/Reset to output (asynchronous)	—	0.378	—	0.426	—	0.474	ns
t _{SUM_PFU}	M_SET	Clock to Mux (M0,M1) input setup time	0.113	—	0.131	—	0.148	—	ns
t _{HM_PFU}	M_HLD	Clock to Mux (M0,M1) input hold time	-0.041	—	-0.046	—	-0.052	—	ns
t _{SUD_PFU}	DIN_SET	Clock to D input setup time	0.072	—	0.083	—	0.094	—	ns
t _{HD_PFU}	DIN_HLD	Clock to D input hold time	-0.028	—	-0.032	—	-0.035	—	ns
t _{CK2Q_PFU}	REG_DEL	Clock to Q delay, D-type register configuration	—	0.224	—	0.252	—	0.279	ns
t _{LE2Q_PFU}	LTCH_DEL	Clock to Q delay latch configuration	—	0.294	—	0.331	—	0.367	ns
t _{LD2Q_PFU}	TLTCH_DEL	D to Q throughput delay when latch is enabled	—	0.300	—	0.338	—	0.376	ns
PFU Memory Mode Timing									
t _{CORAM_PFU}	CLKTOF_DEL	Clock to Output	—	0.575	—	0.649	—	0.724	ns
t _{SUDATA_PFU}	DIN_SET	Data Setup Time	-0.024	—	-0.026	—	-0.027	—	ns
t _{HDATA_PFU}	DIN_HLD	Data Hold Time	0.075	—	0.084	—	0.094	—	ns
t _{SUADDR_PFU}	WAD_SET	Address Setup Time	-0.176	—	-0.196	—	-0.215	—	ns
t _{HADDR_PFU}	WAD_HLD	Address Hold Time	0.110	—	0.124	—	0.138	—	ns
t _{SUWREN_PFU}	WE_SET	Write/Read Enable Setup Time	0.014	—	0.019	—	0.024	—	ns
t _{HWREN_PFU}	WE_HLD	Write/Read Enable Hold Time	0.078	—	0.086	—	0.094	—	ns
PIC Timing									
PIO Input/Output Buffer Timing									
t _{IN_PIO}	IN_DEL	Input Buffer Delay(LVCMOS25)	—	0.578	—	0.661	—	0.744	ns
t _{OUT_PIO}	DOPADI_DEL	Output Buffer Delay(LVCMOS25)	—	2.712	—	3.027	—	3.395	ns
t _{SUI_PIO}	DIN_SET	Input Register Setup Time (Data Before Clock)	0.277	—	0.312	—	0.348	—	ns
t _{HI_PIO}	DIN_HLD	Input Register Hold Time (Data after Clock)	-0.267	—	-0.306	—	-0.345	—	ns
t _{COO_PIO}	CK_DEL	Output Register Clock to Output Delay	—	0.513	—	0.571	—	0.639	ns
t _{SUCE_PIO}	CE_SET	Input Register Clock Enable Setup Time	—	0.000	—	0.000	—	0.000	ns
t _{HCE_PIO}	CE_HLD	Input Register Clock Enable Hold Time	—	0.129	—	0.145	—	0.161	ns
t _{SULSR_PIO}	LSR_SET	Set/Reset Setup Time	0.057	—	0.060	—	0.063	—	ns
t _{HLSR_PIO}	LSR_HLD	Set/Reset Hold Time	-0.151	—	-0.159	—	-0.169	—	ns
t _{LE2Q_PIO}	CK_DEL	Input Register Clock to Q delay latch configuration	—	0.335	—	0.372	—	0.410	ns
t _{LD2Q_PIO}	DIN_DEL	Input Register D to Q throughput delay when latch is enabled	—	0.578	—	0.647	—	0.717	ns

sysCLOCK DLL Timing**Over Recommended Operating Conditions**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		100	—	700	MHz
f_{OUTOP}	Output Clock Frequency (CLKOP)		100	—	700	MHz
f_{OUTOS}	Output Clock Frequency (CLKOS)		25	—	700	MHz
AC Characteristics						
t_{DUTY}	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, 50% duty cycle input clock, duty cycle correction turned off, time reference delay mode)	38	—	62	%
t_{DUTYRD}	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, arbitrary duty cycle input clock, duty cycle correction turned on, time reference delay mode)	45	—	55	%
$t_{DUTYCIR}$	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, arbitrary duty cycle input clock, duty cycle correction turned on, clock injection removal mode)	40	—	60	%
t_{OPJIT}^1	Output Clock Period Jitter		—	—	200	ps
t_{CPJIT}^1	Output Clock Cycle-to-Cycle Jitter		—	—	200	ps
t_{SKEW}	Output Clock to Clock Skew (Between Two Outputs with the Same Phase Setting)		—	—	100	ps
t_{LOCK}	DLL Lock-in Time		8	—	18500	cycles
t_{IDUTY}	Input Clock Duty Cycle	Applies to all operating conditions	35	—	65	%
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 250	ps
t_{HI}	Input Clock High Time	At 80% level	500	—	—	ps
t_{LO}	Input Clock Low Time	At 20% level	500	—	—	ps
t_{RSWD}	Reset Signal Pulse Width		3	—	—	ns
t_{FDEL}	Timeshift Delay Step Size		35	45	80	ps
t_{DLL}	Delay Through the DLL when No Delay Taps are Chosen but Not in Bypass Mode.		—	760	—	ps

1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps.

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PIC row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
VREF1_x, VREF2_x	—	The reference supply pins for I/O bank x. Any I/O pin in a bank can be assigned as a reference supply pin, but software defaults use designated pin.
NC	—	No connect. NC pins should not be connected to any active signals, VCC or GND.
Non-SERDES Power Supplies		
VCCIOx	—	VCCIO - The power supply pins for I/O bank x. Dedicated pins.
VCC12 ¹	—	1.2V supply for configuration logic, PLLs and SERDES Rx, Tx and PLL. All VCC12 pins must be connected. As VCC12 supplies power for analog circuitry, VCC12 should be quiet and isolated from noisy digital board supplies.
VTT_x	—	Termination voltage for bank x. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.
GND	—	GND - Ground. Dedicated pins. All grounds must be electrically connected at the board level.
VCC	—	VCC - The power supply pins for core logic. Dedicated pins (1.2V/1.0V).
VCCAUX	—	VCCAUX - Auxiliary power supply pin - powers all differential and referenced input buffers. Dedicated pins (2.5V).
VCCJ	—	VCCJ - The power supply pin for JTAG Test Access Port.
PROBE_VCC	—	VCC signal - Connected to internal VCC node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
MPI_STRBN	I	Driven active low indicates the start of a transaction on the PowerPC bus. MPI will strobe the address bus at next rising edge of clock.
MPI_ADDR[31:14]	I	Address bus driven by a PowerPC bus master. Only 18-bit width is needed. It has to be the least significant bit of the PowerPC 32-bit address A[31:14].
MPI_DAT[n:0]	I/O	Selectable data bus width from 8, and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
MPI_PAR[m:0]	I/O	Selectable parity bus width from 1, 2, and 3-bit. MPI_DP[0] for MPI_D[7:0], MPI_DP[1] for MPI_D[15:8] and MPI_DP[2] for MPI_D[23:16].
MPI_TA	O	Transfer acknowledge. Driven active low indicates that MPI received the data on the write cycle or returned data on the read cycle.
MPI_TEA	O	Transfer Error Acknowledge. Driven active low indicates that MPI detects a bus error on the internal system bus for current transaction.
MPI_RETRY	O	Active low MPI Retry requests the MPC860 to relinquish the bus and retry the cycle.
Multi-chip Alignment (User I/O if not used.)		
MCA_DONE_OUT	O	Multi-chip alignment done output (to second MCA chip)
MCA_DONE_IN	I	Multi-chip alignment done input (from second MCA chip)
MCA_CLK_P[1:2]_OUT	O	Multi-chip alignment clock [1:2] output (sourced by MCA master chip)
MCA_CLK_P[1:2]_IN	I	Multi-chip alignment clock [1:2] input (from MCA master chip)
TEMP	—	Temperature sensing diode pin. Dedicated pin. Accuracy is typically +/- 10°C.
Miscellaneous Dedicated Pins		
XRES	—	External reference resistor between this pin and ground. The reference resistor is used to calibrate the programmable terminating resistors used in the I/Os. Dedicated pin. Value: 1K ± 1% ohm.
DIFFRx	—	Only used if a differential driver is used in a bank. This DIFFRx must be connected to ground via an external 1K ± 1% ohm resistor for all banks that have a differential driver.
SERDES Block (Dedicated Pins)		
[A:D]_HDINPx_[L/R]	I	High-speed input (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDINNx_[L/R]	I	High-speed input (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTPx_[L/R]	O	High-speed output (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTNx_[L/R]	O	High-speed output (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_REFCLKP_[L/R]	I	Ref clock input (positive), aux channel on left [L] or right [R] side of device.
[A:D]_REFCLKN_[L/R]	I	Ref clock input (negative), aux channel on left [L] or right [R] side of device.

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
J9	VCC	-	
K8	VCC	-	
F6	VCC12	-	
F11	VCC12	-	
L11	VCC12	-	
L6	VCC12	-	
K7	VCC12	-	
K10	VCC12	-	
F10	VCCAUX	-	
F7	VCCAUX	-	
T1	GND	-	
G11	VCCAUX	-	
K11	VCCAUX	-	
L10	VCCAUX	-	
L9	VCCAUX	-	
L7	VCCAUX	-	
L8	VCCAUX	-	
T16	GND	-	
G6	VCCAUX	-	
K6	VCCAUX	-	
B13	VCCIO1	-	
D11	VCCIO1	-	
D14	VCCIO1	-	
F12	VCCIO2	-	
G15	VCCIO2	-	
K14	VCCIO3	-	
N15	VCCIO3	-	
M11	VCCIO4	-	
P13	VCCIO4	-	
R10	VCCIO4	-	
N6	VCCIO5	-	
P7	VCCIO5	-	
R4	VCCIO5	-	
K2	VCCIO6	-	
N3	VCCIO6	-	
F4	VCCIO7	-	
G3	VCCIO7	-	
D4	VCC12	-	
D7	VCC12	-	
D5	VCC12	-	
D6	VCC12	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M15 in a 256-pin package does not support an MPI interface.

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB47C	4	PCLKT4_6	PB54C	4	PCLKT4_6
AH10	PB47D	4	PCLKC4_6	PB54D	4	PCLKC4_6
AK12	PB49A	4	PCLKT4_0	PB55A	4	PCLKT4_0
AJ12	PB49B	4	PCLKC4_0	PB55B	4	PCLKC4_0
AF14	PB49C	4	VREF2_4	PB55C	4	VREF2_4
AE14	PB49D	4		PB55D	4	
AL11	PB51A	4	PCLKT4_5	PB57A	4	PCLKT4_5
AL10	PB51B	4	PCLKC4_5	PB57B	4	PCLKC4_5
AH9	PB51C	4		PB57C	4	
AH8	PB51D	4		PB57D	4	
AK11	PB52A	4	PCLKT4_3	PB58A	4	PCLKT4_3
AJ11	PB52B	4	PCLKC4_3	PB58B	4	PCLKC4_3
AH7	PB52C	4	PCLKT4_4	PB58C	4	PCLKT4_4
AH6	PB52D	4	PCLKC4_4	PB58D	4	PCLKC4_4
AK8	PB53A	4		PB67A	4	
AJ8	PB53B	4		PB67B	4	
AF11	PB53C	4		PB67C	4	
AD12	PB55A	4		PB69A	4	
AE12	PB55B	4		PB69B	4	
AM6	PB56A	4		PB70A	4	
AM5	PB56B	4		PB70B	4	
AC12	PB56C	4		PB70C	4	
AL6	PB57A	4		PB73A	4	
AL5	PB57B	4		PB73B	4	
AG7	PB59A	4		PB74A	4	
AG8	PB59B	4		PB74B	4	
AK6	PB60A	4		PB75A	4	
AJ6	PB60B	4		PB75B	4	
AF10	PB60C	4		PB75C	4	
AE11	PB60D	4		PB75D	4	
AM4	PB61A	4		PB77A	4	
AM3	PB61B	4		PB77B	4	
AH5	PB63A	4		PB78A	4	
AH4	PB63B	4		PB78B	4	
AK5	PB64A	4		PB79A	4	
AJ5	PB64B	4		PB79B	4	
AF8	PB64C	4		PB79C	4	
AF7	PB64D	4		PB79D	4	
AL4	PB65A	4		PB81A	4	
AL3	PB65B	4		PB81B	4	
AG5	PB65C	4		PB81C	4	
AF6	PB65D	4		PB81D	4	
AK3	PB67A	4		PB82A	4	
AJ3	PB67B	4		PB82B	4	
AE10	PB67C	4	VREF1_4	PB82C	4	VREF1_4
AD10	PB67D	4		PB82D	4	
AL2	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AK2	PB68B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AE9	PB68C	4		PB83C	4	
AE8	PB68D	4		PB83D	4	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
V25	PL44C	6		PL56C	6	
W25	PL44D	6		PL56D	6	
U34	PL45A	6		PL57A	6	
V34	PL45B	6		PL57B	6	
V26	PL45C	6		PL57C	6	
W26	PL45D	6		PL57D	6	
V33	PL47A	6		PL60A	6	
W33	PL47B	6		PL60B	6	
V24	PL47C	6		PL60C	6	
W24	PL47D	6		PL60D	6	
W31	PL48A	6		PL63A	6	
Y31	PL48B	6		PL63B	6	
Y29	PL48C	6		PL63C	6	
AA29	PL48D	6		PL63D	6	
Y33	PL49A	6		PL65A	6	
AA33	PL49B	6		PL65B	6	
Y28	PL49C	6		PL65C	6	
AA28	PL49D	6		PL65D	6	
AB32	PL51A	6		PL76A	6	
AC32	PL51B	6		PL76B	6	
AA26	PL51C	6		PL76C	6	
AA27	PL51D	6	DIFFR_6	PL76D	6	DIFFR_6
AB31	PL52A	6		PL77A	6	
AC31	PL52B	6		PL77B	6	
Y24	PL52C	6		PL77C	6	
AA24	PL52D	6		PL77D	6	
AE34	PL53A	6		PL78A	6	
AF34	PL53B	6		PL78B	6	
AB30	PL53C	6		PL78C	6	
AC30	PL53D	6		PL78D	6	
AD33	PL56A	6		PL80A	6	
AE33	PL56B	6		PL80B	6	
AD30	PL56C	6		PL80C	6	
AE30	PL56D	6		PL80D	6	
AE32	PL57A	6		PL81A	6	
AF32	PL57B	6		PL81B	6	
AA25	PL57C	6		PL81C	6	
AB25	PL57D	6		PL81D	6	
AJ34	PL58A	6		PL82A	6	
AK34	PL58B	6		PL82B	6	
AB27	PL58C	6		PL82C	6	
AC27	PL58D	6		PL82D	6	
AF33	PL60A	6		PL84A	6	
AG33	PL60B	6		PL84B	6	
AC29	PL60C	6		PL84C	6	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD8	PR65C	3		PR89C	3	
AJ3	PR65B	3		PR89B	3	
AH3	PR65A	3		PR89A	3	
AD7	PR62D	3		PR86D	3	
AC7	PR62C	3		PR86C	3	
AJ2	PR62B	3		PR86B	3	
AH2	PR62A	3		PR86A	3	
AF6	PR61D	3		PR85D	3	
AF5	PR61C	3		PR85C	3	
AF4	PR61B	3		PR85B	3	
AE4	PR61A	3		PR85A	3	
AD6	PR60D	3		PR84D	3	
AC6	PR60C	3		PR84C	3	
AG2	PR60B	3		PR84B	3	
AF2	PR60A	3		PR84A	3	
AC8	PR58D	3		PR82D	3	
AB8	PR58C	3		PR82C	3	
AK1	PR58B	3		PR82B	3	
AJ1	PR58A	3		PR82A	3	
AB10	PR57D	3		PR81D	3	
AA10	PR57C	3		PR81C	3	
AF3	PR57B	3		PR81B	3	
AE3	PR57A	3		PR81A	3	
AE5	PR56D	3		PR80D	3	
AD5	PR56C	3		PR80C	3	
AE2	PR56B	3		PR80B	3	
AD2	PR56A	3		PR80A	3	
AC5	PR53D	3		PR78D	3	
AB5	PR53C	3		PR78C	3	
AF1	PR53B	3		PR78B	3	
AE1	PR53A	3		PR78A	3	
AA11	PR52D	3		PR77D	3	
Y11	PR52C	3		PR77C	3	
AC4	PR52B	3		PR77B	3	
AB4	PR52A	3		PR77A	3	
AA8	PR51D	3	DIFFR_3	PR76D	3	DIFFR_3
AA9	PR51C	3		PR76C	3	
AC3	PR51B	3		PR76B	3	
AB3	PR51A	3		PR76A	3	
AA7	PR49D	3		PR65D	3	
Y7	PR49C	3		PR65C	3	
AA2	PR49B	3		PR65B	3	
Y2	PR49A	3		PR65A	3	
AA6	PR48D	3		PR63D	3	
Y6	PR48C	3		PR63C	3	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W7	GND	-		GND	-	
AA14	VCC	-		VCC	-	
AA16	VCC	-		VCC	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AB13	VCC	-		VCC	-	
AB22	VCC	-		VCC	-	
N13	VCC	-		VCC	-	
N22	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	
P17	VCC	-		VCC	-	
P18	VCC	-		VCC	-	
P19	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
R15	VCC	-		VCC	-	
R17	VCC	-		VCC	-	
R18	VCC	-		VCC	-	
R20	VCC	-		VCC	-	
T14	VCC	-		VCC	-	
T16	VCC	-		VCC	-	
T19	VCC	-		VCC	-	
T21	VCC	-		VCC	-	
U14	VCC	-		VCC	-	
U15	VCC	-		VCC	-	
U17	VCC	-		VCC	-	
U18	VCC	-		VCC	-	
U20	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V14	VCC	-		VCC	-	
V15	VCC	-		VCC	-	
V17	VCC	-		VCC	-	
V18	VCC	-		VCC	-	
V20	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W14	VCC	-		VCC	-	
W16	VCC	-		VCC	-	
W19	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y15	VCC	-		VCC	-	
Y17	VCC	-		VCC	-	
Y18	VCC	-		VCC	-	
Y20	VCC	-		VCC	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J3	PR45A	2	
M8	PR43D	2	DIFFR_2
L8	PR43C	2	VREF1_2
K4	PR43B	2	
J4	PR43A	2	
M7	PR26D	2	
L7	PR26C	2	
J5	PR26B	2	
H5	PR26A	2	
N9	PR19D	2	
P9	PR19C	2	
G3	PR19B	2	
F3	PR19A	2	
J6	PR18D	2	VREF2_2
H6	PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
D2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
G4	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
F4	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
J7	PR15D	2	
H7	PR15C	2	
G5	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
F5	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
C2	VCCJ	-	
M9	TDO	-	TDO
L9	TMS	-	
D1	TCK	-	
C1	TDI	-	
J8	PROGRAMN	1	
K8	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
B2	CCLK	1	
H9	RESP_URC	-	
H10	VCC12	-	
H8	A_REFCLKN_R	-	
G8	A_REFCLKP_R	-	
C3	VCC12	-	
D3	A_VDDIB0_R	-	
A3	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B3	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E5	VCC12	-	
A4	A_HDOUPT0_R	-	PCS 3E0 CH 0 OUT P

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J17	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT81B	1	MCA_CLK_P1_OUT
E16	PT81A	1	MCA_CLK_P1_IN
H15	PT78D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT78C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT78B	1	MCA_CLK_P2_OUT
C16	PT78A	1	MCA_CLK_P2_IN
L17	PT75D	1	MCA_DONE_OUT
K17	PT75C	1	BUSYN/RCLK/SCK
E17	PT75B	1	DP0/MPI_PAR0
F17	PT75A	1	MPI_TA
G17	PT73D	1	D23/MPI_DATA23
H17	PT73C	1	DP2/MPI_PAR2
A17	PT73B	1	PCLKC1_0
B17	PT73A	1	PCLKT1_0/MPI_CLK
G18	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT71C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT71B	1	MPI_RETRY
F18	PT71A	1	A0/MPI_ADDR14
J18	PT69D	1	A1/MPI_ADDR15
J19	PT69C	1	A2/MPI_ADDR16
C20	PT69B	1	A3/MPI_ADDR17
C19	PT69A	1	A4/MPI_ADDR18
K18	PT66D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT66C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT66B	1	A5/MPI_ADDR19
E19	PT66A	1	A6/MPI_ADDR20
H19	PT63D	1	D27/MPI_DATA27
H20	PT63C	1	VREF1_1
A18	PT63B	1	A7/MPI_ADDR21
B18	PT63A	1	A8/MPI_ADDR22
H21	PT61D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT61C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT61B	1	A9/MPI_ADDR23
B19	PT61A	1	A10/MPI_ADDR24
H22	PT58D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT58C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT58B	1	A11/MPI_ADDR25
G20	PT58A	1	A12/MPI_ADDR26
K21	PT57D	1	D11/MPI_DATA11
K22	PT57C	1	D12/MPI_DATA12
A20	PT57B	1	A13/MPI_ADDR27
B20	PT57A	1	A14/MPI_ADDR28

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
H34	PL40B	7	
M32	PL53A	7	
N32	PL53B	7	
P28	PL53C	7	
R28	PL53D	7	
J34	PL55A	7	
K34	PL55B	7	
P30	PL55C	7	
R30	PL55D	7	
W34	PL73A	6	
Y34	PL73B	6	
W32	PL75A	6	
Y32	PL75B	6	
AA34	PL78A	6	
AB34	PL78B	6	
AC34	PL81A	6	
AD34	PL81B	6	
Y30	PL82A	6	
AA30	PL82B	6	
AB33	PL83A	6	
AC33	PL83B	6	
AC2	PR83B	3	
AB2	PR83A	3	
AA5	PR82B	3	
Y5	PR82A	3	
AD1	PR81B	3	
AC1	PR81A	3	
AB1	PR78B	3	
AA1	PR78A	3	
Y3	PR75B	3	
W3	PR75A	3	
Y1	PR73B	3	
W1	PR73A	3	
R5	PR55D	2	
P5	PR55C	2	
K1	PR55B	2	
J1	PR55A	2	
R7	PR53D	2	
P7	PR53C	2	
N3	PR53B	2	
M3	PR53A	2	
H1	PR40B	2	
G1	PR40A	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL23	PB56D	5		PB58D	5	
AW24	PB57A	5		PB61A	5	
AW23	PB57B	5		PB61B	5	
AN23	PB57C	5		PB61C	5	
AP23	PB57D	5		PB61D	5	
AY23	PB59A	5		PB63A	5	
AY24	PB59B	5		PB63B	5	
AU23	PB59C	5		PB63C	5	
AU22	PB59D	5		PB63D	5	
AV23	PB60A	5		PB66A	5	
AV22	PB60B	5		PB66B	5	
AM22	PB60C	5		PB66C	5	
AL22	PB60D	5		PB66D	5	
BA23	PB61A	5		PB69A	5	
BA22	PB61B	5		PB69B	5	
AN22	PB61C	5		PB69C	5	
AP22	PB61D	5		PB69D	5	
BB23	PB63A	5		PB71A	5	
BB22	PB63B	5		PB71B	5	
AT22	PB63C	5		PB71C	5	
AR22	PB63D	5		PB71D	5	
BB21	PB65A	4		PB73A	4	
BB20	PB65B	4		PB73B	4	
AR21	PB65C	4		PB73C	4	
AT21	PB65D	4		PB73D	4	
BA21	PB66A	4		PB75A	4	
BA20	PB66B	4		PB75B	4	
AP21	PB66C	4		PB75C	4	
AN21	PB66D	4		PB75D	4	
AV21	PB67A	4		PB78A	4	
AV20	PB67B	4		PB78B	4	
AM21	PB67C	4		PB78C	4	
AL21	PB67D	4		PB78D	4	
AY20	PB69A	4		PB81A	4	
AY19	PB69B	4		PB81B	4	
AU21	PB69C	4		PB81C	4	
AU20	PB69D	4		PB81D	4	
AW20	PB70A	4		PB83A	4	
AW19	PB70B	4		PB83B	4	
AP20	PB70C	4		PB83C	4	
AN20	PB70D	4		PB83D	4	
BB19	PB71A	4		PB86A	4	
BB18	PB71B	4		PB86B	4	
AM20	PB71C	4		PB86C	4	
AL20	PB71D	4		PB86D	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K14	VCC12	-		VCC12	-	
H11	B_VDDIB2_R	-		B_VDDIB2_R	-	
D8	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
E8	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
G5	VCC12	-		VCC12	-	
B9	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
L12	B_VDDOB2_R	-		B_VDDOB2_R	-	
A9	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
C5	B_VDDOB3_R	-		B_VDDOB3_R	-	
A10	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
H5	VCC12	-		VCC12	-	
B10	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
E9	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
D9	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
J13	VCC12	-		VCC12	-	
H12	B_VDDIB3_R	-		B_VDDIB3_R	-	
J12	VCC12	-		VCC12	-	
M14	B_REFCLKN_R	-		B_REFCLKN_R	-	
L14	B_REFCLKP_R	-		B_REFCLKP_R	-	
J14	VCC12	-		VCC12	-	
G12	C_VDDIB0_R	-		C_VDDIB0_R	-	
D10	C_HDINP0_R	-	PCS 3E2 CH 0 IN P	C_HDINP0_R	-	PCS 3E2 CH 0 IN P
E10	C_HDINN0_R	-	PCS 3E2 CH 0 IN N	C_HDINN0_R	-	PCS 3E2 CH 0 IN N
H6	VCC12	-		VCC12	-	
B11	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P
M12	C_VDDOB0_R	-		C_VDDOB0_R	-	
A11	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N
L11	C_VDDOB1_R	-		C_VDDOB1_R	-	
A12	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N
K11	VCC12	-		VCC12	-	
B12	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P
E11	C_HDINN1_R	-	PCS 3E2 CH 1 IN N	C_HDINN1_R	-	PCS 3E2 CH 1 IN N
D11	C_HDINP1_R	-	PCS 3E2 CH 1 IN P	C_HDINP1_R	-	PCS 3E2 CH 1 IN P
H13	VCC12	-		VCC12	-	
C6	C_VDDIB1_R	-		C_VDDIB1_R	-	
H15	VCC12	-		VCC12	-	
G13	C_VDDIB2_R	-		C_VDDIB2_R	-	
D12	C_HDINP2_R	-	PCS 3E2 CH 2 IN P	C_HDINP2_R	-	PCS 3E2 CH 2 IN P
E12	C_HDINN2_R	-	PCS 3E2 CH 2 IN N	C_HDINN2_R	-	PCS 3E2 CH 2 IN N
J9	VCC12	-		VCC12	-	
B13	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P
K10	C_VDDOB2_R	-		C_VDDOB2_R	-	
A13	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N
J10	C_VDDOB3_R	-		C_VDDOB3_R	-	
A14	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H18	PT77C	1	LDCN/SCS	PT93C	1	LDCN/SCS
F18	PT77B	1	D8/MPI_DATA8	PT93B	1	D8/MPI_DATA8
E18	PT77A	1	CS1/MPI_CS1	PT93A	1	CS1/MPI_CS1
H19	PT75D	1	D9/MPI_DATA9	PT90D	1	D9/MPI_DATA9
G19	PT75C	1	D10/MPI_DATA10	PT90C	1	D10/MPI_DATA10
D19	PT75B	1	CS0N/MPI_CS0N	PT90B	1	CS0N/MPI_CS0N
D18	PT75A	1	RDN/MPI_STRB_N	PT90A	1	RDN/MPI_STRB_N
J20	PT74D	1	WRN/MPI_WR_N	PT89D	1	WRN/MPI_WR_N
K20	PT74C	1	D7/MPI_DATA7	PT89C	1	D7/MPI_DATA7
E19	PT74B	1	D6/MPI_DATA6	PT89B	1	D6/MPI_DATA6
F19	PT74A	1	D5/MPI_DATA5	PT89A	1	D5/MPI_DATA5
K18	PT73D	1	D4/MPI_DATA4	PT87D	1	D4/MPI_DATA4
J18	PT73C	1	D3/MPI_DATA3	PT87C	1	D3/MPI_DATA3
A19	PT73B	1	D2/MPI_DATA2	PT87B	1	D2/MPI_DATA2
B19	PT73A	1	D1/MPI_DATA1	PT87A	1	D1/MPI_DATA1
H17	PT71D	1	D16/PCLKC1_3/MPI_DATA16	PT86D	1	D16/PCLKC1_3/MPI_DATA16
J17	PT71C	1	D17/PCLKT1_3/MPI_DATA17	PT86C	1	D17/PCLKT1_3/MPI_DATA17
B20	PT71B	1	D0/MPI_DATA0	PT86B	1	D0/MPI_DATA0
C20	PT71A	1	QOUT/CEON	PT86A	1	QOUT/CEON
M20	PT70D	1	VREF2_1	PT83D	1	VREF2_1
L20	PT70C	1	D18/MPI_DATA18	PT83C	1	D18/MPI_DATA18
F20	PT70B	1	DOUT	PT83B	1	DOUT
G20	PT70A	1	MCA_DONE_IN	PT83A	1	MCA_DONE_IN
K19	PT69D	1	D19/PCLKC1_2/MPI_DATA19	PT81D	1	D19/PCLKC1_2/MPI_DATA19
J19	PT69C	1	D20/PCLKT1_2/MPI_DATA20	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D20	PT69B	1	MCA_CLK_P1_OUT	PT81B	1	MCA_CLK_P1_OUT
E20	PT69A	1	MCA_CLK_P1_IN	PT81A	1	MCA_CLK_P1_IN
H21	PT67D	1	D21/PCLKC1_1/MPI_DATA21	PT78D	1	D21/PCLKC1_1/MPI_DATA21
G21	PT67C	1	D22/PCLKT1_1/MPI_DATA22	PT78C	1	D22/PCLKT1_1/MPI_DATA22
B21	PT67B	1	MCA_CLK_P2_OUT	PT78B	1	MCA_CLK_P2_OUT
C21	PT67A	1	MCA_CLK_P2_IN	PT78A	1	MCA_CLK_P2_IN
M21	PT66D	1	MCA_DONE_OUT	PT75D	1	MCA_DONE_OUT
L21	PT66C	1	BUSYN/RCLK/SCK	PT75C	1	BUSYN/RCLK/SCK
A21	PT66B	1	DP0/MPI_PAR0	PT75B	1	DP0/MPI_PAR0
A20	PT66A	1	MPI_TA	PT75A	1	MPI_TA
J21	PT65D	1	D23/MPI_DATA23	PT73D	1	D23/MPI_DATA23
K21	PT65C	1	DP2/MPI_PAR2	PT73C	1	DP2/MPI_PAR2
E21	PT65B	1	PCLKC1_0	PT73B	1	PCLKC1_0
F21	PT65A	1	PCLKT1_0/MPI_CLK	PT73A	1	PCLKT1_0/MPI_CLK
G22	PT63D	1	DP3/PCLKC1_4/MPI_PAR3	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H22	PT63C	1	D24/PCLKT1_4/MPI_DATA24	PT71C	1	D24/PCLKT1_4/MPI_DATA24
A23	PT63B	1	MPI_RETRY	PT71B	1	MPI_RETRY
A22	PT63A	1	A0/MPI_ADDR14	PT71A	1	A0/MPI_ADDR14
L22	PT61D	1	A1/MPI_ADDR15	PT69D	1	A1/MPI_ADDR15
M22	PT61C	1	A2/MPI_ADDR16	PT69C	1	A2/MPI_ADDR16

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH27	VCCAUX	-		VCCAUX	-	
AH29	VCCAUX	-		VCCAUX	-	
AJ14	VCCAUX	-		VCCAUX	-	
AJ15	VCCAUX	-		VCCAUX	-	
AJ28	VCCAUX	-		VCCAUX	-	
AJ29	VCCAUX	-		VCCAUX	-	
P14	VCCAUX	-		VCCAUX	-	
P15	VCCAUX	-		VCCAUX	-	
P28	VCCAUX	-		VCCAUX	-	
P29	VCCAUX	-		VCCAUX	-	
R14	VCCAUX	-		VCCAUX	-	
R16	VCCAUX	-		VCCAUX	-	
R17	VCCAUX	-		VCCAUX	-	
R18	VCCAUX	-		VCCAUX	-	
R19	VCCAUX	-		VCCAUX	-	
R20	VCCAUX	-		VCCAUX	-	
R23	VCCAUX	-		VCCAUX	-	
R24	VCCAUX	-		VCCAUX	-	
R25	VCCAUX	-		VCCAUX	-	
R26	VCCAUX	-		VCCAUX	-	
R27	VCCAUX	-		VCCAUX	-	
R29	VCCAUX	-		VCCAUX	-	
T15	VCCAUX	-		VCCAUX	-	
T28	VCCAUX	-		VCCAUX	-	
U15	VCCAUX	-		VCCAUX	-	
U28	VCCAUX	-		VCCAUX	-	
V15	VCCAUX	-		VCCAUX	-	
V28	VCCAUX	-		VCCAUX	-	
W15	VCCAUX	-		VCCAUX	-	
W28	VCCAUX	-		VCCAUX	-	
Y15	VCCAUX	-		VCCAUX	-	
Y28	VCCAUX	-		VCCAUX	-	
F3	VCCIO1	-		VCCIO1	-	
F39	VCCIO1	-		VCCIO1	-	
G35	VCCIO1	-		VCCIO1	-	
G8	VCCIO1	-		VCCIO1	-	
L19	VCCIO1	-		VCCIO1	-	
L24	VCCIO1	-		VCCIO1	-	
M16	VCCIO1	-		VCCIO1	-	
M27	VCCIO1	-		VCCIO1	-	
N11	VCCIO1	-		VCCIO1	-	
N32	VCCIO1	-		VCCIO1	-	
AA4	VCCIO2	-		VCCIO2	-	
H7	VCCIO2	-		VCCIO2	-	
J4	VCCIO2	-		VCCIO2	-	

Conventional Packaging**Commercial**

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7F256C	-7	fpBGA	256	COM	15.2
LFSC3GA15E-6F256C	-6	fpBGA	256	COM	15.2
LFSC3GA15E-5F256C	-5	fpBGA	256	COM	15.2
LFSC3GA15E-7F900C	-7	fpBGA	900	COM	15.2
LFSC3GA15E-6F900C	-6	fpBGA	900	COM	15.2
LFSC3GA15E-5F900C	-5	fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7F256C	-7	fpBGA	256	COM	15.2
LFSCM3GA15EP1-6F256C	-6	fpBGA	256	COM	15.2
LFSCM3GA15EP1-5F256C	-5	fpBGA	256	COM	15.2
LFSCM3GA15EP1-7F900C	-7	fpBGA	900	COM	15.2
LFSCM3GA15EP1-6F900C	-6	fpBGA	900	COM	15.2
LFSCM3GA15EP1-5F900C	-5	fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7F900C	-7	fpBGA	900	COM	25.4
LFSC3GA25E-6F900C	-6	fpBGA	900	COM	25.4
LFSC3GA25E-5F900C	-5	fpBGA	900	COM	25.4
LFSC3GA25E-7FF1020C ¹	-7	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FF1020C ¹	-6	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FF1020C ¹	-5	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7F900C	-7	fpBGA	900	COM	25.4
LFSCM3GA25EP1-6F900C	-6	fpBGA	900	COM	25.4
LFSCM3GA25EP1-5F900C	-5	fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FF1020C ¹	-7	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FF1020C ¹	-6	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FF1020C ¹	-5	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

Date	Version	Section	Change Summary
March 2007 (cont.)	01.5 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Internal Timing Parameters with ispLEVER 6.1 SP1 results.
			Updated t_{FDEL} and t_{CDEL} specifications.
			Updated LatticeSC Family Timing Adders with ispLEVER 6.1 SP1 results.
			Updated PLL specifications to expand frequency range down to 2 MHz and break out jitter for the different ranges.
			Added footnote to sysCLOCK PLL Timing table specifying the conditions for the jitter measurements.
			Added t_{DLL} specification to sysCLOCK DLL Timing table.
			Added footnote to sysCLOCK DLL Timing table specifying the conditions for the jitter measurements.
			Added sysCONFIG Master Parallel Configuration Mode and sysCONFIG SPI Port to LatticeSC sysCONFIG Port Timing table.
		Pin Information	Updated Pin Information Summary with SC40 information.
			Updated LFSC25 Logic Signal Connections: FF1020 with SC40 information.
			Updated LFSC80 Logic Signal Connections: FC1152 with SC40 information.
August 2007	01.6	General	Changed references of "HDC" to "HDC/SI".
			Changed references of "LDCN" to "LDCN/SCS".
			Changed references of "BUSYN/RCLK" to "BUSYN/RCLK/SCK".
			Changed references of "RDCFGN" to "TSALLN".
			Changed references of "TDO/RDDATA" to "TDO".
		Architecture	Updated text in Ripple Mode section.
			Added information to Global Set/Reset.
			Added information for Spread Spectrum Clocking
			Modified information for PLL/DLL Cascading. DLL to PLL is now supported.
			Modified AIL Block text and figure.
			Modified Figure 2-20 DDR/Shift Register Block.
			Added Information to Hot Socketing.
			Added new information for I/O Architecture Rules.
			Added information to SERDES Power Supply Sequencing Requirements.
		DC and Switching Characteristics	Added footnote to Hot Socketing Specifications table.
			Modified Initialization and Standby Supply Current table.
			Modified GSR Timing table.
			Modified sysCLOCK DLL Timing table to include I_{DUTY} .
			Deleted Readback Timing information from sysCONFIG Port Timing table.
			Modified data in External Switching Characteristics table.
		Pin Information	Added information to the Signal Descriptions table for HDC/SI, LDCN/SCS.
			Added footnote to Signal Descriptions table.
			Modified Description for signal BUSYN/RCLK/SCK.
			Modified data in Pin Information Summary and device-specific Pinout Information tables.