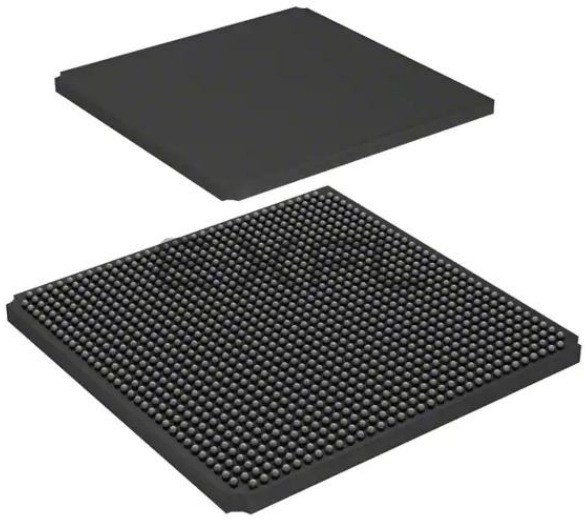
# Lattice Semiconductor Corporation - LFSC3GA80E-7FF1152C Datasheet



**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 20000 |
| Number of Logic Elements/Cells | 80000 |
| Total RAM Bits | 5816320 |
| Number of I/O | 660 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-7ff1152c |

*Table 1-1. LatticeSC Family Selection Guide*[1]

| Device | SC15 | SC25 | SC40 | SC80 | SC115 |
|---|---|---|---|---|---|
| LUT4s (K) | 15 | 25 | 40 | 80 | 115 |
| sysMEM Blocks (18Kb) | 56 | 104 | 216 | 308 | 424 |
| Embedded Memory (Mbits) | 1.03 | 1.92 | 3.98 | 5.68 | 7.8 |
| Max. Distributed Memory (Mbits) | 0.24 | 0.41 | 0.65 | 1.28 | 1.84 |
| Number of 3.8Gbps SERDES (Max.) | 8 | 16 | 16 | 32 | 32 |
| DLLs | 12 | 12 | 12 | 12 | 12 |
| Analog PLLs | 8 | 8 | 8 | 8 | 8 |
| MACO Blocks | 4 | 6 | 10 | 10 | 12 |
| **Package I/O/SERDES Combinations (1mm ball pitch)** | | | | | |
| 256-ball fpBGA (17 x 17mm) | 139/4 | | | | |
| 900-ball fpBGA (31 x 31mm) | 300/8 | 378/8 | | | |
| 1020-ball fcBGA (33 x 33mm)[2] | | 476/16 | 562/16 | | |
| 1152-ball fcBGA (35 x 35mm)[3] | | | 604/16 | 660/16 | 660/16 |
| 1704-ball fcBGA (42.5 x 42.5mm)[3] | | | | 904/32 | 942/32 |

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per PCN #02A-10.
3. Ceramic fcBGA converted to organic fcBGA per PCN #01A-10.

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

*Table 1-2. LatticeSCM Family*

| Device | SCM15 | SCM25 | SCM40 | SCM80 | SCM115 |
|---|---|---|---|---|---|
| flexiMAC Blocks<br>• 1GbE Mode<br>• 10GbE Mode<br>• PCI Express Mode | 1 | 2 | 2 | 2 | 4 |
| SPI4.2 Blocks | 1 | 2 | 2 | 2 | 2 |
| Memory Controller Blocks<br>• DDR/DDR2 DRAM Mode<br>• QDR II/II+ SRAM Mode<br>• RLDRAM I<br>• RLDRAM II CIO/SIO | 1 | 2 | 2 | 2 | 2 |
| Low-Speed CDR Blocks | 0 | 0 | 2 | 2 | 2 |
| PCI Express LTSSM (PHY) Blocks | 1 | 0 | 2 | 2 | 2 |

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

## Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

# LatticeSC/M Internal Timing Parameters[1]

**Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%**

| Parameter | Symbol | Description | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU Logic Mode Timing** | | | | | | | | | |
| $t_{LUT4\_PFU}$ | CTOF_DEL | LUT4 delay (A to D inputs to F output) | — | 0.045 | — | 0.050 | — | 0.054 | ns |
| $t_{LUT5\_PFU}$ | MTOOFX_DEL | LUT5 delay (inputs to output) | — | 0.152 | — | 0.172 | — | 0.192 | ns |
| $t_{LSR\_PFU}$ | LSR_DEL | Set/Reset to output (asynchronous) | — | 0.378 | — | 0.426 | — | 0.474 | ns |
| $t_{SUM\_PFU}$ | M_SET | Clock to Mux (M0,M1) input setup time | 0.113 | — | 0.131 | — | 0.148 | — | ns |
| $t_{HM\_PFU}$ | M_HLD | Clock to Mux (M0,M1) input hold time | -0.041 | — | -0.046 | — | -0.052 | — | ns |
| $t_{SUD\_PFU}$ | DIN_SET | Clock to D input setup time | 0.072 | — | 0.083 | — | 0.094 | — | ns |
| $t_{HD\_PFU}$ | DIN_HLD | Clock to D input hold time | -0.028 | — | -0.032 | — | -0.035 | — | ns |
| $t_{CK2Q\_PFU}$ | REG_DEL | Clock to Q delay, D-type register configuration | — | 0.224 | — | 0.252 | — | 0.279 | ns |
| $t_{LE2Q\_PFU}$ | LTCH_DEL | Clock to Q delay latch configuration | — | 0.294 | — | 0.331 | — | 0.367 | ns |
| $t_{LD2Q\_PFU}$ | TLTCH_DEL | D to Q throughput delay when latch is enabled | — | 0.300 | — | 0.338 | — | 0.376 | ns |
| **PFU Memory Mode Timing** | | | | | | | | | |
| $t_{CORAM\_PFU}$ | CLKTOF_DEL | Clock to Output | — | 0.575 | — | 0.649 | — | 0.724 | ns |
| $t_{SUDATA\_PFU}$ | DIN_SET | Data Setup Time | -0.024 | — | -0.026 | — | -0.027 | — | ns |
| $t_{HDATA\_PFU}$ | DIN_HLD | Data Hold Time | 0.075 | — | 0.084 | — | 0.094 | — | ns |
| $t_{SUADDR\_PFU}$ | WAD_SET | Address Setup Time | -0.176 | — | -0.196 | — | -0.215 | — | ns |
| $t_{HADDR\_PFU}$ | WAD_HLD | Address Hold Time | 0.110 | — | 0.124 | — | 0.138 | — | ns |
| $t_{SUWREN\_PFU}$ | WE_SET | Write/Read Enable Setup Time | 0.014 | — | 0.019 | — | 0.024 | — | ns |
| $t_{HWREN\_PFU}$ | WE_HLD | Write/Read Enable Hold Time | 0.078 | — | 0.086 | — | 0.094 | — | ns |
| **PIC Timing** | | | | | | | | | |
| **PIO Input/Output Buffer Timing** | | | | | | | | | |
| $t_{IN\_PIO}$ | IN_DEL | Input Buffer Delay(LVCMOS25) | — | 0.578 | — | 0.661 | — | 0.744 | ns |
| $t_{OUT\_PIO}$ | DOPADI_DEL | Output Buffer Delay(LVCMOS25) | — | 2.712 | — | 3.027 | — | 3.395 | ns |
| $t_{SUI\_PIO}$ | DIN_SET | Input Register Setup Time (Data Before Clock) | 0.277 | — | 0.312 | — | 0.348 | — | ns |
| $t_{HI\_PIO}$ | DIN_HLD | Input Register Hold Time (Data after Clock) | -0.267 | — | -0.306 | — | -0.345 | — | ns |
| $t_{COO\_PIO}$ | CK_DEL | Output Register Clock to Output Delay | — | 0.513 | — | 0.571 | — | 0.639 | ns |
| $t_{SUCE\_PIO}$ | CE_SET | Input Register Clock Enable Setup Time | — | 0.000 | — | 0.000 | — | 0.000 | ns |
| $t_{HCE\_PIO}$ | CE_HLD | Input Register Clock Enable Hold Time | — | 0.129 | — | 0.145 | — | 0.161 | ns |
| $t_{SULSR\_PIO}$ | LSR_SET | Set/Reset Setup Time | 0.057 | — | 0.060 | — | 0.063 | — | ns |
| $t_{HLSR\_PIO}$ | LSR_HLD | Set/Reset Hold Time | -0.151 | — | -0.159 | — | -0.169 | — | ns |
| $t_{LE2Q\_PIO}$ | CK_DEL | Input Register Clock to Q delay latch configuration | — | 0.335 | — | 0.372 | — | 0.410 | ns |
| $t_{LD2Q\_PIO}$ | DIN_DEL | Input Register D to Q throughput delay when latch is enabled | — | 0.578 | — | 0.647 | — | 0.717 | ns |

***Figure 3-8. Read Mode with Input and Output Registers***

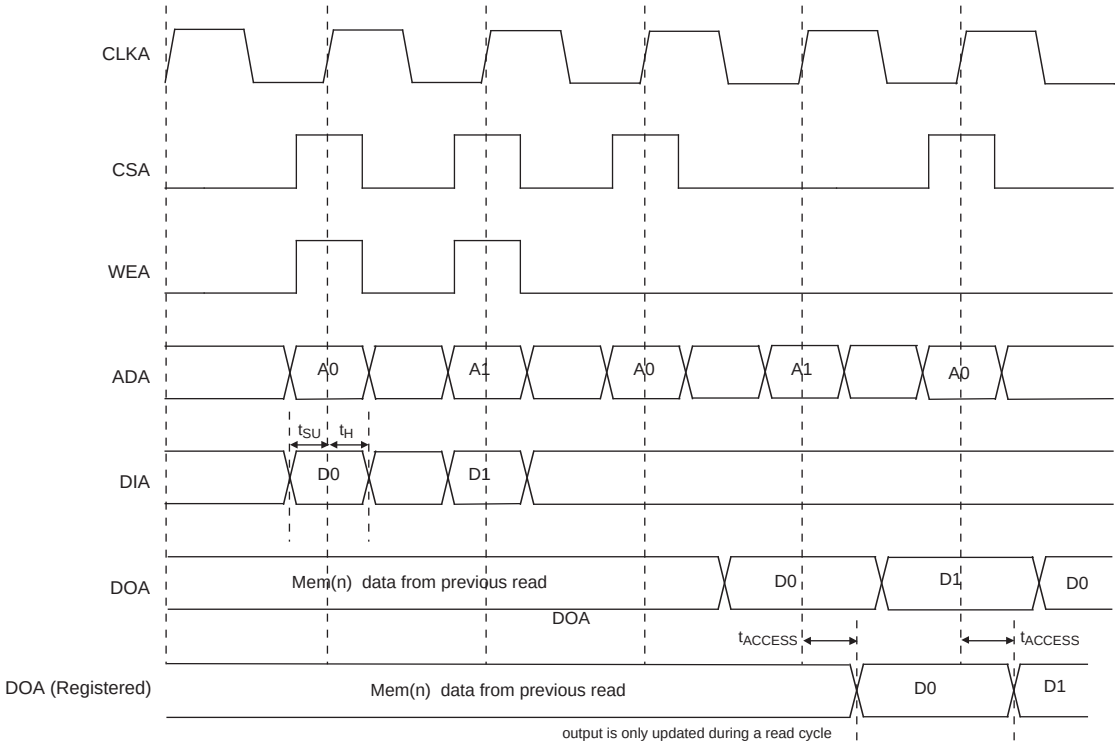
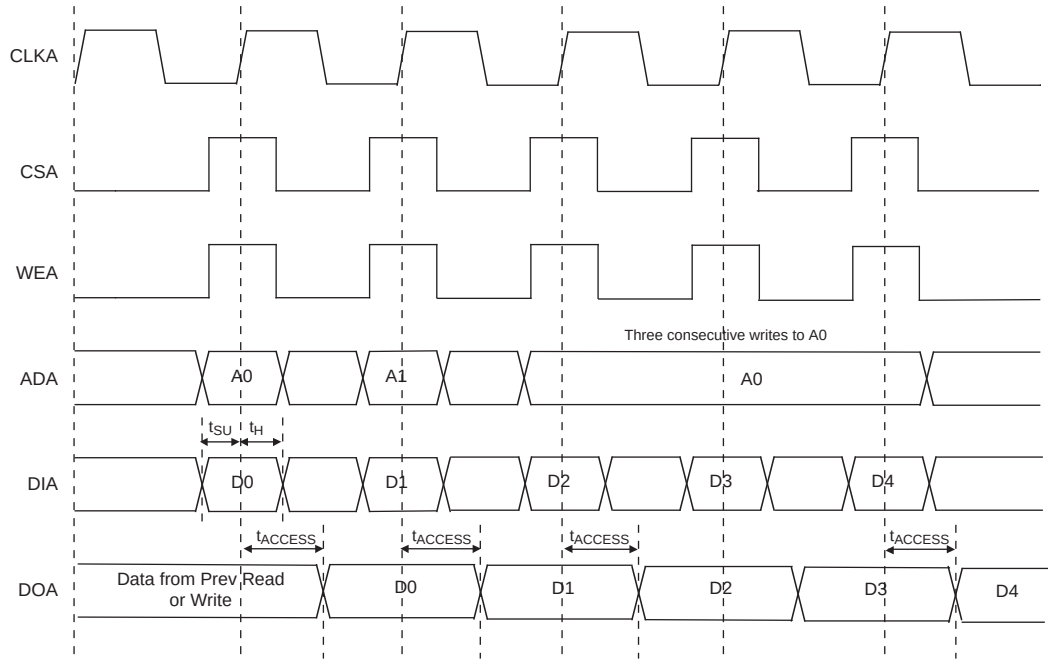



***Figure 3-9. Write Through (SP Read/Write On Port A, Input Registers Only)***




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| PROBE_GND | — | GND signal - Connected to internal VSS node. Can be used for feedback to control an external board power converter. Can be unconnected if not used. |
| **PLL and Clock Functions (Used as user-programmable I/O pins when not in use for PLL, DLL or clock pins.)** | | |
| [LOC]_PLL[T, C]_FB_[A/B] | I | PLL feedback input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the PLL is located in: ULC (upper left), URC (upper right), LLC (lower left) and LRC (lower right). [T, C] indicates whether input is true or complement. [A, B] indicates PLL reference within the corner. |
| [LOC]_DLL[T, C]_FB_[C, D, E, F] | I | DLL feedback input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the DLL is located in: ULC (upper left), URC (upper right), LLC (lower left) and LRC (lower right). [T/C] indicates whether input is true or complement. [C, D, E, F] indicates DLL reference within a corner. Note: E and F are only available on the lower corners. |
| [LOC]_PLL[T, C]_IN[A/B] | I | PLL reference clock input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the PLL is located in: ULC (upper left corner), URC (upper right corner), LLC (lower left corner) and LRC (lower right corner). [T, C] indicates whether input is true or complement.[A, B] indicates PLL reference within the corner. |
| [LOC]_DLL[T, C]_IN[C, D, E, F] | | DLL reference clock inputs. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the DLL is located in: ULC (upper left corner), URC (upper right corner), LLC (lower left corner) and LRC (lower right corner). [T/C] indicates whether input is true or complement. [C, D, E, F] indicates DLL reference within a corner. Note: E and F are only available on the lower corners. PCKLxy_[0:3] can drive primary clocks, edge clocks, and CLKDIVs. PCLKxy_[4:7] can only drive edge clocks. |
| PCLKxy_z | | General clock inputs. x indicates whether T (true) or C (complement). y indicates the I/O bank the clock is associated with. z indicates the clock number within a bank. |
| **Test and Programming (Dedicated pins. Pull-up is enabled on input pins during configuration.)** | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. |
| TDI | I | Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). |
| TDO | O | Output pin -Test Data out pin used to shift data out of device using 1149.1. |
| **Configuration Pads (Dedicated pins. Used during sysCONFIG.)** | | |
| M[3:0] | I | Mode pins used to specify configuration modes values latched on rising edge of INITN. |
| INITN | I/O | Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled that will pull the I/O above 1.5V. |
| PROGRAMN | I | Initiates configuration sequence when asserted low. This pin always has an active pull-up. |
| DONE | I/O | Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress. |
| CCLK | I/O | Configuration Clock for configuring an FPGA in sysCONFIG mode. |

## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| D[n:0] | I/O | In parallel configuration modes, D[7:0] receives configuration data, and each pin is pull-up enabled. For slave serial mode, D0 is the data input.<br><br>D[7:3] is the output internal status for peripheral mode when RDN is low.<br><br>D[7:0] is also the first byte of MPI data pins.<br><br>In MPI configuration mode, MPI selectable data bus width from 8 and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction. |
| DP[m:0] | I/O | MPI selectable parity data bus width from 1, 2, and 3-bit DP[0] for D[7:0], DP[1] for D[15:8], and DP[2] for D[23:16]. |
| BUSYN/RCLK/SCK | O | During configuration in peripheral mode, high on BUSYN indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D[7] in asynchronous peripheral mode.<br><br>During configuration in slave parallel mode, low on BUSYN inhibits the external host from sending new data. The output is used by slave parallel and master serial modes only for decompression.<br><br>During configuration in master parallel and master byte modes, RCLK is a read clock output signal to an external memory. The RCLK frequency is the same as CCLK when used with uncompressed bitstreams. RCLK will be 1/8 the frequency of CCLK when the bitstream is compressed.<br><br>During configuration in SPI modes, SCK is generated by the device and connected to the CLK input of the FLASH memory. |
| **MPI Interface (Dedicated pin)** | | |
| MPI_IRQ_N | O | MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins. |
| **MPI Interface (User I/O if MPI is not used.)** | | |
| MPI_CS0N MPI_CS1 | I | MPI chip select pins, active low on MPI_CS0N while active high on MPI_CS1. Both have to be active during the whole transfer data phase. During transfer address phase, both can be inactive so that the decoding for them from address can be slow. If they are active during address phase, one cycle can be saved for sync read. |
| MPI_CLK | I | This is the PowerPC bus clock. It can be a source of the clock for embedded system bus. If MPI_CLK is used as system bus clock, MPI will be set into sync mode by default. All of the operation on PowerPC side of MPI are synchronized to the rising edge of this clock. |
| MPI_TSIZ[1:0] | I | Driven by a bus master to indicate the data transfer size for the transaction. 01 for byte, 10 for half-word, and 00 for word. |
| MPI_WR_N | I | Driven high indicates that a read access is in progress. Driven low indicates that a write access is in process. |
| MPI_BURST | I | Driven active low indicates that a burst transfer is in progress. Driven high indicates that the current transfer is not a burst. |
| MPI_BDIP | I | Active low “Burst Data in Process” is driven by a PowerPC processor. Asserted indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase. |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| G1 | NC | - | | PL20B | 7 | |
| M4 | NC | - | | NC | - | |
| J3 | NC | - | | NC | - | |
| P5 | NC | - | | NC | - | |
| W5 | NC | - | | PL48C | 6 | |
| T6 | NC | - | | PL35C | 6 | |
| U3 | NC | - | | PL36A | 6 | |
| V3 | NC | - | | PL36B | 6 | |
| T5 | NC | - | | PL39A | 6 | |
| T4 | NC | - | | PL39B | 6 | |
| V5 | NC | - | | PL43C | 6 | |
| U6 | NC | - | | PL42C | 6 | |
| U4 | NC | - | | PL40A | 6 | |
| U5 | NC | - | | PL40B | 6 | |
| V4 | NC | - | | PL43D | 6 | |
| Y2 | NC | - | | PL47A | 6 | |
| AA2 | NC | - | | PL47B | 6 | |
| W3 | NC | - | | PL47D | 6 | |
| Y3 | NC | - | | PL47C | 6 | |
| AB3 | NC | - | | NC | - | |
| AC4 | NC | - | | PL53A | 6 | |
| AD4 | NC | - | | PL53B | 6 | |
| AE3 | NC | - | | PL56A | 6 | |
| AF3 | NC | - | | PL56B | 6 | |
| AF7 | NC | - | | PB7A | 5 | |
| AF6 | NC | - | | PB7B | 5 | |
| AH4 | NC | - | | PB8A | 5 | |
| AG5 | NC | - | | PB8B | 5 | |
| AF8 | NC | - | | PB9A | 5 | |
| AG8 | NC | - | | PB9B | 5 | |
| AG7 | NC | - | | NC | - | |
| AG10 | NC | - | | NC | - | |
| AF12 | NC | - | | NC | - | |
| AH7 | NC | - | | PB15A | 5 | |
| AE13 | NC | - | | PB15D | 5 | |
| AG13 | NC | - | | PB23C | 5 | |
| AH8 | NC | - | | PB15B | 5 | |
| AJ5 | NC | - | | PB17A | 5 | |
| AJ6 | NC | - | | PB17B | 5 | |
| AF15 | NC | - | | PB21D | 5 | |
| AJ7 | NC | - | | PB19A | 5 | |
| AJ8 | NC | - | | PB19B | 5 | |
| AE12 | NC | - | | PB15C | 5 | |
| AF16 | NC | - | | PB38D | 4 | |
| AF19 | NC | - | | PB49D | 4 | |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| U18 | GND | - | | GND | - | |
| U19 | GND | - | | GND | - | |
| U20 | GND | - | | GND | - | |
| V11 | GND | - | | GND | - | |
| V12 | GND | - | | GND | - | |
| V13 | GND | - | | GND | - | |
| V14 | GND | - | | GND | - | |
| V15 | GND | - | | GND | - | |
| V16 | GND | - | | GND | - | |
| V17 | GND | - | | GND | - | |
| V18 | GND | - | | GND | - | |
| V19 | GND | - | | GND | - | |
| V20 | GND | - | | GND | - | |
| W11 | GND | - | | GND | - | |
| W12 | GND | - | | GND | - | |
| W13 | GND | - | | GND | - | |
| W14 | GND | - | | GND | - | |
| W15 | GND | - | | GND | - | |
| W16 | GND | - | | GND | - | |
| W17 | GND | - | | GND | - | |
| W18 | GND | - | | GND | - | |
| W19 | GND | - | | GND | - | |
| W20 | GND | - | | GND | - | |
| Y11 | GND | - | | GND | - | |
| Y12 | GND | - | | GND | - | |
| Y13 | GND | - | | GND | - | |
| Y14 | GND | - | | GND | - | |
| Y15 | GND | - | | GND | - | |
| Y16 | GND | - | | GND | - | |
| Y17 | GND | - | | GND | - | |
| Y18 | GND | - | | GND | - | |
| Y19 | GND | - | | GND | - | |
| Y20 | GND | - | | GND | - | |
| H2 | VCCIO7 | - | | VCCIO7 | - | |
| N4 | VCCIO7 | - | | VCCIO7 | - | |
| N6 | VCCIO7 | - | | VCCIO7 | - | |
| J2 | VCCIO7 | - | | VCCIO7 | - | |
| L2 | VCCIO7 | - | | VCCIO7 | - | |
| H4 | VCCIO7 | - | | VCCIO7 | - | |
| AB2 | VCCIO6 | - | | VCCIO6 | - | |
| AD1 | VCCIO6 | - | | VCCIO6 | - | |
| W4 | VCCIO6 | - | | VCCIO6 | - | |
| AA4 | VCCIO6 | - | | VCCIO6 | - | |
| AE7 | VCCIO5 | - | | VCCIO5 | - | |
| AH6 | VCCIO5 | - | | VCCIO5 | - | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2]

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| C28 | A_REFCLKP_L | - | | A_REFCLKP_L | - | |
| D28 | A_REFCLKN_L | - | | A_REFCLKN_L | - | |
| B28 | VCC12 | - | | VCC12 | - | |
| F28 | RESP_ULC | - | | RESP_ULC | - | |
| J21 | RESETN | 1 | | RESETN | 1 | |
| J20 | TSALLN | 1 | | TSALLN | 1 | |
| K20 | DONE | 1 | | DONE | 1 | |
| K21 | INITN | 1 | | INITN | 1 | |
| K23 | M0 | 1 | | M0 | 1 | |
| J23 | M1 | 1 | | M1 | 1 | |
| J24 | M2 | 1 | | M2 | 1 | |
| K24 | M3 | 1 | | M3 | 1 | |
| K25 | PL16A | 7 | ULC_PLLT_IN_A/ULC_PLLT_FB_B | PL16A | 7 | ULC_PLLT_IN_A/ULC_PLLT_FB_B |
| J25 | PL16B | 7 | ULC_PLLC_IN_A/ULC_PLLC_FB_B | PL16B | 7 | ULC_PLLC_IN_A/ULC_PLLC_FB_B |
| K26 | PL16C | 7 | | PL16C | 7 | |
| K27 | PL16D | 7 | | PL16D | 7 | |
| D32 | PL17A | 7 | ULC_DLLT_IN_C/ULC_DLLT_FB_D | PL17A | 7 | ULC_DLLT_IN_C/ULC_DLLT_FB_D |
| D31 | PL17B | 7 | ULC_DLLC_IN_C/ULC_DLLC_FB_D | PL17B | 7 | ULC_DLLC_IN_C/ULC_DLLC_FB_D |
| M23 | PL17C | 7 | ULC_PLLT_IN_B/ULC_PLLT_FB_A | PL17C | 7 | ULC_PLLT_IN_B/ULC_PLLT_FB_A |
| N23 | PL17D | 7 | ULC_PLLC_IN_B/ULC_PLLC_FB_A | PL17D | 7 | ULC_PLLC_IN_B/ULC_PLLC_FB_A |
| E32 | PL18A | 7 | ULC_DLLT_IN_D/ULC_DLLT_FB_C | PL18A | 7 | ULC_DLLT_IN_D/ULC_DLLT_FB_C |
| E31 | PL18B | 7 | ULC_DLLC_IN_D/ULC_DLLC_FB_C | PL18B | 7 | ULC_DLLC_IN_D/ULC_DLLC_FB_C |
| J28 | PL18C | 7 | | PL18C | 7 | |
| K28 | PL18D | 7 | VREF2_7 | PL18D | 7 | VREF2_7 |
| F32 | PL20A | 7 | | PL21A | 7 | |
| F31 | PL20B | 7 | | PL21B | 7 | |
| L25 | PL20C | 7 | | PL21C | 7 | |
| L26 | PL20D | 7 | | PL21D | 7 | |
| G31 | PL21A | 7 | | PL22A | 7 | |
| G32 | PL21B | 7 | | PL22B | 7 | |
| J29 | PL22A | 7 | | PL25A | 7 | |
| H29 | PL22B | 7 | | PL25B | 7 | |
| M25 | PL22C | 7 | | PL25C | 7 | |
| N25 | PL22D | 7 | | PL25D | 7 | |
| H31 | PL25A | 7 | | PL23A | 7 | |
| H32 | PL25B | 7 | | PL23B | 7 | |
| M24 | PL25C | 7 | VREF1_7 | PL23C | 7 | VREF1_7 |
| N24 | PL25D | 7 | DIFFR_7 | PL23D | 7 | DIFFR_7 |
| L32 | PL26A | 7 | PCLKT7_1 | PL35A | 7 | PCLKT7_1 |
| M32 | PL26B | 7 | PCLKC7_1 | PL35B | 7 | PCLKC7_1 |
| R25 | PL26C | 7 | PCLKT7_3 | PL35C | 7 | PCLKT7_3 |
| R24 | PL26D | 7 | PCLKC7_3 | PL35D | 7 | PCLKC7_3 |
| N31 | PL27A | 7 | PCLKT7_0 | PL36A | 7 | PCLKT7_0 |
| N32 | PL27B | 7 | PCLKC7_0 | PL36B | 7 | PCLKC7_0 |
| P27 | PL27C | 7 | PCLKT7_2 | PL36C | 7 | PCLKT7_2 |
| P28 | PL27D | 7 | PCLKC7_2 | PL36D | 7 | PCLKC7_2 |
| P30 | PL29A | 6 | PCLKT6_0 | PL38A | 6 | PCLKT6_0 |
| P29 | PL29B | 6 | PCLKC6_0 | PL38B | 6 | PCLKC6_0 |
| T23 | PL29C | 6 | PCLKT6_1 | PL38C | 6 | PCLKT6_1 |
| T24 | PL29D | 6 | PCLKC6_1 | PL38D | 6 | PCLKC6_1 |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AJ31 | PB9A | 5 | | PB9A | 5 | |
| AH30 | PB9B | 5 | | PB9B | 5 | |
| AM30 | PB11A | 5 | | PB11A | 5 | |
| AM29 | PB11B | 5 | | PB11B | 5 | |
| AH29 | PB11C | 5 | | PB11C | 5 | |
| AH28 | PB11D | 5 | | PB11D | 5 | |
| AJ27 | PB12A | 5 | | PB13A | 5 | |
| AK27 | PB12B | 5 | | PB13B | 5 | |
| AE22 | PB12C | 5 | | PB13C | 5 | |
| AF23 | PB12D | 5 | | PB13D | 5 | |
| AL28 | PB13A | 5 | | PB15A | 5 | |
| AL27 | PB13B | 5 | | PB15B | 5 | |
| AC21 | PB13C | 5 | | PB15C | 5 | |
| AD21 | PB13D | 5 | | PB15D | 5 | |
| AM28 | PB15A | 5 | | PB17A | 5 | |
| AM27 | PB15B | 5 | | PB17B | 5 | |
| AG23 | PB15C | 5 | | PB17C | 5 | |
| AF22 | PB15D | 5 | | PB17D | 5 | |
| AG26 | PB16A | 5 | | PB19A | 5 | |
| AG25 | PB16B | 5 | | PB19B | 5 | |
| AL26 | PB17A | 5 | | PB22A | 5 | |
| AM26 | PB17B | 5 | | PB22B | 5 | |
| AJ24 | PB19A | 5 | | PB25A | 5 | |
| AK24 | PB19B | 5 | | PB25B | 5 | |
| AE21 | PB19C | 5 | | PB25C | 5 | |
| AE20 | PB19D | 5 | | PB25D | 5 | |
| AJ22 | PB20A | 5 | PCLKT5_3 | PB30A | 5 | PCLKT5_3 |
| AK22 | PB20B | 5 | PCLKC5_3 | PB30B | 5 | PCLKC5_3 |
| AG22 | PB20C | 5 | PCLKT5_4 | PB30C | 5 | PCLKT5_4 |
| AH22 | PB20D | 5 | PCLKC5_4 | PB30D | 5 | PCLKC5_4 |
| AL23 | PB21A | 5 | PCLKT5_5 | PB31A | 5 | PCLKT5_5 |
| AL22 | PB21B | 5 | PCLKC5_5 | PB31B | 5 | PCLKC5_5 |
| AH23 | PB21C | 5 | | PB31C | 5 | |
| AH24 | PB21D | 5 | | PB31D | 5 | |
| AJ21 | PB23A | 5 | PCLKT5_0 | PB33A | 5 | PCLKT5_0 |
| AK21 | PB23B | 5 | PCLKC5_0 | PB33B | 5 | PCLKC5_0 |
| AE19 | PB23C | 5 | | PB33C | 5 | |
| AF19 | PB23D | 5 | VREF2_5 | PB33D | 5 | VREF2_5 |
| AM23 | PB24A | 5 | PCLKT5_1 | PB34A | 5 | PCLKT5_1 |
| AM22 | PB24B | 5 | PCLKC5_1 | PB34B | 5 | PCLKC5_1 |
| AH25 | PB24C | 5 | PCLKT5_6 | PB34C | 5 | PCLKT5_6 |
| AH26 | PB24D | 5 | PCLKC5_6 | PB34D | 5 | PCLKC5_6 |
| AL21 | PB25A | 5 | PCLKT5_2 | PB35A | 5 | PCLKT5_2 |
| AL20 | PB25B | 5 | PCLKC5_2 | PB35B | 5 | PCLKC5_2 |
| AG20 | PB25C | 5 | PCLKT5_7 | PB35C | 5 | PCLKT5_7 |
| AG19 | PB25D | 5 | PCLKC5_7 | PB35D | 5 | PCLKC5_7 |
| AJ19 | PB28A | 5 | | PB37A | 5 | |
| AK19 | PB28B | 5 | | PB37B | 5 | |
| AD18 | PB28C | 5 | | PB37C | 5 | |
| AE18 | PB28D | 5 | | PB37D | 5 | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| P17 | VCC | - | | VCC | - | |
| P19 | VCC | - | | VCC | - | |
| R13 | VCC | - | | VCC | - | |
| R15 | VCC | - | | VCC | - | |
| R18 | VCC | - | | VCC | - | |
| R20 | VCC | - | | VCC | - | |
| T13 | VCC | - | | VCC | - | |
| T14 | VCC | - | | VCC | - | |
| T16 | VCC | - | | VCC | - | |
| T17 | VCC | - | | VCC | - | |
| T19 | VCC | - | | VCC | - | |
| T20 | VCC | - | | VCC | - | |
| U13 | VCC | - | | VCC | - | |
| U14 | VCC | - | | VCC | - | |
| U16 | VCC | - | | VCC | - | |
| U17 | VCC | - | | VCC | - | |
| U19 | VCC | - | | VCC | - | |
| U20 | VCC | - | | VCC | - | |
| V13 | VCC | - | | VCC | - | |
| V15 | VCC | - | | VCC | - | |
| V18 | VCC | - | | VCC | - | |
| V20 | VCC | - | | VCC | - | |
| W14 | VCC | - | | VCC | - | |
| W16 | VCC | - | | VCC | - | |
| W17 | VCC | - | | VCC | - | |
| W19 | VCC | - | | VCC | - | |
| Y13 | VCC | - | | VCC | - | |
| Y15 | VCC | - | | VCC | - | |
| Y16 | VCC | - | | VCC | - | |
| Y17 | VCC | - | | VCC | - | |
| Y18 | VCC | - | | VCC | - | |
| Y20 | VCC | - | | VCC | - | |
| C17 | VCCIO1 | - | | VCCIO1 | - | |
| D16 | VCCIO1 | - | | VCCIO1 | - | |
| F15 | VCCIO1 | - | | VCCIO1 | - | |
| F24 | VCCIO1 | - | | VCCIO1 | - | |
| G18 | VCCIO1 | - | | VCCIO1 | - | |
| G9 | VCCIO1 | - | | VCCIO1 | - | |
| J11 | VCCIO1 | - | | VCCIO1 | - | |
| J19 | VCCIO1 | - | | VCCIO1 | - | |
| K14 | VCCIO1 | - | | VCCIO1 | - | |
| K22 | VCCIO1 | - | | VCCIO1 | - | |
| G4 | VCCIO2 | - | | VCCIO2 | - | |
| J7 | VCCIO2 | - | | VCCIO2 | - | |
| K3 | VCCIO2 | - | | VCCIO2 | - | |
| L10 | VCCIO2 | - | | VCCIO2 | - | |
| M6 | VCCIO2 | - | | VCCIO2 | - | |
| N4 | VCCIO2 | - | | VCCIO2 | - | |
| P9 | VCCIO2 | - | | VCCIO2 | - | |
| R7 | VCCIO2 | - | | VCCIO2 | - | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| U12 | VCC12 | - | | VCC12 | - | |
| U21 | VCC12 | - | | VCC12 | - | |
| AA16 | VCC12 | - | | VCC12 | - | |
| AA17 | VCC12 | - | | VCC12 | - | |
| M14 | VCC12 | - | | VCC12 | - | |
| P12 | VCC12 | - | | VCC12 | - | |
| W12 | VCC12 | - | | VCC12 | - | |
| AA14 | VCC12 | - | | VCC12 | - | |
| AA19 | VCC12 | - | | VCC12 | - | |
| W21 | VCC12 | - | | VCC12 | - | |
| P21 | VCC12 | - | | VCC12 | - | |
| M19 | VCC12 | - | | VCC12 | - | |
| A2 | GND | - | | GND | - | |
| A10 | GND | - | | GND | - | |
| E28 | NC | - | | NC | - | |
| E5 | NC | - | | NC | - | |
| F10 | NC | - | | NC | - | |
| E10 | NC | - | | NC | - | |
| E23 | NC | - | | NC | - | |
| F23 | NC | - | | NC | - | |

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M25 and LatticeSC/M40 in a 1020-pin package support a 16-bit MPI interface.

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| G27 | A_REFCLKP_L | - | |
| H27 | A_REFCLKN_L | - | |
| H25 | VCC12 | - | |
| H26 | RESP_ULC | - | |
| B33 | RESETN | 1 | |
| C34 | TSALLN | 1 | |
| D34 | DONE | 1 | |
| C33 | INITN | 1 | |
| J27 | M0 | 1 | |
| K27 | M1 | 1 | |
| M26 | M2 | 1 | |
| L26 | M3 | 1 | |
| F30 | PL15A | 7 | ULC_PLLT_IN_A/ULC_PLLT_FB_B |
| G30 | PL15B | 7 | ULC_PLLC_IN_A/ULC_PLLC_FB_B |
| H28 | PL15C | 7 | |
| J28 | PL15D | 7 | |
| F31 | PL17A | 7 | ULC_DLLT_IN_C/ULC_DLLT_FB_D |
| G31 | PL17B | 7 | ULC_DLLC_IN_C/ULC_DLLC_FB_D |
| N25 | PL17C | 7 | ULC_PLLT_IN_B/ULC_PLLT_FB_A |
| P25 | PL17D | 7 | ULC_PLLC_IN_B/ULC_PLLC_FB_A |
| D33 | PL18A | 7 | ULC_DLLT_IN_D/ULC_DLLT_FB_C |
| E33 | PL18B | 7 | ULC_DLLC_IN_D/ULC_DLLC_FB_C |
| H29 | PL18C | 7 | |
| J29 | PL18D | 7 | VREF2_7 |
| F32 | PL19A | 7 | |
| G32 | PL19B | 7 | |
| P26 | PL19C | 7 | |
| N26 | PL19D | 7 | |
| H30 | PL26A | 7 | |
| J30 | PL26B | 7 | |
| L28 | PL26C | 7 | |
| M28 | PL26D | 7 | |
| J31 | PL43A | 7 | |
| K31 | PL43B | 7 | |
| L27 | PL43C | 7 | VREF1_7 |
| M27 | PL43D | 7 | DIFFR_7 |
| J32 | PL45A | 7 | |
| K32 | PL45B | 7 | |
| L29 | PL45C | 7 | |
| M29 | PL45D | 7 | |
| H33 | PL47A | 7 | |
| J33 | PL47B | 7 | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| AN33 | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B |
| AH29 | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| AJ29 | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| AM32 | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C |
| AM31 | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C |
| AG27 | PB4C | 5 | |
| AG26 | PB4D | 5 | |
| AL29 | PB5A | 5 | |
| AL28 | PB5B | 5 | |
| AH27 | PB5C | 5 | |
| AH26 | PB5D | 5 | VREF1_5 |
| AN32 | PB7A | 5 | |
| AP32 | PB7B | 5 | |
| AF25 | PB7C | 5 | |
| AE25 | PB7D | 5 | |
| AN31 | PB11A | 5 | |
| AN30 | PB11B | 5 | |
| AK29 | PB11C | 5 | |
| AK28 | PB11D | 5 | |
| AP31 | PB12A | 5 | |
| AP30 | PB12B | 5 | |
| AD24 | PB12C | 5 | |
| AE24 | PB12D | 5 | |
| AM29 | PB15A | 5 | |
| AM28 | PB15B | 5 | |
| AJ27 | PB15C | 5 | |
| AJ26 | PB15D | 5 | |
| AP29 | PB16A | 5 | |
| AP28 | PB16B | 5 | |
| AK27 | PB16C | 5 | |
| AK26 | PB16D | 5 | |
| AN29 | PB19A | 5 | |
| AN28 | PB19B | 5 | |
| AG25 | PB19C | 5 | |
| AG24 | PB19D | 5 | |
| AL26 | PB20A | 5 | |
| AL25 | PB20B | 5 | |
| AG23 | PB20C | 5 | |
| AG22 | PB20D | 5 | |
| AN27 | PB23A | 5 | |
| AN26 | PB23B | 5 | |
| AF24 | PB23C | 5 | |
| AF23 | PB23D | 5 | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| AD5 | PR94C | 3 | |
| AE2 | PR94B | 3 | |
| AD2 | PR94A | 3 | |
| AC5 | PR92D | 3 | |
| AB5 | PR92C | 3 | |
| AF1 | PR92B | 3 | |
| AE1 | PR92A | 3 | |
| AA11 | PR91D | 3 | |
| Y11 | PR91C | 3 | |
| AC4 | PR91B | 3 | |
| AB4 | PR91A | 3 | |
| AA8 | PR90D | 3 | DIFFR_3 |
| AA9 | PR90C | 3 | |
| AC3 | PR90B | 3 | |
| AB3 | PR90A | 3 | |
| AA7 | PR79D | 3 | |
| Y7 | PR79C | 3 | |
| AA2 | PR79B | 3 | |
| Y2 | PR79A | 3 | |
| AA6 | PR77D | 3 | |
| Y6 | PR77C | 3 | |
| Y4 | PR77B | 3 | |
| W4 | PR77A | 3 | |
| W11 | PR74D | 3 | |
| V11 | PR74C | 3 | |
| W2 | PR74B | 3 | |
| V2 | PR74A | 3 | |
| W9 | PR71D | 3 | |
| V9 | PR71C | 3 | |
| V1 | PR71B | 3 | |
| U1 | PR71A | 3 | |
| W10 | PR70D | 3 | |
| V10 | PR70C | 3 | |
| U2 | PR70B | 3 | |
| T2 | PR70A | 3 | |
| Y8 | PR69D | 3 | |
| W8 | PR69C | 3 | VREF1_3 |
| W5 | PR69B | 3 | |
| V5 | PR69A | 3 | |
| V7 | PR66D | 3 | PCLKC3_2 |
| U7 | PR66C | 3 | PCLKT3_2 |
| T1 | PR66B | 3 | |
| R1 | PR66A | 3 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| P38 | PL26B | 7 | | PL40B | 7 | |
| N35 | PL26C | 7 | | PL40C | 7 | |
| N36 | PL26D | 7 | | PL40D | 7 | |
| N39 | PL29A | 7 | | PL43A | 7 | |
| P39 | PL29B | 7 | | PL43B | 7 | |
| R34 | PL29C | 7 | VREF1_7 | PL43C | 7 | VREF1_7 |
| T34 | PL29D | 7 | DIFFR_7 | PL43D | 7 | DIFFR_7 |
| L41 | PL30A | 7 | | PL44A | 7 | |
| M41 | PL30B | 7 | | PL44B | 7 | |
| W29 | PL30C | 7 | | PL44C | 7 | |
| Y29 | PL30D | 7 | | PL44D | 7 | |
| L42 | PL31A | 7 | | PL45A | 7 | |
| M42 | PL31B | 7 | | PL45B | 7 | |
| U32 | PL31C | 7 | | PL45C | 7 | |
| V32 | PL31D | 7 | | PL45D | 7 | |
| R37 | PL33A | 7 | | PL47A | 7 | |
| T37 | PL33B | 7 | | PL47B | 7 | |
| M36 | PL33C | 7 | | PL47C | 7 | |
| M37 | PL33D | 7 | | PL47D | 7 | |
| P40 | PL34A | 7 | | PL48A | 7 | |
| N40 | PL34B | 7 | | PL48B | 7 | |
| R35 | PL34C | 7 | | PL48C | 7 | |
| T35 | PL34D | 7 | | PL48D | 7 | |
| N41 | PL35A | 7 | | PL49A | 7 | |
| P41 | PL35B | 7 | | PL49B | 7 | |
| V33 | PL35C | 7 | | PL49C | 7 | |
| U33 | PL35D | 7 | | PL49D | 7 | |
| R38 | PL37A | 7 | | PL51A | 7 | |
| T38 | PL37B | 7 | | PL51B | 7 | |
| R36 | PL37C | 7 | | PL51C | 7 | |
| T36 | PL37D | 7 | | PL51D | 7 | |
| N42 | PL38A | 7 | | PL52A | 7 | |
| P42 | PL38B | 7 | | PL52B | 7 | |
| Y31 | PL38C | 7 | | PL52C | 7 | |
| AA31 | PL38D | 7 | | PL52D | 7 | |
| U37 | PL39A | 7 | | PL53A | 7 | |
| V37 | PL39B | 7 | | PL53B | 7 | |
| U34 | PL39C | 7 | | PL53C | 7 | |
| V34 | PL39D | 7 | | PL53D | 7 | |
| U39 | PL41A | 7 | | PL55A | 7 | |
| T39 | PL41B | 7 | | PL55B | 7 | |
| V35 | PL41C | 7 | | PL55C | 7 | |
| W35 | PL41D | 7 | | PL55D | 7 | |
| R41 | PL42A | 7 | | PL56A | 7 | |
| T41 | PL42B | 7 | | PL56B | 7 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AU9 | PB103C | 4 | | PB117C | 4 | |
| AU8 | PB103D | 4 | | PB117D | 4 | |
| AY8 | PB104A | 4 | | PB118A | 4 | |
| AY7 | PB104B | 4 | | PB118B | 4 | |
| AU7 | PB104C | 4 | | PB118C | 4 | |
| AU6 | PB104D | 4 | | PB118D | 4 | |
| BA7 | PB105A | 4 | | PB119A | 4 | |
| BA6 | PB105B | 4 | | PB119B | 4 | |
| AN13 | PB105C | 4 | | PB119C | 4 | |
| AN12 | PB105D | 4 | | PB119D | 4 | |
| AV9 | PB107A | 4 | | PB121A | 4 | |
| AV8 | PB107B | 4 | | PB121B | 4 | |
| AT10 | PB107C | 4 | | PB121C | 4 | |
| AT9 | PB107D | 4 | | PB121D | 4 | |
| AW8 | PB108A | 4 | | PB122A | 4 | |
| AW7 | PB108B | 4 | | PB122B | 4 | |
| AP11 | PB108C | 4 | | PB122C | 4 | |
| AP10 | PB108D | 4 | | PB122D | 4 | |
| BB5 | PB109A | 4 | | PB123A | 4 | |
| BB4 | PB109B | 4 | | PB123B | 4 | |
| AR10 | PB109C | 4 | | PB123C | 4 | |
| AR9 | PB109D | 4 | | PB123D | 4 | |
| BA5 | PB111A | 4 | | PB125A | 4 | |
| BA4 | PB111B | 4 | | PB125B | 4 | |
| AT7 | PB111C | 4 | | PB125C | 4 | |
| AT6 | PB111D | 4 | | PB125D | 4 | |
| BB3 | PB112A | 4 | | PB126A | 4 | |
| BA3 | PB112B | 4 | | PB126B | 4 | |
| AM14 | PB112C | 4 | | PB126C | 4 | |
| AL14 | PB112D | 4 | | PB126D | 4 | |
| AY5 | PB113A | 4 | | PB127A | 4 | |
| AY4 | PB113B | 4 | | PB127B | 4 | |
| AN11 | PB113C | 4 | | PB127C | 4 | |
| AN10 | PB113D | 4 | | PB127D | 4 | |
| AV7 | PB115A | 4 | | PB129A | 4 | |
| AV6 | PB115B | 4 | | PB129B | 4 | |
| AM12 | PB115C | 4 | | PB129C | 4 | |
| AM11 | PB115D | 4 | | PB129D | 4 | |
| AW5 | PB116A | 4 | | PB130A | 4 | |
| AW4 | PB116B | 4 | | PB130B | 4 | |
| AT5 | PB116C | 4 | | PB130C | 4 | |
| AT4 | PB116D | 4 | | PB130D | 4 | |
| AY2 | PB117A | 4 | | PB131A | 4 | |
| BA2 | PB117B | 4 | | PB131B | 4 | |
| AP9 | PB117C | 4 | | PB131C | 4 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| E37 | B_HDINN0_L | - | PCS 361 CH 0 IN N | B_HDINN0_L | - | PCS 361 CH 0 IN N |
| D37 | B_HDINP0_L | - | PCS 361 CH 0 IN P | B_HDINP0_L | - | PCS 361 CH 0 IN P |
| F34 | B_VDDIB0_L | - | | B_VDDIB0_L | - | |
| N29 | VCC12 | - | | VCC12 | - | |
| L30 | A_VDDIB3_L | - | | A_VDDIB3_L | - | |
| K31 | VCC12 | - | | VCC12 | - | |
| D38 | A_HDINP3_L | - | PCS 360 CH 3 IN P | A_HDINP3_L | - | PCS 360 CH 3 IN P |
| E38 | A_HDINN3_L | - | PCS 360 CH 3 IN N | A_HDINN3_L | - | PCS 360 CH 3 IN N |
| A37 | A_HDOUTP3_L | - | PCS 360 CH 3 OUT P | A_HDOUTP3_L | - | PCS 360 CH 3 OUT P |
| G37 | VCC12 | - | | VCC12 | - | |
| B37 | A_HDOUTN3_L | - | PCS 360 CH 3 OUT N | A_HDOUTN3_L | - | PCS 360 CH 3 OUT N |
| L33 | A_VDDOB3_L | - | | A_VDDOB3_L | - | |
| B38 | A_HDOUTN2_L | - | PCS 360 CH 2 OUT N | A_HDOUTN2_L | - | PCS 360 CH 2 OUT N |
| D41 | A_VDDOB2_L | - | | A_VDDOB2_L | - | |
| A38 | A_HDOUTP2_L | - | PCS 360 CH 2 OUT P | A_HDOUTP2_L | - | PCS 360 CH 2 OUT P |
| K34 | VCC12 | - | | VCC12 | - | |
| E39 | A_HDINN2_L | - | PCS 360 CH 2 IN N | A_HDINN2_L | - | PCS 360 CH 2 IN N |
| D39 | A_HDINP2_L | - | PCS 360 CH 2 IN P | A_HDINP2_L | - | PCS 360 CH 2 IN P |
| M32 | A_VDDIB2_L | - | | A_VDDIB2_L | - | |
| J32 | VCC12 | - | | VCC12 | - | |
| E41 | A_VDDIB1_L | - | | A_VDDIB1_L | - | |
| M33 | VCC12 | - | | VCC12 | - | |
| D40 | A_HDINP1_L | - | PCS 360 CH 1 IN P | A_HDINP1_L | - | PCS 360 CH 1 IN P |
| E40 | A_HDINN1_L | - | PCS 360 CH 1 IN N | A_HDINN1_L | - | PCS 360 CH 1 IN N |
| B39 | A_HDOUTP1_L | - | PCS 360 CH 1 OUT P | A_HDOUTP1_L | - | PCS 360 CH 1 OUT P |
| B41 | VCC12 | - | | VCC12 | - | |
| A39 | A_HDOUTN1_L | - | PCS 360 CH 1 OUT N | A_HDOUTN1_L | - | PCS 360 CH 1 OUT N |
| C41 | A_VDDOB1_L | - | | A_VDDOB1_L | - | |
| B40 | A_HDOUTN0_L | - | PCS 360 CH 0 OUT N | A_HDOUTN0_L | - | PCS 360 CH 0 OUT N |
| E42 | A_VDDOB0_L | - | | A_VDDOB0_L | - | |
| A40 | A_HDOUTP0_L | - | PCS 360 CH 0 OUT P | A_HDOUTP0_L | - | PCS 360 CH 0 OUT P |
| F42 | VCC12 | - | | VCC12 | - | |
| D42 | A_HDINN0_L | - | PCS 360 CH 0 IN N | A_HDINN0_L | - | PCS 360 CH 0 IN N |
| C42 | A_HDINP0_L | - | PCS 360 CH 0 IN P | A_HDINP0_L | - | PCS 360 CH 0 IN P |
| H39 | A_VDDIB0_L | - | | A_VDDIB0_L | - | |
| F41 | VCC12 | - | | VCC12 | - | |
| P16 | VDDAX25_R | - | | VDDAX25_R | - | |
| P27 | VDDAX25_L | - | | VDDAX25_L | - | |
| K39 | NC | - | | PL32A | 7 | |
| L39 | NC | - | | PL32B | 7 | |
| M38 | NC | - | | PL35A | 7 | |
| K40 | NC | - | | PL36A | 7 | |
| L40 | NC | - | | PL36B | 7 | |
| N37 | NC | - | | PL39A | 7 | |
| P37 | NC | - | | PL39B | 7 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| C3 | GND | - | | GND | - | |
| C30 | GND | - | | GND | - | |
| C33 | GND | - | | GND | - | |
| C35 | GND | - | | GND | - | |
| C36 | GND | - | | GND | - | |
| C39 | GND | - | | GND | - | |
| C4 | GND | - | | GND | - | |
| C40 | GND | - | | GND | - | |
| C7 | GND | - | | GND | - | |
| C8 | GND | - | | GND | - | |
| D15 | GND | - | | GND | - | |
| D21 | GND | - | | GND | - | |
| D25 | GND | - | | GND | - | |
| D31 | GND | - | | GND | - | |
| F4 | GND | - | | GND | - | |
| F40 | GND | - | | GND | - | |
| G11 | GND | - | | GND | - | |
| G17 | GND | - | | GND | - | |
| G26 | GND | - | | GND | - | |
| G32 | GND | - | | GND | - | |
| H14 | GND | - | | GND | - | |
| H20 | GND | - | | GND | - | |
| H23 | GND | - | | GND | - | |
| H29 | GND | - | | GND | - | |
| H35 | GND | - | | GND | - | |
| H8 | GND | - | | GND | - | |
| J3 | GND | - | | GND | - | |
| J39 | GND | - | | GND | - | |
| L16 | GND | - | | GND | - | |
| L27 | GND | - | | GND | - | |
| L36 | GND | - | | GND | - | |
| L7 | GND | - | | GND | - | |
| M19 | GND | - | | GND | - | |
| M24 | GND | - | | GND | - | |
| M4 | GND | - | | GND | - | |
| M40 | GND | - | | GND | - | |
| N12 | GND | - | | GND | - | |
| N31 | GND | - | | GND | - | |
| P35 | GND | - | | GND | - | |
| P8 | GND | - | | GND | - | |
| R15 | GND | - | | GND | - | |
| R28 | GND | - | | GND | - | |
| R3 | GND | - | | GND | - | |
| R39 | GND | - | | GND | - | |
| T11 | GND | - | | GND | - | |

## Conventional Packaging

**Commercial**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA15E-7F256C | -7 | fpBGA | 256 | COM | 15.2 |
| LFSC3GA15E-6F256C | -6 | fpBGA | 256 | COM | 15.2 |
| LFSC3GA15E-5F256C | -5 | fpBGA | 256 | COM | 15.2 |
| LFSC3GA15E-7F900C | -7 | fpBGA | 900 | COM | 15.2 |
| LFSC3GA15E-6F900C | -6 | fpBGA | 900 | COM | 15.2 |
| LFSC3GA15E-5F900C | -5 | fpBGA | 900 | COM | 15.2 |

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA15EP1-7F256C | -7 | fpBGA | 256 | COM | 15.2 |
| LFSCM3GA15EP1-6F256C | -6 | fpBGA | 256 | COM | 15.2 |
| LFSCM3GA15EP1-5F256C | -5 | fpBGA | 256 | COM | 15.2 |
| LFSCM3GA15EP1-7F900C | -7 | fpBGA | 900 | COM | 15.2 |
| LFSCM3GA15EP1-6F900C | -6 | fpBGA | 900 | COM | 15.2 |
| LFSCM3GA15EP1-5F900C | -5 | fpBGA | 900 | COM | 15.2 |

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA25E-7F900C | -7 | fpBGA | 900 | COM | 25.4 |
| LFSC3GA25E-6F900C | -6 | fpBGA | 900 | COM | 25.4 |
| LFSC3GA25E-5F900C | -5 | fpBGA | 900 | COM | 25.4 |
| LFSC3GA25E-7FF1020C[1] | -7 | Organic fcBGA | 1020 | COM | 25.4 |
| LFSC3GA25E-6FF1020C[1] | -6 | Organic fcBGA | 1020 | COM | 25.4 |
| LFSC3GA25E-5FF1020C[1] | -5 | Organic fcBGA | 1020 | COM | 25.4 |
| LFSC3GA25E-7FFA1020C | -7 | Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSC3GA25E-6FFA1020C | -6 | Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSC3GA25E-5FFA1020C | -5 | Organic fcBGA Revision 2 | 1020 | COM | 25.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA25EP1-7F900C | -7 | fpBGA | 900 | COM | 25.4 |
| LFSCM3GA25EP1-6F900C | -6 | fpBGA | 900 | COM | 25.4 |
| LFSCM3GA25EP1-5F900C | -5 | fpBGA | 900 | COM | 25.4 |
| LFSCM3GA25EP1-7FF1020C[1] | -7 | Organic fcBGA | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-6FF1020C[1] | -6 | Organic fcBGA | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-5FF1020C[1] | -5 | Organic fcBGA | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-7FFA1020C | -7 | Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-6FFA1020C | -6 | Organic fcBGA Revision 2 | 1020 | COM | 25.4 |
| LFSCM3GA25EP1-5FFA1020C | -5 | Organic fcBGA Revision 2 | 1020 | COM | 25.4 |

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

# LatticeSC/M Family Data Sheet Supplemental Information

**January 2008** **Data Sheet DS1004**

## For Further Information

For further information about the flexiPCS, see the LatticeSC/M Family flexiPCS Data Sheet.

A variety of technical notes for the LatticeSC/M family are also available on the Lattice Semiconductor website at www.latticesemi.com.

- LatticeSC PURESPEED I/O Usage Guide (TN1088)
- LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide (TN1158)
- LatticeSC sysCLOCK PLL/DLL User's Guide (TN1098)
- On-Chip Memory Usage Guide for LatticeSC Devices (TN1094)
- LatticeSC/M DDR/DDR2 SDRAM Memory Interface User's Guide (TN1099)
- LatticeSC QDRII/II+ SRAM Memory Interface User's Guide (TN1096)
- LatticeSC sysCONFIG Usage Guide (TN1080)
- LatticeSC MPI/System Bus (TN1085)
- SPI Serial Flash Programming Using ispJTAG in LatticeSC Devices (TN1100)
- Power Estimation and Management for LatticeSC Devices (TN1101)
- LatticeSC SERDES Jitter (TN1084)
- LatticeSC FPGAs: Implementing 3.3V Interfaces in 2.5V VCCIO Banks (TN1110)
- Lattice PCI Express Basic Demo User's Guide (UG08)
- LatticeSC flexiPCS/SERDES Design Guide (TN1145)
- Temperature Sensing Diode in LatticeSC Devices (TN1115)
- SPI4.2 Interoperability Between ORSPI4 and LatticeSC Devices (TN1116)

For further information on Interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- Optical Interface (SPI-4.2, XSBI, CSIX and XGMII): www.oiforum.com
- RAPIDIO: www.rapidio.org
- PCI/PCIX: ww.pcisig.com