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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfsc3ga80e-7ffn1152c

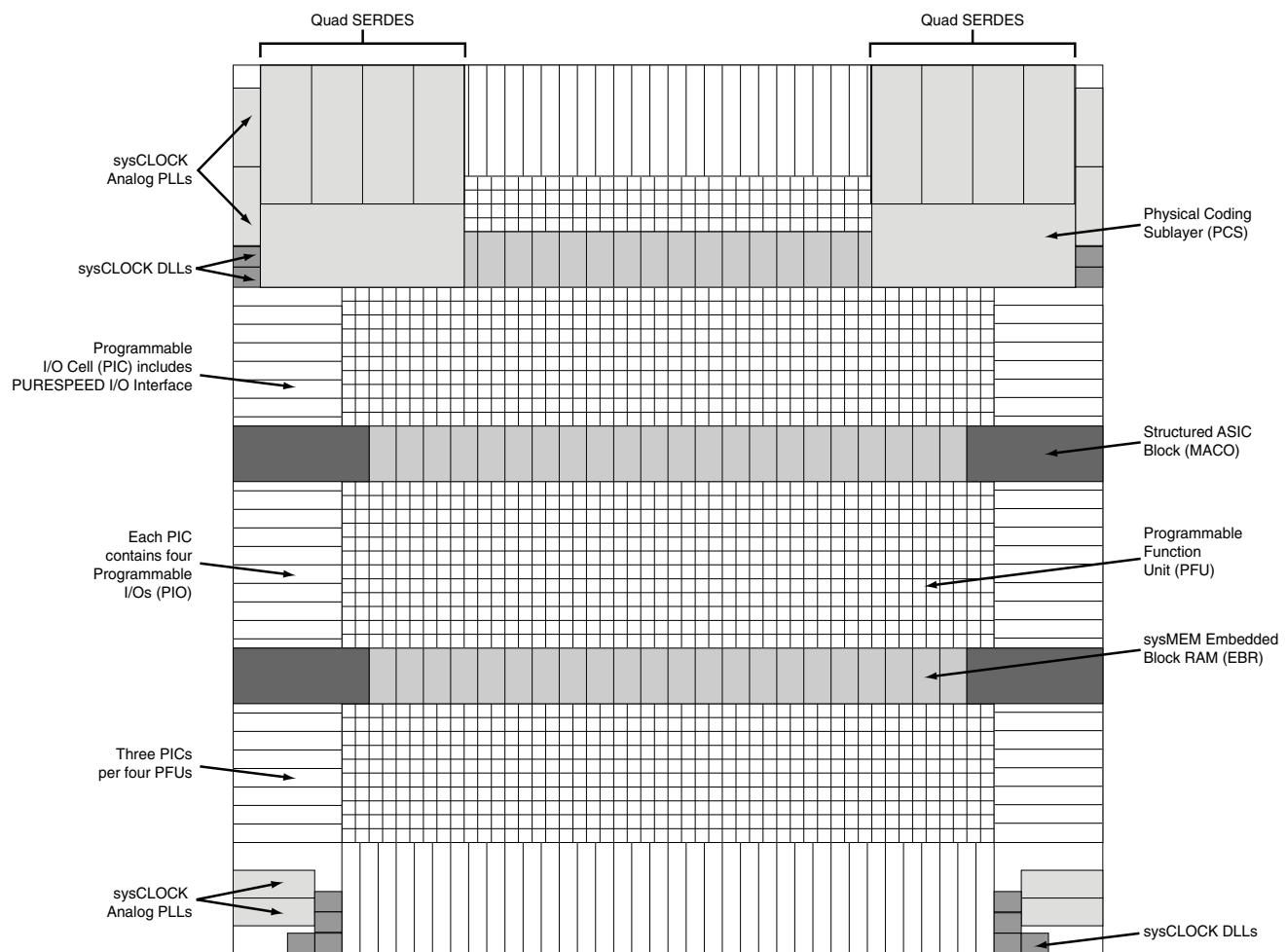
Figure 2-1. Simplified Block Diagram (Top Level)

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
FIFO	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Single, Dual and Pseudo-Dual Port Modes

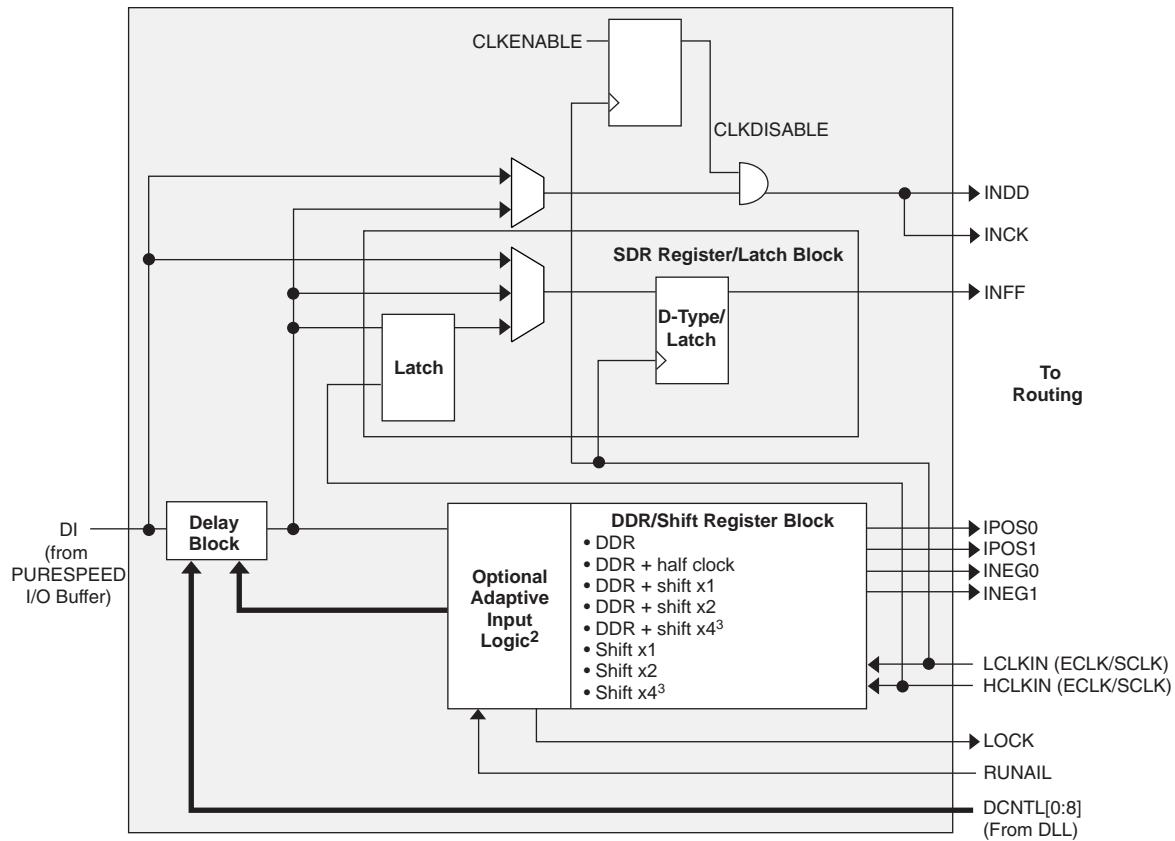
In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output. A clock is required even in asynchronous read mode.

The EBR memory supports two forms of write behavior for dual port operation:

1. **Normal** — data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output.
2. **Write Through** — a copy of the input data appears at the output of the same port.

FIFO Configuration

The FIFO has a write port with Data-in, WCE, WE and WCLK signals. There is a separate read port with Data-out, RCE, RE and RCLK signals. The FIFO internally generates Almost Full, Full, Almost Empty, and Empty Flags. The Full and Almost Full flags are registered with WCLK. The Empty and Almost Empty flags are registered with RCLK.

Figure 2-20. Input Register Block¹

1. UPDATE, Set and Reset not shown for clarity

2. Adaptive input logic is only available in selected PIO

3. By four shift modes utilize DDR/shift register block from paired PIO.

4. CLKDISABLE is used to block the transitions on the DQS pin during post-amble. Its main use is to disable DQS (typically found in DDR memory interfaces) or other clock signals. It can also be used to disable any/all input signals to save power.

Table 2-9. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}^1 (Nom.)	On-chip Termination
Single Ended Interfaces			
LVTTL33 ³	—	3.3	None
LVCMOS 33, 25, 18, 15, 12 ³	—	3.3/2.5/1.8/1.5/1.2	None
PCI33, PCIX33, AGP1X33 ³	—	3.3	None
PCIX15	0.75	1.5 ²	None / $V_{CCIO}/2$: 50, 60 / V_{TT} : 60, 75, 120, 210
AGP2X33	1.32	—	None
HSTL18_I, II	0.9	1.8 ²	None / $V_{CCIO}/2$: 50, 60 / V_{TT} : 60, 75, 120, 210
HSTL18_III, IV	1.08	1.8 ²	None / V_{CCIO} : 50
HSTL15_I, II	0.75	1.5 ²	None / $V_{CCIO}/2$: 50, 60 / V_{TT} : 60, 75, 120, 210
HSTL15_III, IV	0.9	1.5 ²	None / V_{CCIO} : 50
SSTL33_I, II	1.5	3.3	None
SSTL25_I, II	1.25	2.5 ²	None / $V_{CCIO}/2$: 50, 60 / V_{TT} : 60, 75, 120, 210
SSTL18_I, II	0.9	1.8 ²	None / $V_{CCIO}/2$: 50, 60 / V_{TT} : 60, 75, 120, 210
GTL+, GTL	1.0 / 0.8	1.5 / 1.2 ²	None / V_{CCIO} : 50
Differential Interfaces			
SSTL18D_I, II	—	1.8 ²	None / Diff: 120, 150, 220, 420 / Diff to V_{CMT} : 120, 150, 220, 420 / $V_{CCIO}/2$: 50, 60 / V_{TT} : 60, 75, 120, 210
SSTL25D_I, II	—	2.5 ²	None / Diff: 120, 150, 220, 420 / Diff to V_{CMT} : 120, 150, 220, 420 / $V_{CCIO}/2$: 50, 60 / V_{TT} : 60, 75, 120, 210
SSTL33D_I, II	—	3.3	None
HSTL15D_I, II	—	1.5 ²	None / Diff: 120, 150, 220, 420 / Diff to V_{CMT} : 120, 150, 220, 420 / $V_{CCIO}/2$: 50, 60 / V_{TT} : 60, 75, 120, 210
HSTL18D_I, II	—	1.8 ²	None / Diff: 120, 150, 220, 420 / Diff to V_{CMT} : 120, 150, 220, 420 / $V_{CCIO}/2$: 50, 60 / V_{TT} : 60, 75, 120, 210
LVDS	—	—	None / Diff: 120, 150, 220, 240 / Diff to V_{CMT} : 120, 150, 220, 240
Mini-LVDS	—	—	None / Diff: 120, 150 / Diff to V_{CMT} : 120, 150
BLVDS25	—	—	None
MLVDS25	—	—	None
RSDS	—	—	None / Diff: 120, 150, 220, 240 / Diff to V_{CMT} : 120, 150, 220, 240
LVPECL33	—	≤ 2.5	None / Diff: 120, 150, 220, 240 / Diff to V_{CMT} : 120, 150, 220, 240

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.

2. V_{CCIO} needed for on-chip termination to $V_{CCIO}/2$ or V_{CCIO} only. V_{CCIO} is not specified for off-chip termination or V_{TT} termination.

3. All ratioed input buffers and dedicated pin input buffers include hysteresis with a typical value of 50mV.

VDDAX25 needs to be connected independent of the use of the SERDES. This supply is used to control the SERDES CML I/O regardless of the SERDES being used in the design.

Supported Source Synchronous Interfaces

The LatticeSC devices contain a variety of hardware, such as delay elements, DDR registers and PLLs, to simplify the implementation of Source Synchronous interfaces. Table 2-11 lists Source Synchronous and DDR/QDR standards supported in the LatticeSC. For additional detail refer to technical information at the end of the data sheet.

Table 2-11. Source Synchronous Standards Table¹

Source Synchronous Standard	Clocking	Speeds (MHz)	Data Rate (Mbps)
RapidIO	DDR	500	1000
SPI4.2 (POS-PHY4)/NPSI	DDR	500	1000
SFI4/XSBI	DDR	334	667
	SDR	667	
XGMII	DDR	156.25	312
CSIX	SDR	250	250
QDRII/QDRII+ memory interface	DDR	300	600
DDR memory interface	DDR	240	480
DDRII memory interface	DDR	333	667
RLDRAM memory interface	DDR	400	800

1. Memory width is dependent on the system design and limited by the number of I/Os in the device.

flexiPCS™ (Physical Coding Sublayer Block)

flexiPCS Functionality

The LatticeSC family combines a high-performance FPGA fabric, high-performance I/Os and large embedded RAM in a single industry leading architecture. LatticeSC devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES for high-speed, full-duplex serial data transfers at data rates up to 3.8 Gbps. The PCS logic in each channel can be configured to support an array of popular data protocols including SONET (STS-12/STS-12c, STS-48/STS-48c, and TFI-5 support of 10 Gbps or above), Gigabit Ethernet (compliant to the IEEE 1000BASE-X specification), 1.02 or 2.04 Gbps Fibre Channel, PCI-Express, and Serial RapidIO. In addition, the protocol based logic can be fully or partially bypassed in a number of configurations to allow users flexibility in designing their own high-speed data interface.

Protocols requiring data rates above 3.8 Gbps can be accommodated by dedicating either one pair or all four channels in one flexiPCS quad block to one data link. One quad can support full-duplex serial data transfers at data rates up to 15.2 Gbps. A single flexiPCS quad can be configured to support 10Gb Ethernet (with a fully compliant XAUI interface), 10Gb Fibre Channel, and x4 PCI-Express and 4x RapidIO.

The flexiPCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic which can also be geared to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Each SERDES pin can be DC coupled independently and can allow for both high-speed and low-speed operation down to DC rates on the same SERDES pin, as required by some Serial Digital Video applications.

The ispLEVER design tools from Lattice support all modes of the flexiPCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow a user to define their own operation. With ispLEVER, the user can define the mode for each quad in a design. Nine modes are currently supported by the ispLEVER design flow:

Switching Test Conditions

Figure 3-15 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-4.

Figure 3-15. Output Test Load, LVTTL and LVC MOS Standards

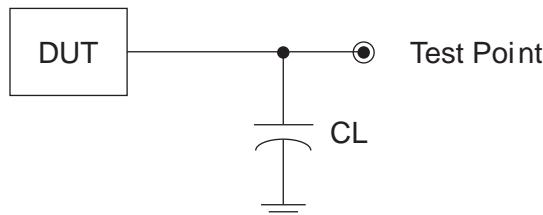


Table 3-4. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	C_L	Timing Ref.	V_T
LVTTL and other LVC MOS settings (L -> H, H -> L)	30pF	LVC MOS 3.3 = 1.5V	—
		LVC MOS 2.5 = $V_{CCIO}/2$	—
		LVC MOS 1.8 = $V_{CCIO}/2$	—
		LVC MOS 1.5 = $V_{CCIO}/2$	—
		LVC MOS 1.2 = $V_{CCIO}/2$	—
LVC MOS 2.5 I/O (Z -> H)	30pF	$V_{CCIO}/2$	V_{OL}
LVC MOS 2.5 I/O (Z -> L)		$V_{CCIO}/2$	V_{OH}
LVC MOS 2.5 I/O (H -> Z)		$V_{OH} - 0.15$	V_{OL}
LVC MOS 2.5 I/O (L -> Z)		$V_{OL} + 0.15$	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Pin Information Summary (Cont.)

Pin Type	1152 fcBGA			1704 fcBGA	
	LFSC/M40	LFSC/M80	LFSC/M115	LFSC/M80	LFSC/M115
Single Ended User I/O	604	660	660	904	942
Differential Pair User I/O	302	330	330	452	470
LVDS Output Pairs	78	102	102	114	132
Configuration	Dedicated	11	11	11	11
	Muxes/MPI sysBus	72	72	72	72
JTAG (excluding VCCJ)	4	4	4	4	4
Dedicated Pins	4	4	4	4	4
VCC	44	44	44	76	76
VCC12	52	52	52	88	88
VCCAUX	38	38	38	52	52
VCCIO	Bank 1	10	10	10	10
	Bank 2	9	9	12	12
	Bank 3	12	12	14	14
	Bank 4	12	12	14	14
	Bank 5	12	12	14	14
	Bank 6	12	12	14	14
	Bank 7	9	9	12	12
VTT	Bank 2	3	3	4	4
	Bank 3	3	3	4	4
	Bank 4	3	3	5	5
	Bank 5	3	3	5	5
	Bank 6	3	3	4	4
	Bank 7	3	3	4	4
GND	130	130	130	184	184
NC	62	6	6	52	14
Single Ended User / Differential I/O per Bank	Bank 1	80/40	80/40	80/40	80/40
	Bank 2	60/30	76/38	76/38	96/48
	Bank 3	96/48	108/54	108/54	132/66
	Bank 4	106/53	106/53	106/53	184/92
	Bank 5	106/53	106/53	106/53	184/92
	Bank 6	96/48	108/54	108/54	132/66
	Bank 7	60/30	76/38	76/38	96/48
LVDS Output Pairs Per Bank	Bank 2	15	21	21	27
	Bank 3	24	30	30	39
	Bank 6	24	30	30	39
	Bank 7	15	21	21	27
VCCJ	1	1	1	1	1
SERDES (signal + power supply)	108	108	108	212	212
Total	1152	1152	1152	1704	1704

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH29	PB48B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB68B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AE26	PB48C	4		PB68C	4	
AD25	PB48D	4		PB68D	4	
AJ30	PB49A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB69A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AH30	PB49B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB69B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AG28	PB49C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB69C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AG29	PB49D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB69D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF26	VCC12	-		VCC12	-	
AD27	PROBE_VCC	-		PROBE_VCC	-	
AG27	VCC12	-		VCC12	-	
AE28	PROBE_GND	-		PROBE_GND	-	
AC25	PR45D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR57D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AD26	PR45C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR57C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AF28	PR45B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR57B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AF29	PR45A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR57A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AC26	PR44D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR55D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AB26	PR44C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR55C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AG30	PR44B	3		PR55B	3	
AF30	PR44A	3		PR55A	3	
AC28	PR43B	3		PR52B	3	
AB28	PR43A	3		PR52A	3	
AB27	PR41D	3	VREF2_3	PR51D	3	VREF2_3
AE30	PR41B	3		PR51B	3	
AD30	PR41A	3		PR51A	3	
AB25	PR40B	3		PR49B	3	
AA25	PR40A	3		PR49A	3	
AA30	PR39B	3		PR48B	3	
Y30	PR39A	3		PR48A	3	
W29	PR37B	3		PR44B	3	
V29	PR37A	3		PR44A	3	
U30	PR36B	3		PR43B	3	
T30	PR36A	3		PR43A	3	
V25	PR35D	3	DIFFR_3	PR42D	3	DIFFR_3
W28	PR35B	3		PR42B	3	
V28	PR35A	3		PR42A	3	
R30	PR33B	3		PR38B	3	
P30	PR33A	3		PR38A	3	
N30	PR32B	3		PR35B	3	
M29	PR32A	3		PR35A	3	
U26	PR31D	3		PR34D	3	
T26	PR31C	3	VREF1_3	PR34C	3	VREF1_3
U28	PR31B	3		PR34B	3	
T28	PR31A	3		PR34A	3	
M30	PR28D	3	PCLKC3_2	PR31D	3	PCLKC3_2
L29	PR28C	3	PCLKT3_2	PR31C	3	PCLKT3_2

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W24	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC18	VCCAUX	-		VCCAUX	-	
AC19	VCCAUX	-		VCCAUX	-	
AD17	VCCAUX	-		VCCAUX	-	
AD18	VCCAUX	-		VCCAUX	-	
AD19	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
AC14	VCCAUX	-		VCCAUX	-	
AD12	VCCAUX	-		VCCAUX	-	
AD13	VCCAUX	-		VCCAUX	-	
AD14	VCCAUX	-		VCCAUX	-	
U7	VCCAUX	-		VCCAUX	-	
U8	VCCAUX	-		VCCAUX	-	
V7	VCCAUX	-		VCCAUX	-	
V8	VCCAUX	-		VCCAUX	-	
W7	VCCAUX	-		VCCAUX	-	
W8	VCCAUX	-		VCCAUX	-	
M7	VCCAUX	-		VCCAUX	-	
M8	VCCAUX	-		VCCAUX	-	
N7	VCCAUX	-		VCCAUX	-	
N8	VCCAUX	-		VCCAUX	-	
H10	VCCIO1	-		VCCIO1	-	
H21	VCCIO1	-		VCCIO1	-	
H22	VCCIO1	-		VCCIO1	-	
H9	VCCIO1	-		VCCIO1	-	
J11	VCCIO1	-		VCCIO1	-	
J12	VCCIO1	-		VCCIO1	-	
J13	VCCIO1	-		VCCIO1	-	
J14	VCCIO1	-		VCCIO1	-	
J15	VCCIO1	-		VCCIO1	-	
J16	VCCIO1	-		VCCIO1	-	
J17	VCCIO1	-		VCCIO1	-	
J18	VCCIO1	-		VCCIO1	-	
J19	VCCIO1	-		VCCIO1	-	
J20	VCCIO1	-		VCCIO1	-	
J23	VCCIO2	-		VCCIO2	-	
J24	VCCIO2	-		VCCIO2	-	
K23	VCCIO2	-		VCCIO2	-	
K24	VCCIO2	-		VCCIO2	-	
L22	VCCIO2	-		VCCIO2	-	
L23	VCCIO2	-		VCCIO2	-	
M22	VCCIO2	-		VCCIO2	-	
N22	VCCIO2	-		VCCIO2	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y6	PR42D	3	DIFFR_3	PR51D	3	DIFFR_3
W6	PR42C	3		PR51C	3	
Y2	PR42B	3		PR51B	3	
W2	PR42A	3		PR51A	3	
W7	PR40D	3		PR49D	3	
V8	PR40C	3		PR49C	3	
W4	PR40B	3		PR49B	3	
W3	PR40A	3		PR49A	3	
V5	PR39D	3		PR48D	3	
U6	PR39C	3		PR48C	3	
V3	PR39B	3		PR48B	3	
V4	PR39A	3		PR48A	3	
V10	PR38D	3		PR47D	3	
V9	PR38C	3		PR47C	3	
V2	PR38B	3		PR47B	3	
V1	PR38A	3		PR47A	3	
U8	PR36D	3		PR45D	3	
U7	PR36C	3		PR45C	3	
U2	PR36B	3		PR45B	3	
U1	PR36A	3		PR45A	3	
U5	PR35D	3		PR44D	3	
T6	PR35C	3		PR44C	3	
T1	PR35B	3		PR44B	3	
T2	PR35A	3		PR44A	3	
U9	PR34D	3		PR43D	3	
U10	PR34C	3	VREF1_3	PR43C	3	VREF1_3
R1	PR34B	3		PR43B	3	
R2	PR34A	3		PR43A	3	
T7	PR31D	3	PCLKC3_2	PR40D	3	PCLKC3_2
T8	PR31C	3	PCLKT3_2	PR40C	3	PCLKT3_2
R4	PR31B	3		PR40B	3	
R3	PR31A	3		PR40A	3	
T5	PR30D	3	PCLKC3_3	PR39D	3	PCLKC3_3
R5	PR30C	3	PCLKT3_3	PR39C	3	PCLKT3_3
P2	PR30B	3		PR39B	3	
P1	PR30A	3		PR39A	3	
T9	PR29D	3	PCLKC3_1	PR38D	3	PCLKC3_1
T10	PR29C	3	PCLKT3_1	PR38C	3	PCLKT3_1
P4	PR29B	3	PCLKC3_0	PR38B	3	PCLKC3_0
P3	PR29A	3	PCLKT3_0	PR38A	3	PCLKT3_0
P5	PR27D	2	PCLKC2_2	PR36D	2	PCLKC2_2
P6	PR27C	2	PCLKT2_2	PR36C	2	PCLKT2_2
N1	PR27B	2	PCLKC2_0	PR36B	2	PCLKC2_0
N2	PR27A	2	PCLKT2_0	PR36A	2	PCLKT2_0
R9	PR26D	2	PCLKC2_3	PR35D	2	PCLKC2_3
R8	PR26C	2	PCLKT2_3	PR35C	2	PCLKT2_3
M1	PR26B	2	PCLKC2_1	PR35B	2	PCLKC2_1
L1	PR26A	2	PCLKT2_1	PR35A	2	PCLKT2_1
N9	PR25D	2	DIFFR_2	PR23D	2	DIFFR_2
M9	PR25C	2	VREF1_2	PR23C	2	VREF1_2

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E22	VCC12	-		VCC12	-	
E21	VCC12	-		VCC12	-	
E3	VCC12	-		VCC12	-	
E4	VCC12	-		VCC12	-	
E6	VCC12	-		VCC12	-	
E7	VCC12	-		VCC12	-	
E8	VCC12	-		VCC12	-	
E9	VCC12	-		VCC12	-	
E11	VCC12	-		VCC12	-	
E12	VCC12	-		VCC12	-	
A23	GND	-		GND	-	
A31	GND	-		GND	-	
AA13	GND	-		GND	-	
AA15	GND	-		GND	-	
AA18	GND	-		GND	-	
AA20	GND	-		GND	-	
AA26	GND	-		GND	-	
AA6	GND	-		GND	-	
AB10	GND	-		GND	-	
AB24	GND	-		GND	-	
AC14	GND	-		GND	-	
AC22	GND	-		GND	-	
AC29	GND	-		GND	-	
AC3	GND	-		GND	-	
AD11	GND	-		GND	-	
AD19	GND	-		GND	-	
AD27	GND	-		GND	-	
AD7	GND	-		GND	-	
AF12	GND	-		GND	-	
AF18	GND	-		GND	-	
AF24	GND	-		GND	-	
AF30	GND	-		GND	-	
AF4	GND	-		GND	-	
AG15	GND	-		GND	-	
AG21	GND	-		GND	-	
AG9	GND	-		GND	-	
AJ10	GND	-		GND	-	
AJ16	GND	-		GND	-	
AJ20	GND	-		GND	-	
AJ26	GND	-		GND	-	
AJ29	GND	-		GND	-	
AJ4	GND	-		GND	-	
AK13	GND	-		GND	-	
AK17	GND	-		GND	-	
AK23	GND	-		GND	-	
AK7	GND	-		GND	-	
AL1	GND	-		GND	-	
AL32	GND	-		GND	-	
AM2	GND	-		GND	-	
AM31	GND	-		GND	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G27	A_REFCLKP_L	-		A_REFCLKP_L	-	
H27	A_REFCLKN_L	-		A_REFCLKN_L	-	
H25	VCC12	-		VCC12	-	
H26	RESP_ULC	-		RESP_ULC	-	
B33	RESETN	1		RESETN	1	
C34	TSALLN	1		TSALLN	1	
D34	DONE	1		DONE	1	
C33	INITN	1		INITN	1	
J27	M0	1		M0	1	
K27	M1	1		M1	1	
M26	M2	1		M2	1	
L26	M3	1		M3	1	
F30	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
G30	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
H28	PL16C	7		PL16C	7	
J28	PL16D	7		PL16D	7	
F31	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N25	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P25	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
D33	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E33	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
H29	PL18C	7		PL18C	7	
J29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F32	PL21A	7		PL20A	7	
G32	PL21B	7		PL20B	7	
P26	PL21C	7		PL20C	7	
N26	PL21D	7		PL20D	7	
H30	PL22A	7		PL21A	7	
J30	PL22B	7		PL21B	7	
L28	PL22C	7		PL21C	7	
M28	PL22D	7		PL21D	7	
J31	PL23A	7		PL29A	7	
K31	PL23B	7		PL29B	7	
L27	PL23C	7	VREF1_7	PL29C	7	VREF1_7
M27	PL23D	7	DIFFR_7	PL29D	7	DIFFR_7
J32	PL25A	7		PL31A	7	
K32	PL25B	7		PL31B	7	
L29	PL25C	7		PL31C	7	
M29	PL25D	7		PL31D	7	
H33	PL26A	7		PL33A	7	
J33	PL26B	7		PL33B	7	
N27	PL26C	7		PL33C	7	
P27	PL26D	7		PL33D	7	
K33	PL27A	7		PL35A	7	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH27	PB5C	5		PB5C	5	
AH26	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AN32	PB7A	5		PB7A	5	
AP32	PB7B	5		PB7B	5	
AF25	PB7C	5		PB7C	5	
AE25	PB7D	5		PB7D	5	
AN31	PB8A	5		PB9A	5	
AN30	PB8B	5		PB9B	5	
AK29	PB8C	5		PB9C	5	
AK28	PB8D	5		PB9D	5	
AP31	PB9A	5		PB11A	5	
AP30	PB9B	5		PB11B	5	
AD24	PB9C	5		PB11C	5	
AE24	PB9D	5		PB11D	5	
AM29	PB11A	5		PB13A	5	
AM28	PB11B	5		PB13B	5	
AJ27	PB11C	5		PB13C	5	
AJ26	PB11D	5		PB13D	5	
AP29	PB13A	5		PB15A	5	
AP28	PB13B	5		PB15B	5	
AK27	PB13C	5		PB15C	5	
AK26	PB13D	5		PB15D	5	
AN29	PB15A	5		PB17A	5	
AN28	PB15B	5		PB17B	5	
AG25	PB15C	5		PB17C	5	
AG24	PB15D	5		PB17D	5	
AL26	PB17A	5		PB19A	5	
AL25	PB17B	5		PB19B	5	
AG23	PB17C	5		PB19C	5	
AG22	PB17D	5		PB19D	5	
AN27	PB19A	5		PB21A	5	
AN26	PB19B	5		PB21B	5	
AF24	PB19C	5		PB21C	5	
AF23	PB19D	5		PB21D	5	
AP27	PB22A	5		PB24A	5	
AP26	PB22B	5		PB24B	5	
AK25	PB22C	5		PB24C	5	
AK24	PB22D	5		PB24D	5	
AN25	PB25A	5		PB27A	5	
AN24	PB25B	5		PB27B	5	
AE22	PB25C	5		PB27C	5	
AE21	PB25D	5		PB27D	5	
AM26	PB26A	5		PB29A	5	
AM25	PB26B	5		PB29B	5	
AF22	PB26C	5		PB29C	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF21	PB26D	5		PB29D	5	
AN23	PB27A	5		PB45A	5	
AN22	PB27B	5		PB45B	5	
AP23	PB29A	5		PB55A	5	
AP22	PB29B	5		PB55B	5	
AG21	PB29C	5		PB55C	5	
AG20	PB29D	5		PB55D	5	
AP25	PB30A	5	PCLKT5_3	PB48A	5	PCLKT5_3
AP24	PB30B	5	PCLKC5_3	PB48B	5	PCLKC5_3
AD21	PB30C	5	PCLKT5_4	PB48C	5	PCLKT5_4
AD20	PB30D	5	PCLKC5_4	PB48D	5	PCLKC5_4
AL23	PB31A	5	PCLKT5_5	PB49A	5	PCLKT5_5
AL22	PB31B	5	PCLKC5_5	PB49B	5	PCLKC5_5
AH24	PB31C	5		PB49C	5	
AH23	PB31D	5		PB49D	5	
AM23	PB33A	5	PCLKT5_0	PB51A	5	PCLKT5_0
AM22	PB33B	5	PCLKC5_0	PB51B	5	PCLKC5_0
AJ24	PB33C	5		PB51C	5	
AJ23	PB33D	5	VREF2_5	PB51D	5	VREF2_5
AN21	PB34A	5	PCLKT5_1	PB52A	5	PCLKT5_1
AN20	PB34B	5	PCLKC5_1	PB52B	5	PCLKC5_1
AE19	PB34C	5	PCLKT5_6	PB52C	5	PCLKT5_6
AD19	PB34D	5	PCLKC5_6	PB52D	5	PCLKC5_6
AK21	PB35A	5	PCLKT5_2	PB53A	5	PCLKT5_2
AK20	PB35B	5	PCLKC5_2	PB53B	5	PCLKC5_2
AK23	PB35C	5	PCLKT5_7	PB53C	5	PCLKT5_7
AK22	PB35D	5	PCLKC5_7	PB53D	5	PCLKC5_7
AL20	PB37A	5		PB56A	5	
AL19	PB37B	5		PB56B	5	
AG19	PB37C	5		PB56C	5	
AF19	PB37D	5		PB56D	5	
AP21	PB38A	5		PB57A	5	
AP20	PB38B	5		PB57B	5	
AH21	PB38C	5		PB57C	5	
AH20	PB38D	5		PB57D	5	
AM20	PB39A	5		PB59A	5	
AM19	PB39B	5		PB59B	5	
AJ21	PB39C	5		PB59C	5	
AJ20	PB39D	5		PB59D	5	
AK19	PB41A	5		PB60A	5	
AK18	PB41B	5		PB60B	5	
AE18	PB41C	5		PB60C	5	
AD18	PB41D	5		PB60D	5	
AN19	PB42A	5		PB61A	5	
AN18	PB42B	5		PB61B	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C2	VCCJ	-		VCCJ	-	
M9	TDO	-	TDO	TDO	-	TDO
L9	TMS	-		TMS	-	
D1	TCK	-		TCK	-	
C1	TDI	-		TDI	-	
J8	PROGRAMN	1		PROGRAMN	1	
K8	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
B2	CCLK	1		CCLK	1	
H9	RESP_URC	-		RESP_URC	-	
H10	VCC12	-		VCC12	-	
H8	A_REFCLKN_R	-		A_REFCLKN_R	-	
G8	A_REFCLKP_R	-		A_REFCLKP_R	-	
C3	VCC12	-		VCC12	-	
D3	A_VDDIB0_R	-		A_VDDIB0_R	-	
A3	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B3	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E5	VCC12	-		VCC12	-	
A4	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
F6	A_VDDOB0_R	-		A_VDDOB0_R	-	
B4	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
F7	A_VDDOB1_R	-		A_VDDOB1_R	-	
B5	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
E6	VCC12	-		VCC12	-	
A5	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
B6	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
A6	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
C6	VCC12	-		VCC12	-	
D4	A_VDDIB1_R	-		A_VDDIB1_R	-	
C7	VCC12	-		VCC12	-	
D5	A_VDDIB2_R	-		A_VDDIB2_R	-	
A7	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
B7	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
E7	VCC12	-		VCC12	-	
A8	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
F8	A_VDDOB2_R	-		A_VDDOB2_R	-	
B8	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
F9	A_VDDOB3_R	-		A_VDDOB3_R	-	
B9	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
E8	VCC12	-		VCC12	-	
A9	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
B10	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
A10	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
C10	VCC12	-		VCC12	-	
D6	A_VDDIB3_R	-		A_VDDIB3_R	-	
G10	VCC12	-		VCC12	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K20	GND	-		GND	-	
K23	GND	-		GND	-	
K26	GND	-		GND	-	
K28	GND	-		GND	-	
K6	GND	-		GND	-	
K9	GND	-		GND	-	
L12	GND	-		GND	-	
L32	GND	-		GND	-	
L4	GND	-		GND	-	
M10	GND	-		GND	-	
M17	GND	-		GND	-	
M24	GND	-		GND	-	
N29	GND	-		GND	-	
N7	GND	-		GND	-	
P15	GND	-		GND	-	
P20	GND	-		GND	-	
P3	GND	-		GND	-	
P31	GND	-		GND	-	
R10	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
T15	GND	-		GND	-	
T17	GND	-		GND	-	
T18	GND	-		GND	-	
T20	GND	-		GND	-	
T28	GND	-		GND	-	
T6	GND	-		GND	-	
U16	GND	-		GND	-	
U19	GND	-		GND	-	
U23	GND	-		GND	-	
U32	GND	-		GND	-	
U4	GND	-		GND	-	
V12	GND	-		GND	-	
V16	GND	-		GND	-	
V19	GND	-		GND	-	
V3	GND	-		GND	-	
V31	GND	-		GND	-	
W15	GND	-		GND	-	
W17	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W29	GND	-		GND	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB15	VCC12	-		VCC12	-	
AB20	VCC12	-		VCC12	-	
N15	VCC12	-		VCC12	-	
N20	VCC12	-		VCC12	-	
R13	VCC12	-		VCC12	-	
R22	VCC12	-		VCC12	-	
Y13	VCC12	-		VCC12	-	
Y22	VCC12	-		VCC12	-	
AA12	VCCAUX	-		VCCAUX	-	
AA23	VCCAUX	-		VCCAUX	-	
AB12	VCCAUX	-		VCCAUX	-	
AB16	VCCAUX	-		VCCAUX	-	
AB17	VCCAUX	-		VCCAUX	-	
AB18	VCCAUX	-		VCCAUX	-	
AB19	VCCAUX	-		VCCAUX	-	
AB23	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
Y19	GND	-		GND	-	
AC14	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC21	VCCAUX	-		VCCAUX	-	
AC22	VCCAUX	-		VCCAUX	-	
AC23	VCCAUX	-		VCCAUX	-	
M13	VCCAUX	-		VCCAUX	-	
M14	VCCAUX	-		VCCAUX	-	
M18	VCCAUX	-		VCCAUX	-	
M21	VCCAUX	-		VCCAUX	-	
M22	VCCAUX	-		VCCAUX	-	
N12	VCCAUX	-		VCCAUX	-	
N16	VCCAUX	-		VCCAUX	-	
N17	VCCAUX	-		VCCAUX	-	
N18	VCCAUX	-		VCCAUX	-	
N19	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
P12	VCCAUX	-		VCCAUX	-	
P23	VCCAUX	-		VCCAUX	-	
T13	VCCAUX	-		VCCAUX	-	
T22	VCCAUX	-		VCCAUX	-	
U12	VCCAUX	-		VCCAUX	-	
U13	VCCAUX	-		VCCAUX	-	
U22	VCCAUX	-		VCCAUX	-	
V13	VCCAUX	-		VCCAUX	-	
V22	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL4	PR117B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR117A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR116D	3	
AD9	PR116C	3	
AH4	PR116B	3	
AJ4	PR116A	3	
AK5	PR115D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR115C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR115B	3	
AL1	PR115A	3	
AH5	PR112D	3	
AG5	PR112C	3	
AL2	PR112B	3	
AK2	PR112A	3	
AB9	PR109D	3	
AC9	PR109C	3	
AH1	PR109B	3	
AG1	PR109A	3	
AE8	PR107D	3	VREF2_3
AD8	PR107C	3	
AJ3	PR107B	3	
AH3	PR107A	3	
AD7	PR104D	3	
AC7	PR104C	3	
AJ2	PR104B	3	
AH2	PR104A	3	
AF6	PR103D	3	
AF5	PR103C	3	
AF4	PR103B	3	
AE4	PR103A	3	
AD6	PR99D	3	
AC6	PR99C	3	
AG2	PR99B	3	
AF2	PR99A	3	
AC8	PR98D	3	
AB8	PR98C	3	
AK1	PR98B	3	
AJ1	PR98A	3	
AB10	PR96D	3	
AA10	PR96C	3	
AF3	PR96B	3	
AE3	PR96A	3	
AE5	PR94D	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AY41	PB12A	5		PB13A	5	
BA41	PB12B	5		PB13B	5	
AT39	PB12C	5		PB13C	5	
AT38	PB12D	5		PB13D	5	
AV37	PB13A	5		PB15A	5	
AV36	PB13B	5		PB15B	5	
AM31	PB13C	5		PB15C	5	
AM32	PB13D	5		PB15D	5	
BA40	PB15A	5		PB16A	5	
BB40	PB15B	5		PB16B	5	
AM29	PB15C	5		PB16C	5	
AL29	PB15D	5		PB16D	5	
AY39	PB16A	5		PB17A	5	
AY38	PB16B	5		PB17B	5	
AN33	PB16C	5		PB17C	5	
AN32	PB16D	5		PB17D	5	
BA39	PB17A	5		PB19A	5	
BA38	PB17B	5		PB19B	5	
AT37	PB17C	5		PB19C	5	
AT36	PB17D	5		PB19D	5	
AW36	PB19A	5		PB20A	5	
AW35	PB19B	5		PB20B	5	
AM28	PB19C	5		PB20C	5	
AL28	PB19D	5		PB20D	5	
BB38	PB20A	5		PB21A	5	
BB39	PB20B	5		PB21B	5	
AR34	PB20C	5		PB21C	5	
AR33	PB20D	5		PB21D	5	
AV35	PB21A	5		PB23A	5	
AV34	PB21B	5		PB23B	5	
AT33	PB21C	5		PB23C	5	
AT34	PB21D	5		PB23D	5	
BA37	PB23A	5		PB25A	5	
BA36	PB23B	5		PB25B	5	
AP33	PB23C	5		PB25C	5	
AP32	PB23D	5		PB25D	5	
AY36	PB24A	5		PB26A	5	
AY35	PB24B	5		PB26B	5	
AN31	PB24C	5		PB26C	5	
AN30	PB24D	5		PB26D	5	
BB37	PB25A	5		PB27A	5	
BB36	PB25B	5		PB27B	5	
AP31	PB25C	5		PB27C	5	
AP30	PB25D	5		PB27D	5	
AV33	PB27A	5		PB29A	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL23	PB56D	5		PB58D	5	
AW24	PB57A	5		PB61A	5	
AW23	PB57B	5		PB61B	5	
AN23	PB57C	5		PB61C	5	
AP23	PB57D	5		PB61D	5	
AY23	PB59A	5		PB63A	5	
AY24	PB59B	5		PB63B	5	
AU23	PB59C	5		PB63C	5	
AU22	PB59D	5		PB63D	5	
AV23	PB60A	5		PB66A	5	
AV22	PB60B	5		PB66B	5	
AM22	PB60C	5		PB66C	5	
AL22	PB60D	5		PB66D	5	
BA23	PB61A	5		PB69A	5	
BA22	PB61B	5		PB69B	5	
AN22	PB61C	5		PB69C	5	
AP22	PB61D	5		PB69D	5	
BB23	PB63A	5		PB71A	5	
BB22	PB63B	5		PB71B	5	
AT22	PB63C	5		PB71C	5	
AR22	PB63D	5		PB71D	5	
BB21	PB65A	4		PB73A	4	
BB20	PB65B	4		PB73B	4	
AR21	PB65C	4		PB73C	4	
AT21	PB65D	4		PB73D	4	
BA21	PB66A	4		PB75A	4	
BA20	PB66B	4		PB75B	4	
AP21	PB66C	4		PB75C	4	
AN21	PB66D	4		PB75D	4	
AV21	PB67A	4		PB78A	4	
AV20	PB67B	4		PB78B	4	
AM21	PB67C	4		PB78C	4	
AL21	PB67D	4		PB78D	4	
AY20	PB69A	4		PB81A	4	
AY19	PB69B	4		PB81B	4	
AU21	PB69C	4		PB81C	4	
AU20	PB69D	4		PB81D	4	
AW20	PB70A	4		PB83A	4	
AW19	PB70B	4		PB83B	4	
AP20	PB70C	4		PB83C	4	
AN20	PB70D	4		PB83D	4	
BB19	PB71A	4		PB86A	4	
BB18	PB71B	4		PB86B	4	
AM20	PB71C	4		PB86C	4	
AL20	PB71D	4		PB86D	4	