Lattice Semiconductor Corporation - LFSCM3GA115EP1-5FC1152I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BCBGA, FCBGA
Supplier Device Package	1152-CFCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga115ep1-5fc1152i

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR 16x2 x 4 DPR 16x2 x 2	ROM 16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR 16x4 x 2 DPR 16x4 x 1	ROM 16x2 x 4
LUT 6x2 or MUX 8x1 x 2	2-bit Counter x 4	SPR 16x8 x 1	ROM 16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM 16x8 x1

Routing

There are many resources provided in the LatticeSC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

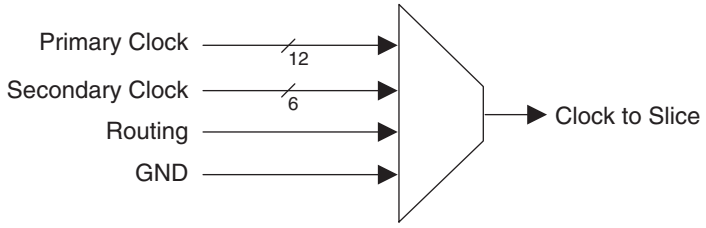
The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU) resources. The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. All connections are buffered to ensure high-speed operation even with long high-fanout connections.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Network

The LatticeSC devices have three distinct clock networks for use in distributing high-performance clocks within the device: primary clocks, secondary clocks and edge clocks. In addition to these dedicated clock networks, users are free to route clocks within the device using the general purpose routing. Figure 2-4 shows the clock resources available to each slice.

Figure 2-4. Slice Clock Selection



Note: GND is available to switch off the network.

Primary Clock Sources

LatticeSC devices have a wide variety of primary clock sources available. Primary clocks sources consists of the following:

- Primary clock input pins
- Edge clock input pins
- Two outputs per DLL

PURESPEED I/O Buffer Banks

LatticeSC devices have seven PURESPEED I/O buffer banks; each is capable of supporting multiple I/O standards. Each PURESPEED I/O bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-26 shows the seven banks and their associated supplies. Table 2-7 lists the maximum number of I/Os per bank for the whole LatticeSC family.

In the LatticeSC devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI33 and PCIX33) are powered using V_{CCIO}. In addition to the bank V_{CCIO} supplies, the LatticeSC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers. VCCAUX also powers a predriver of single-ended output buffers to enhance buffer performance.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeSC devices any I/O pin in a bank can be configured to be a dedicated reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Differential drivers have user selectable internal or external bias. External bias is brought in by the VREF1 pin in the bank. External bias for differential buffers is needed for applications that requires tighter than standard output common mode range.

Since a bank can have only one external bias circuit for differential drivers, LVDS and RSDS differential outputs can be mixed in a bank.

If a differential driver is configured in a bank, one pin in that bank becomes a DIFFR pin. This DIFFR pin must be connected to ground via an external 1K +/-1% ohm resistor. Note that differential drivers are not supported in banks 1, 4 and 5.

In addition, there are dedicated Terminating Supply (V_{TT}) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These V_{TT} pins are available in banks 2-7, these pins are not available in some packages. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.

There are further restrictions on the use of V_{TT} pins, for additional details refer to technical information at the end of this data sheet.

Table 2-10. Supported Output Standards[4]

Output Standard	Drive	V_{CCIO} (Nom)	On-chip Output Termination
Single-ended Interfaces			
LVTTL/D[1]	8mA, 16mA, 24mA	3.3	None.
LVCMOS33/D[1]	8mA, 16mA, 24mA	3.3	None
LVCMOS25/D[1, 2]	4mA, 8mA, 12mA, 16mA,	2.5	None, series: 25, 33, 50, 100
LVCMOS18/D[1, 2]	4mA, 8mA, 12mA, 16mA,	1.8	None, series: 25, 33, 50, 100
LVCMOS15/D[1, 2]	4mA, 8mA, 12mA, 16mA,	1.5	None, series: 25, 33, 50, 100
LVCMOS12/D[1, 2]	2mA, 4mA, 8mA, 12mA	1.2	None, series: 25, 33, 50, 100
PCIX15	N/A	1.5	None
PCI33, PCIX33, AGP1X33, AGP2X33	N/A	3.3	None
HSTL18_I	N/A	1.8	None, series: 50
HSTL18_II	N/A	1.8	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
HSTL15_I	N/A	1.5	None, series: 50
HSTL15_II	N/A	1.5	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
SSTL33_I	N/A	3.3	None
SSTL33_II	N/A	3.3	None
SSTL25_I	N/A	2.5	None, series: 50
SSTL25_II	N/A	2.5	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
SSTL18_ I	N/A	1.8	None, series: 33
SSTL18_II	N/A	1.8	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
Differential Interfaces			
SSTL18D_I	N/A	1.8	None, series: 33
SSTL25D_I	N/A	2.5	None, series: 50
SSTL18D_II, SSTL25D_II	N/A	1.2/2.5/3.3	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
SSTL33D_I, II	N/A	3.3	None
HSTL15D_I, HSTL18D_I	N/A	1.5/1.8	None, series: 50
HST15D_II, HSTL18D_II	N/A	1.5/1.8	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
LVDS	2mA, 3.5mA, 4mA, 6mA	N/A	None
Mini-LVDS	3.5mA, 4mA, 6mA	N/A	None
BLVDS25	N/A	N/A	None
MLVDS25	N/A	N/A	None
LVPECL33[3]	N/A	3.3	None
RSDS	2mA, 3.5mA, 4mA, 6mA	N/A	None

1. D refers to open drain capability.
2. User can select either drive current or driver impedances but not both.
3. Emulated with external resistors.
4. No GTL or GTL+ support.

PCI Clamp

A programmable PCI clamp is available on the top and bottom banks of the device. The PCI clamp can be turned “ON” or “OFF” on each pin independently. The PCI clamp is used when implementing a 3.3V PCI interface. The

this allows for easy integration with the rest of the system. These capabilities make the LatticeSC ideal for many multiple power supply and hot-swap applications. The maximum current during hot socketing is 4mA. See Hot Socketing Specifications in Chapter 3 of this data sheet.

Power-Up Requirements

To prevent high power supply and input pin currents, each VCC, VCC12, VCCAUX, VCCIO and VCCJ power supplies must have a monotonic ramp up time of 75 ms or less to reach its minimum operating voltage. Apart from VCC and VCC12, which have an additional requirement, and VCCIO and VCCAUX, which also have an additional requirement, the VCC, VCC12, VCCAUX, VCCIO and VCCJ power supplies can ramp up in any order, with no restriction on the time between them. However, the ramp time for each must be 75 ms or less. Configuration of the device will not proceed until the last power supply has reached its minimum operating voltage.

Additional Requirement for VCC and VCC12:
VCC12 must always be higher than VCC. This condition must be maintained at ALL times, including during power-up and power-down. Note that for 1.2V only operation, it is advisable to source both of these supplies from the same power supply.

Additional Requirement for VCCIO and VCCAUX:
If any VCCIOs are 1.2/1.5/1.8V, then VCCAUX MUST be applied before them. If any VCCIO is 1.2/1.5/1.8V and is powered up before VCCAUX, then when VCCAUX is powered up, it may drag VCCIO up with it as it crosses through the VCCIO value. (Note: If the VCCIO supply is capable of sinking current, as well as the more usual sourcing capability, this behavior is eliminated. However, the amount of current that the supply needs to sink is unknown and is likely to be in the hundreds of milliamps range).

Power-Down Requirements

To prevent high power supply and input pin currents, power must be removed monotonically from either VCC or VCCAUX (and must reach the power-down trip point of 0.5V for VCC, 0.95V for VCCAUX) before power is removed monotonically from VCC12, any of the VCCIOs, or VCCJ. Note that VCC12 can be removed at the same time as VCC, but it cannot be removed earlier. In many applications, VCC and VCC12 will be sourced from the same power supply and so will be removed together. For systems where disturbance of the user pins is a don't care condition, the power supplies can be removed in any order as long as they power down monotonically within 200ms of each other.

Additionally, if any banks have VCCIO=3.3V nominal (potentially banks 1, 4, 5) then VCCIO for those banks must not be lower than VCCAUX during power-down. The normal variation in ramp-up times of power supplies and voltage regulators is not a concern here.

Note: The SERDES power supplies are NOT included in these requirements and have no specific sequencing requirements. However, when using the SERDES with VDDIB or VDDOB that is greater than 1.2V (1.5V nominal for example), the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in the ramp-up times of power supplies and voltage regulators is not a concern here.

SERDES Power Supply Sequencing Requirements

When using the SERDES with 1.5V VDDIB or VDDOB supplies, the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and the 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in ramp-up times of power supples and voltage regulators is not a concern.

Additional Requirement for SERDES Power Supply
All VCC12 pins need to be connected on all devices independent of functionality used on the device. This analog supply is used by both the RX and TX portions of the SERDES and is used to control the core SERDES logic regardless of the SERDES being used in the design. VDDIB and VDDOB are used as supplies for the terminations on the CML input and output buffers. If a particular channel is not used, these can be UNCONNECTED (floating).

PURESPEED I/O Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 33	3.135	3.3	3.465	—	—	—
LVCMOS 25	2.375	2.5	2.625	—	—	—
LVCMOS 18	1.71	1.8	1.89	—	—	—
LVCMOS 15	1.425	1.5	1.575	—	—	—
LVCMOS 12	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
PCIX33	3.135	3.3	3.465	—	—	—
PCIX15	1.425	1.5	1.575	$0.49V_{CCIO}$	$0.5V_{CCIO}$	$0.51V_{CCIO}$
AGP1X33	3.135	3.3	3.465	—	—	—
AGP2X33	3.135	3.3	3.465	$0.39V_{CCIO}$	$0.4V_{CCIO}$	$0.41V_{CCIO}$
SSTL18_I, II[3]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II[3]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II[3]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I, II[3]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15_III[1, 3] and IV[1, 3]	1.425	1.5	1.575	0.68	0.9	0.9
HSTL 18_I[3], II[3]	1.71	1.8	1.89	0.816	0.9	1.08
HSTL 18_ III[1, 3], IV[1, 3]	1.71	1.8	1.89	0.816	1.08	1.08
GTL12[1, 3], GTLPLUS15[1, 3]	—	—	—	0.882	1.0	1.122
LVDS	—	—	—	—	—	—
Mini-LVDS	—	—	—	—	—	—
RSDS	—	—	—	—	—	—
LVPECL33 (outputs)[2]	3.135	3.3	3.465	—	—	—
LVPECL33 (inputs)[2, 4]	—	≤ 2.5	—	—	—	—
BLVDS25[2, 3]	2.375	2.5	2.625	—	—	—
MLVDS25[2, 3]	2.375	2.5	2.625	—	—	—
SSTL18D_I[3], II[3]	1.71	1.8	1.89	—	—	—
SSTL25D_I[3], II[3]	2.375	2.5	2.625	—	—	—
SSTL33D_I[3], II[3]	3.135	3.3	3.465	—	—	—
HSTL15D_I[3], II[3]	1.425	1.5	1.575	—	—	—
HSTL18D_I[3], II[3]	1.71	1.8	1.89	—	—	—

1. Input only.
2. Inputs on chip. Outputs are implemented with the addition of external resisters.
3. Input for this standard does not depend on the value of V_{CCIO}.
4. Inputs for this standard cannot be in 3.3V VCCIO banks (≤ 2.5V only).

Switching Characteristics

All devices are 100% functionally tested. Listed below are representative values of internal and external timing parameters. For more specific, more precise, and worst-case guaranteed data at a particular temperature and voltage, use the values reported by the static timing analyzer in the ispLEVER design tool from Lattice and back-annotate to the simulation net list.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2]

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F7	A_VDDAX25_L	-		A_VDDAX25_L	-	
B1	A_REFCLKP_L	-		A_REFCLKP_L	-	
C1	A_REFCLKN_L	-		A_REFCLKN_L	-	
D5	VCC12	-		VCC12	-	
A2	RESP_ULC	-		RESP_ULC	-	
E5	VCC12	-		VCC12	-	
D4	VCC12	-		VCC12	-	
H5	RESETN	1		RESETN	1	
H6	TSALLN	1		TSALLN	1	
G6	DONE	1		DONE	1	
G5	INITN	1		INITN	1	
F5	M0	1		M0	1	
F6	M1	1		M1	1	
F4	M2	1		M2	1	
E4	M3	1		M3	1	
D3	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
D2	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
J6	PL15C	7		PL16C	7	
J5	PL15D	7		PL16D	7	
E3	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
E2	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
K4	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
J4	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
F3	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
G3	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
K5	PL18C	7		PL18C	7	
K6	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F2	PL19A	7		PL22A	7	
F1	PL19B	7		PL22B	7	
E1	PL19C	7		PL22C	7	
D1	PL19D	7		PL22D	7	
K3	PL22A	7		PL25A	7	
L3	PL22B	7		PL25B	7	
L6	PL22C	7	VREF1_7	PL25C	7	VREF1_7
M6	PL22D	7	DIFFR_7	PL25D	7	DIFFR_7
J1	PL23A	7	PCLKT7_1	PL26A	7	PCLKT7_1
K1	PL23B	7	PCLKC7_1	PL26B	7	PCLKC7_1
L1	PL24A	7	PCLKT7_0	PL27A	7	PCLKT7_0
M1	PL24B	7	PCLKC7_0	PL27B	7	PCLKC7_0
P8	PL24C	7	PCLKT7_2	PL27C	7	PCLKT7_2
R8	PL24D	7	PCLKC7_2	PL27D	7	PCLKC7_2
N2	PL26A	6	PCLKT6_0	PL29A	6	PCLKT6_0
N1	PL26B	6	PCLKC6_0	PL29B	6	PCLKC6_0
R7	PL26C	6	PCLKT6_1	PL29C	6	PCLKT6_1
R6	PL26D	6	PCLKC6_1	PL29D	6	PCLKC6_1

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH29	PB48B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB68B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AE26	PB48C	4		PB68C	4	
AD25	PB48D	4		PB68D	4	
AJ30	PB49A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB69A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AH30	PB49B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB69B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AG28	PB49C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB69C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AG29	PB49D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB69D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF26	VCC12	-		VCC12	-	
AD27	PROBE_VCC	-		PROBE_VCC	-	
AG27	VCC12	-		VCC12	-	
AE28	PROBE_GND	-		PROBE_GND	-	
AC25	PR45D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR57D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AD26	PR45C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR57C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AF28	PR45B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR57B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AF29	PR45A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR57A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AC26	PR44D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR55D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AB26	PR44C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR55C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AG30	PR44B	3		PR55B	3	
AF30	PR44A	3		PR55A	3	
AC28	PR43B	3		PR52B	3	
AB28	PR43A	3		PR52A	3	
AB27	PR41D	3	VREF2_3	PR51D	3	VREF2_3
AE30	PR41B	3		PR51B	3	
AD30	PR41A	3		PR51A	3	
AB25	PR40B	3		PR49B	3	
AA25	PR40A	3		PR49A	3	
AA30	PR39B	3		PR48B	3	
Y30	PR39A	3		PR48A	3	
W29	PR37B	3		PR44B	3	
V29	PR37A	3		PR44A	3	
U30	PR36B	3		PR43B	3	
T30	PR36A	3		PR43A	3	
V25	PR35D	3	DIFFR_3	PR42D	3	DIFFR_3
W28	PR35B	3		PR42B	3	
V28	PR35A	3		PR42A	3	
R30	PR33B	3		PR38B	3	
P30	PR33A	3		PR38A	3	
N30	PR32B	3		PR35B	3	
M29	PR32A	3		PR35A	3	
U26	PR31D	3		PR34D	3	
T26	PR31C	3	VREF1_3	PR34C	3	VREF1_3
U28	PR31B	3		PR34B	3	
T28	PR31A	3		PR34A	3	
M30	PR28D	3	PCLKC3_2	PR31D	3	PCLKC3_2
L29	PR28C	3	PCLKT3_2	PR31C	3	PCLKT3_2

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB10	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
J10	VCC	-		VCC	-	
J21	VCC	-		VCC	-	
K10	VCC	-		VCC	-	
K11	VCC	-		VCC	-	
K12	VCC	-		VCC	-	
K13	VCC	-		VCC	-	
K14	VCC	-		VCC	-	
K17	VCC	-		VCC	-	
K18	VCC	-		VCC	-	
K19	VCC	-		VCC	-	
K20	VCC	-		VCC	-	
K21	VCC	-		VCC	-	
K22	VCC	-		VCC	-	
K9	VCC	-		VCC	-	
L10	VCC	-		VCC	-	
L21	VCC	-		VCC	-	
M10	VCC	-		VCC	-	
M21	VCC	-		VCC	-	
N10	VCC	-		VCC	-	
N21	VCC	-		VCC	-	
P10	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
U10	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V10	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W10	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y10	VCC	-		VCC	-	
Y21	VCC	-		VCC	-	
H11	VCCAUX	-		VCCAUX	-	
H12	VCCAUX	-		VCCAUX	-	
H19	VCCAUX	-		VCCAUX	-	
H20	VCCAUX	-		VCCAUX	-	
M23	VCCAUX	-		VCCAUX	-	
M24	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
N24	VCCAUX	-		VCCAUX	-	
U23	VCCAUX	-		VCCAUX	-	
U24	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	
V24	VCCAUX	-		VCCAUX	-	
W23	VCCAUX	-		VCCAUX	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AA7	VCCIO3	-		VCCIO3	-	
AB9	VCCIO3	-		VCCIO3	-	
AC4	VCCIO3	-		VCCIO3	-	
AD6	VCCIO3	-		VCCIO3	-	
AF3	VCCIO3	-		VCCIO3	-	
T3	VCCIO3	-		VCCIO3	-	
U4	VCCIO3	-		VCCIO3	-	
V6	VCCIO3	-		VCCIO3	-	
W10	VCCIO3	-		VCCIO3	-	
Y3	VCCIO3	-		VCCIO3	-	
AC11	VCCIO4	-		VCCIO4	-	
AD14	VCCIO4	-		VCCIO4	-	
AF15	VCCIO4	-		VCCIO4	-	
AF9	VCCIO4	-		VCCIO4	-	
AG12	VCCIO4	-		VCCIO4	-	
AJ13	VCCIO4	-		VCCIO4	-	
AJ7	VCCIO4	-		VCCIO4	-	
AK10	VCCIO4	-		VCCIO4	-	
AK16	VCCIO4	-		VCCIO4	-	
AK4	VCCIO4	-		VCCIO4	-	
AC19	VCCIO5	-		VCCIO5	-	
AD22	VCCIO5	-		VCCIO5	-	
AF21	VCCIO5	-		VCCIO5	-	
AG18	VCCIO5	-		VCCIO5	-	
AG24	VCCIO5	-		VCCIO5	-	
AJ17	VCCIO5	-		VCCIO5	-	
AJ23	VCCIO5	-		VCCIO5	-	
AJ30	VCCIO5	-		VCCIO5	-	
AK20	VCCIO5	-		VCCIO5	-	
AK26	VCCIO5	-		VCCIO5	-	
AA27	VCCIO6	-		VCCIO6	-	
AB23	VCCIO6	-		VCCIO6	-	
AC30	VCCIO6	-		VCCIO6	-	
AD26	VCCIO6	-		VCCIO6	-	
AF29	VCCIO6	-		VCCIO6	-	
T29	VCCIO6	-		VCCIO6	-	
U30	VCCIO6	-		VCCIO6	-	
V26	VCCIO6	-		VCCIO6	-	
W24	VCCIO6	-		VCCIO6	-	
Y29	VCCIO6	-		VCCIO6	-	
G30	VCCIO7	-		VCCIO7	-	
J27	VCCIO7	-		VCCIO7	-	
K29	VCCIO7	-		VCCIO7	-	
L24	VCCIO7	-		VCCIO7	-	
M26	VCCIO7	-		VCCIO7	-	
N30	VCCIO7	-		VCCIO7	-	
P23	VCCIO7	-		VCCIO7	-	
R27	VCCIO7	-		VCCIO7	-	
AA11	VCCAUX	-		VCCAUX	-	
AA12	VCCAUX	-		VCCAUX	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
U12	VCC12	-		VCC12	-	
U21	VCC12	-		VCC12	-	
AA16	VCC12	-		VCC12	-	
AA17	VCC12	-		VCC12	-	
M14	VCC12	-		VCC12	-	
P12	VCC12	-		VCC12	-	
W12	VCC12	-		VCC12	-	
AA14	VCC12	-		VCC12	-	
AA19	VCC12	-		VCC12	-	
W21	VCC12	-		VCC12	-	
P21	VCC12	-		VCC12	-	
M19	VCC12	-		VCC12	-	
A2	GND	-		GND	-	
A10	GND	-		GND	-	
E28	NC	-		NC	-	
E5	NC	-		NC	-	
F10	NC	-		NC	-	
E10	NC	-		NC	-	
E23	NC	-		NC	-	
F23	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M25 and LatticeSC/M40 in a 1020-pin package support a 16-bit MPI interface.

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD29	PL60D	6		PL84D	6	
AE31	PL61A	6		PL85A	6	
AF31	PL61B	6		PL85B	6	
AF30	PL61C	6		PL85C	6	
AF29	PL61D	6		PL85D	6	
AH33	PL62A	6		PL86A	6	
AJ33	PL62B	6		PL86B	6	
AC28	PL62C	6		PL86C	6	
AD28	PL62D	6		PL86D	6	
AH32	PL65A	6		PL89A	6	
AJ32	PL65B	6		PL89B	6	
AD27	PL65C	6		PL89C	6	
AE27	PL65D	6	VREF2_6	PL89D	6	VREF2_6
AG34	PL66A	6		PL90A	6	
AH34	PL66B	6		PL90B	6	
AC26	PL66C	6		PL90C	6	
AB26	PL66D	6		PL90D	6	
AK33	PL67A	6		PL91A	6	
AL33	PL67B	6		PL91B	6	
AG30	PL67C	6		PL91C	6	
AH30	PL67D	6		PL91D	6	
AL34	PL69A	6		PL93A	6	
AM34	PL69B	6		PL93B	6	
AJ30	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL93C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL93D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL70A	6		PL94A	6	
AH31	PL70B	6		PL94B	6	
AD26	PL70C	6		PL94C	6	
AD25	PL70D	6		PL94D	6	
AL32	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL95A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL95B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL95C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL95D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-		XRES	-	
AF27	TEMP	6		TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AN33	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AH29	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AJ29	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AM32	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AM31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AG27	PB4C	5		PB4C	5	
AG26	PB4D	5		PB4D	5	
AL29	PB5A	5		PB5A	5	
AL28	PB5B	5		PB5B	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH27	PB5C	5		PB5C	5	
AH26	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AN32	PB7A	5		PB7A	5	
AP32	PB7B	5		PB7B	5	
AF25	PB7C	5		PB7C	5	
AE25	PB7D	5		PB7D	5	
AN31	PB8A	5		PB9A	5	
AN30	PB8B	5		PB9B	5	
AK29	PB8C	5		PB9C	5	
AK28	PB8D	5		PB9D	5	
AP31	PB9A	5		PB11A	5	
AP30	PB9B	5		PB11B	5	
AD24	PB9C	5		PB11C	5	
AE24	PB9D	5		PB11D	5	
AM29	PB11A	5		PB13A	5	
AM28	PB11B	5		PB13B	5	
AJ27	PB11C	5		PB13C	5	
AJ26	PB11D	5		PB13D	5	
AP29	PB13A	5		PB15A	5	
AP28	PB13B	5		PB15B	5	
AK27	PB13C	5		PB15C	5	
AK26	PB13D	5		PB15D	5	
AN29	PB15A	5		PB17A	5	
AN28	PB15B	5		PB17B	5	
AG25	PB15C	5		PB17C	5	
AG24	PB15D	5		PB17D	5	
AL26	PB17A	5		PB19A	5	
AL25	PB17B	5		PB19B	5	
AG23	PB17C	5		PB19C	5	
AG22	PB17D	5		PB19D	5	
AN27	PB19A	5		PB21A	5	
AN26	PB19B	5		PB21B	5	
AF24	PB19C	5		PB21C	5	
AF23	PB19D	5		PB21D	5	
AP27	PB22A	5		PB24A	5	
AP26	PB22B	5		PB24B	5	
AK25	PB22C	5		PB24C	5	
AK24	PB22D	5		PB24D	5	
AN25	PB25A	5		PB27A	5	
AN24	PB25B	5		PB27B	5	
AE22	PB25C	5		PB27C	5	
AE21	PB25D	5		PB27D	5	
AM26	PB26A	5		PB29A	5	
AM25	PB26B	5		PB29B	5	
AF22	PB26C	5		PB29C	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB15	VCC12	-		VCC12	-	
AB20	VCC12	-		VCC12	-	
N15	VCC12	-		VCC12	-	
N20	VCC12	-		VCC12	-	
R13	VCC12	-		VCC12	-	
R22	VCC12	-		VCC12	-	
Y13	VCC12	-		VCC12	-	
Y22	VCC12	-		VCC12	-	
AA12	VCCAUX	-		VCCAUX	-	
AA23	VCCAUX	-		VCCAUX	-	
AB12	VCCAUX	-		VCCAUX	-	
AB16	VCCAUX	-		VCCAUX	-	
AB17	VCCAUX	-		VCCAUX	-	
AB18	VCCAUX	-		VCCAUX	-	
AB19	VCCAUX	-		VCCAUX	-	
AB23	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
Y19	GND	-		GND	-	
AC14	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC21	VCCAUX	-		VCCAUX	-	
AC22	VCCAUX	-		VCCAUX	-	
AC23	VCCAUX	-		VCCAUX	-	
M13	VCCAUX	-		VCCAUX	-	
M14	VCCAUX	-		VCCAUX	-	
M18	VCCAUX	-		VCCAUX	-	
M21	VCCAUX	-		VCCAUX	-	
M22	VCCAUX	-		VCCAUX	-	
N12	VCCAUX	-		VCCAUX	-	
N16	VCCAUX	-		VCCAUX	-	
N17	VCCAUX	-		VCCAUX	-	
N18	VCCAUX	-		VCCAUX	-	
N19	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
P12	VCCAUX	-		VCCAUX	-	
P23	VCCAUX	-		VCCAUX	-	
T13	VCCAUX	-		VCCAUX	-	
T22	VCCAUX	-		VCCAUX	-	
U12	VCCAUX	-		VCCAUX	-	
U13	VCCAUX	-		VCCAUX	-	
U22	VCCAUX	-		VCCAUX	-	
V13	VCCAUX	-		VCCAUX	-	
V22	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
D9	B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-	
E9	B_VDDIB3_R	-	
L13	VCC12	-	
J11	B_REFCLKN_R	-	
H11	B_REFCLKP_R	-	
M15	PT93D	1	HDC/SI
M16	PT93C	1	LDCN/SCS
F14	PT93B	1	D8/MPI_DATA8
G14	PT93A	1	CS1/MPI_CS1
L15	PT90D	1	D9/MPI_DATA9
L14	PT90C	1	D10/MPI_DATA10
D14	PT90B	1	CS0N/MPI_CS0N
E14	PT90A	1	RDN/MPI_STRB_N
L16	PT89D	1	WRN/MPI_WR_N
K16	PT89C	1	D7/MPI_DATA7
G15	PT89B	1	D6/MPI_DATA6
F15	PT89A	1	D5/MPI_DATA5
K14	PT87D	1	D4/MPI_DATA4
K13	PT87C	1	D3/MPI_DATA3
B15	PT87B	1	D2/MPI_DATA2
A15	PT87A	1	D1/MPI_DATA1
J14	PT86D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT86C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT86B	1	D0/MPI_DATA0
B16	PT86A	1	QOUT/CEON
J13	PT83D	1	VREF2_1
H13	PT83C	1	D18/MPI_DATA18
D15	PT83B	1	DOUT
E15	PT83A	1	MCA_DONE_IN
J16	PT81D	1	D19/PCLKC1_2/MPI_DATA19

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
W7	GND	-	
AA14	VCC	-	
AA16	VCC	-	
AA17	VCC	-	
AA18	VCC	-	
AA19	VCC	-	
AA21	VCC	-	
AB13	VCC	-	
AB22	VCC	-	
N13	VCC	-	
N22	VCC	-	
P14	VCC	-	
P16	VCC	-	
P17	VCC	-	
P18	VCC	-	
P19	VCC	-	
P21	VCC	-	
R15	VCC	-	
R17	VCC	-	
R18	VCC	-	
R20	VCC	-	
T14	VCC	-	
T16	VCC	-	
T19	VCC	-	
T21	VCC	-	
U14	VCC	-	
U15	VCC	-	
U17	VCC	-	
U18	VCC	-	
U20	VCC	-	
U21	VCC	-	
V14	VCC	-	
V15	VCC	-	
V17	VCC	-	
V18	VCC	-	
V20	VCC	-	
V21	VCC	-	
W14	VCC	-	
W16	VCC	-	
W19	VCC	-	
W21	VCC	-	
Y15	VCC	-	
Y17	VCC	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F5	VCC12	-		VCC12	-	
B14	C_HDOUTP3_R	-	PCS 3E2 CH 3 OUT P	C_HDOUTP3_R	-	PCS 3E2 CH 3 OUT P
E13	C_HDINN3_R	-	PCS 3E2 CH 3 IN N	C_HDINN3_R	-	PCS 3E2 CH 3 IN N
D13	C_HDINP3_R	-	PCS 3E2 CH 3 IN P	C_HDINP3_R	-	PCS 3E2 CH 3 IN P
F12	VCC12	-		VCC12	-	
G14	C_VDDIB3_R	-		C_VDDIB3_R	-	
F11	VCC12	-		VCC12	-	
K15	C_REFCLKN_R	-		C_REFCLKN_R	-	
J15	C_REFCLKP_R	-		C_REFCLKP_R	-	
G15	VCC12	-		VCC12	-	
H16	D_VDDIB0_R	-		D_VDDIB0_R	-	
D14	D_HDINP0_R	-	PCS 3E3 CH 0 IN P	D_HDINP0_R	-	PCS 3E3 CH 0 IN P
E14	D_HDINN0_R	-	PCS 3E3 CH 0 IN N	D_HDINN0_R	-	PCS 3E3 CH 0 IN N
F6	VCC12	-		VCC12	-	
B15	D_HDOUTP0_R	-	PCS 3E3 CH 0 OUT P	D_HDOUTP0_R	-	PCS 3E3 CH 0 OUT P
M13	D_VDDOB0_R	-		D_VDDOB0_R	-	
A15	D_HDOUTN0_R	-	PCS 3E3 CH 0 OUT N	D_HDOUTN0_R	-	PCS 3E3 CH 0 OUT N
F8	D_VDDOB1_R	-		D_VDDOB1_R	-	
A16	D_HDOUTN1_R	-	PCS 3E3 CH 1 OUT N	D_HDOUTN1_R	-	PCS 3E3 CH 1 OUT N
F7	VCC12	-		VCC12	-	
B16	D_HDOUTP1_R	-	PCS 3E3 CH 1 OUT P	D_HDOUTP1_R	-	PCS 3E3 CH 1 OUT P
F15	D_HDINN1_R	-	PCS 3E3 CH 1 IN N	D_HDINN1_R	-	PCS 3E3 CH 1 IN N
E15	D_HDINP1_R	-	PCS 3E3 CH 1 IN P	D_HDINP1_R	-	PCS 3E3 CH 1 IN P
K17	VCC12	-		VCC12	-	
F13	D_VDDIB1_R	-		D_VDDIB1_R	-	
C14	VCC12	-		VCC12	-	
C15	D_VDDIB2_R	-		D_VDDIB2_R	-	
D16	D_HDINP2_R	-	PCS 3E3 CH 2 IN P	D_HDINP2_R	-	PCS 3E3 CH 2 IN P
E16	D_HDINN2_R	-	PCS 3E3 CH 2 IN N	D_HDINN2_R	-	PCS 3E3 CH 2 IN N
C11	VCC12	-		VCC12	-	
B17	D_HDOUTP2_R	-	PCS 3E3 CH 2 OUT P	D_HDOUTP2_R	-	PCS 3E3 CH 2 OUT P
C9	D_VDDOB2_R	-		D_VDDOB2_R	-	
A17	D_HDOUTN2_R	-	PCS 3E3 CH 2 OUT N	D_HDOUTN2_R	-	PCS 3E3 CH 2 OUT N
D17	D_VDDOB3_R	-		D_VDDOB3_R	-	
A18	D_HDOUTN3_R	-	PCS 3E3 CH 3 OUT N	D_HDOUTN3_R	-	PCS 3E3 CH 3 OUT N
C17	VCC12	-		VCC12	-	
B18	D_HDOUTP3_R	-	PCS 3E3 CH 3 OUT P	D_HDOUTP3_R	-	PCS 3E3 CH 3 OUT P
F17	D_HDINN3_R	-	PCS 3E3 CH 3 IN N	D_HDINN3_R	-	PCS 3E3 CH 3 IN N
E17	D_HDINP3_R	-	PCS 3E3 CH 3 IN P	D_HDINP3_R	-	PCS 3E3 CH 3 IN P
F14	VCC12	-		VCC12	-	
F16	D_VDDIB3_R	-		D_VDDIB3_R	-	
G16	VCC12	-		VCC12	-	
M17	D_REFCLKN_R	-		D_REFCLKN_R	-	
L17	D_REFCLKP_R	-		D_REFCLKP_R	-	
G18	PT77D	1	HDC/SI	PT93D	1	HDC/SI

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB25	VCC	-		VCC	-	
AB26	VCC	-		VCC	-	
AC16	VCC	-		VCC	-	
AC18	VCC	-		VCC	-	
AC20	VCC	-		VCC	-	
AC23	VCC	-		VCC	-	
AC25	VCC	-		VCC	-	
AC27	VCC	-		VCC	-	
AD17	VCC	-		VCC	-	
AD19	VCC	-		VCC	-	
AD21	VCC	-		VCC	-	
AD22	VCC	-		VCC	-	
AD24	VCC	-		VCC	-	
AD26	VCC	-		VCC	-	
AE16	VCC	-		VCC	-	
AE18	VCC	-		VCC	-	
AE20	VCC	-		VCC	-	
AE21	VCC	-		VCC	-	
AE22	VCC	-		VCC	-	
AE23	VCC	-		VCC	-	
AE25	VCC	-		VCC	-	
AE27	VCC	-		VCC	-	
AF17	VCC	-		VCC	-	
AF19	VCC	-		VCC	-	
AF21	VCC	-		VCC	-	
AF22	VCC	-		VCC	-	
AF24	VCC	-		VCC	-	
AF26	VCC	-		VCC	-	
AG18	VCC	-		VCC	-	
AG20	VCC	-		VCC	-	
AG23	VCC	-		VCC	-	
AG25	VCC	-		VCC	-	
T18	VCC	-		VCC	-	
T20	VCC	-		VCC	-	
T23	VCC	-		VCC	-	
T25	VCC	-		VCC	-	
U17	VCC	-		VCC	-	
U19	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
U22	VCC	-		VCC	-	
U24	VCC	-		VCC	-	
U26	VCC	-		VCC	-	
V16	VCC	-		VCC	-	
V18	VCC	-		VCC	-	
V20	VCC	-		VCC	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-7FF1020C[1]	-7	Organic fcBGA	1020	COM	40.4
LFSC3GA40E-6FF1020C[1]	-6	Organic fcBGA	1020	COM	40.4
LFSC3GA40E-5FF1020C[1]	-5	Organic fcBGA	1020	COM	40.4
LFSC3GA40E-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-7FC1152C[2]	-7	Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-6FC1152C[2]	-6	Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-5FC1152C[2]	-5	Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-7FF1152C	-7	Organic fcBGA	1152	COM	40.4
LFSC3GA40E-6FF1152C	-6	Organic fcBGA	1152	COM	40.4
LFSC3GA40E-5FF1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-7FF1020C[1]	-7	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-6FF1020C[1]	-6	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-5FF1020C[1]	-5	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-7FC1152C[2]	-7	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FC1152C[2]	-6	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FC1152C[2]	-5	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-7FF1152C	-7	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FF1152C	-6	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FF1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C[1]	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C[1]	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C[1]	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C[1]	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.