Lattice Semiconductor Corporation - LFSCM3GA115EP1-5FC1704C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	942
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BCBGA, FCBGA
Supplier Device Package	1704-CFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga115ep1-5fc1704c

Figure 2-1. Simplified Block Diagram (Top Level)

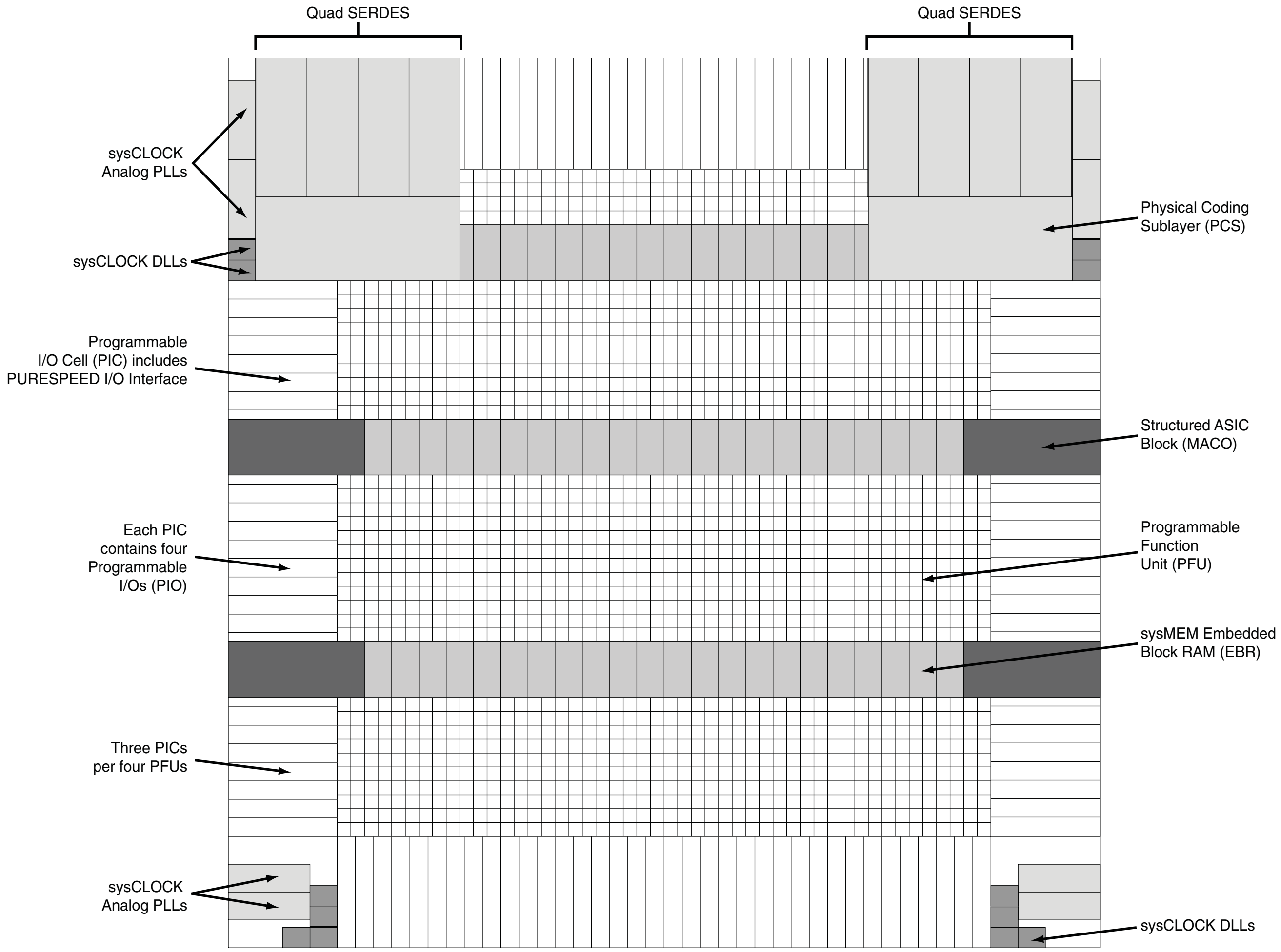


Figure 2-3. Slice Diagram

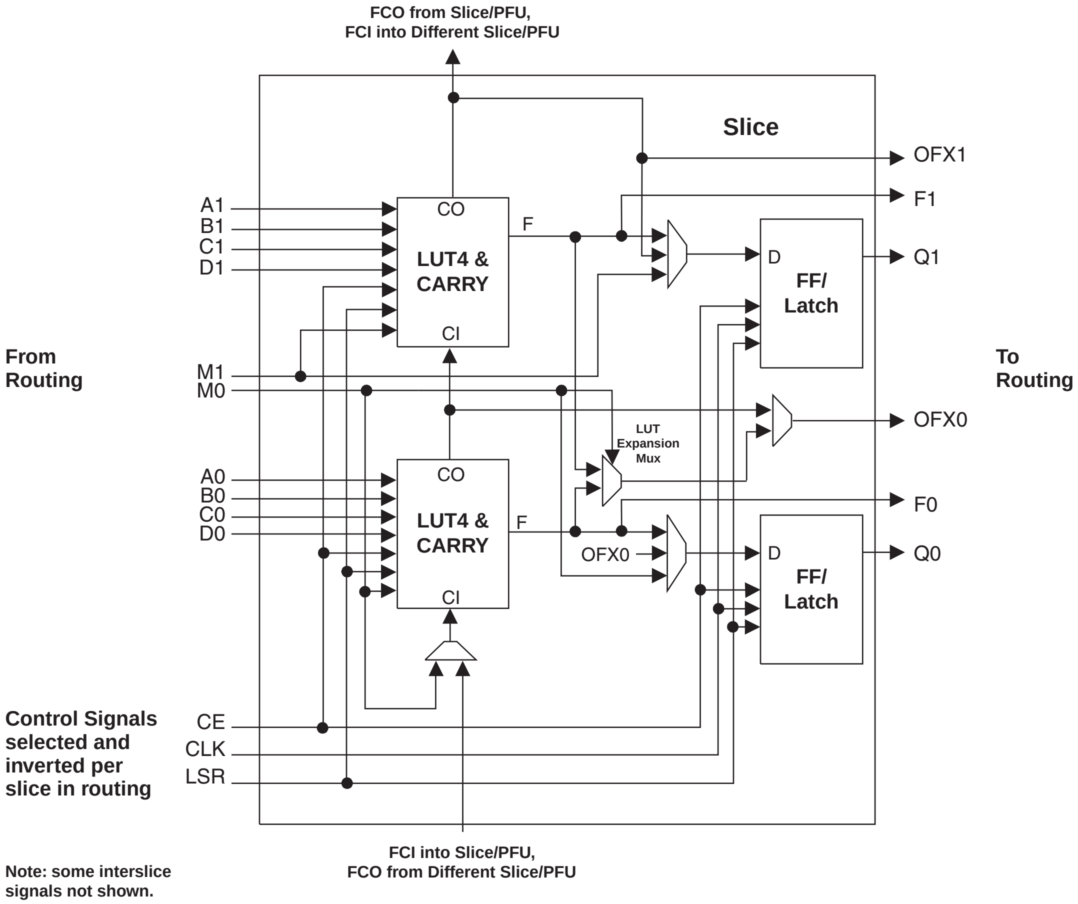


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[2]

1. See Figure 2-2 for connection details.
2. Requires two PFUs.

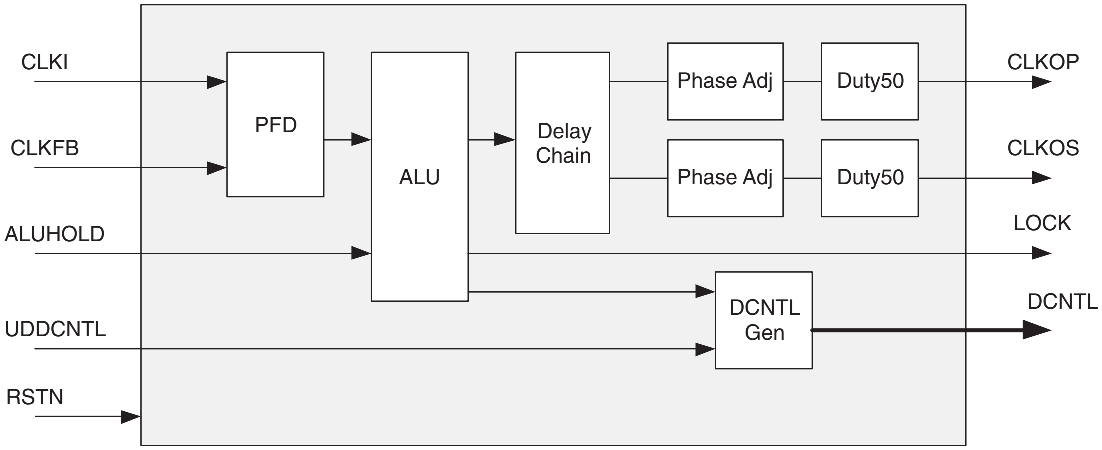
There is a Digital Control (DCNTL) bus available from the DLL block. This Digital Control bus is available to the delay lines in the PIC blocks in the adjacent banks. The UDDCNTL signal allows the user to latch the current value on the digital control bus.

Figure 2-12 shows the DLL block diagram of the DLL inputs and outputs. The output of the phase frequency detector controls an arithmetic logic unit (ALU) to add or subtract one delay tap. The digital output of this ALU is used to control the delay value of the delay chain and this digital code is transmitted via the DCNTL bus.

The sysCLOCK DLL can be configured at power-up, then, if desired, reconfigured dynamically through the Serial Memory Interface bus which interfaces with the on-chip Microprocessor Interface (MPI) bus. In addition, users can drive the SMI interface from routing if desired.

The user can configure the DLL for many common functions such as clock injection match and single delay cell. Lattice provides primitives in its design for time reference delay (DDR memory) and clock injection delay removal.

Figure 2-12. DLL Diagram



PLL/DLL Cascading

The LatticeSC devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are as follows:

- PLL to PLL
- PLL to DLL
- DLL to DLL
- DLL to PLL

DLLs are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLL and PLLs.

When cascading the DLL to the PLL, the DLL can be used to drive the PLL to create fine phase shifts of an input clock signal. Figure 2-13 shows a shift of all outputs for CLKOP and CLKOS out in time.

PURESPEED I/O Buffer Banks

LatticeSC devices have seven PURESPEED I/O buffer banks; each is capable of supporting multiple I/O standards. Each PURESPEED I/O bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-26 shows the seven banks and their associated supplies. Table 2-7 lists the maximum number of I/Os per bank for the whole LatticeSC family.

In the LatticeSC devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI33 and PCIX33) are powered using V_{CCIO}. In addition to the bank V_{CCIO} supplies, the LatticeSC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers. VCCAUX also powers a predriver of single-ended output buffers to enhance buffer performance.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeSC devices any I/O pin in a bank can be configured to be a dedicated reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Differential drivers have user selectable internal or external bias. External bias is brought in by the VREF1 pin in the bank. External bias for differential buffers is needed for applications that requires tighter than standard output common mode range.

Since a bank can have only one external bias circuit for differential drivers, LVDS and RSDS differential outputs can be mixed in a bank.

If a differential driver is configured in a bank, one pin in that bank becomes a DIFFR pin. This DIFFR pin must be connected to ground via an external 1K +/-1% ohm resistor. Note that differential drivers are not supported in banks 1, 4 and 5.

In addition, there are dedicated Terminating Supply (V_{TT}) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These V_{TT} pins are available in banks 2-7, these pins are not available in some packages. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.

There are further restrictions on the use of V_{TT} pins, for additional details refer to technical information at the end of this data sheet.

Table 2-10. Supported Output Standards[4]

Output Standard	Drive	V_{CCIO} (Nom)	On-chip Output Termination
Single-ended Interfaces			
LVTTL/D[1]	8mA, 16mA, 24mA	3.3	None.
LVCMOS33/D[1]	8mA, 16mA, 24mA	3.3	None
LVCMOS25/D[1, 2]	4mA, 8mA, 12mA, 16mA,	2.5	None, series: 25, 33, 50, 100
LVCMOS18/D[1, 2]	4mA, 8mA, 12mA, 16mA,	1.8	None, series: 25, 33, 50, 100
LVCMOS15/D[1, 2]	4mA, 8mA, 12mA, 16mA,	1.5	None, series: 25, 33, 50, 100
LVCMOS12/D[1, 2]	2mA, 4mA, 8mA, 12mA	1.2	None, series: 25, 33, 50, 100
PCIX15	N/A	1.5	None
PCI33, PCIX33, AGP1X33, AGP2X33	N/A	3.3	None
HSTL18_I	N/A	1.8	None, series: 50
HSTL18_II	N/A	1.8	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
HSTL15_I	N/A	1.5	None, series: 50
HSTL15_II	N/A	1.5	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
SSTL33_I	N/A	3.3	None
SSTL33_II	N/A	3.3	None
SSTL25_I	N/A	2.5	None, series: 50
SSTL25_II	N/A	2.5	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
SSTL18_ I	N/A	1.8	None, series: 33
SSTL18_II	N/A	1.8	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
Differential Interfaces			
SSTL18D_I	N/A	1.8	None, series: 33
SSTL25D_I	N/A	2.5	None, series: 50
SSTL18D_II, SSTL25D_II	N/A	1.2/2.5/3.3	None, series: 33, series + parallel to V_{CCIO}/2: 33+ 60
SSTL33D_I, II	N/A	3.3	None
HSTL15D_I, HSTL18D_I	N/A	1.5/1.8	None, series: 50
HST15D_II, HSTL18D_II	N/A	1.5/1.8	None, series: 25, series + parallel to V_{CCIO}/2: 25 + 60
LVDS	2mA, 3.5mA, 4mA, 6mA	N/A	None
Mini-LVDS	3.5mA, 4mA, 6mA	N/A	None
BLVDS25	N/A	N/A	None
MLVDS25	N/A	N/A	None
LVPECL33[3]	N/A	3.3	None
RSDS	2mA, 3.5mA, 4mA, 6mA	N/A	None

1. D refers to open drain capability.
2. User can select either drive current or driver impedances but not both.
3. Emulated with external resistors.
4. No GTL or GTL+ support.

PCI Clamp

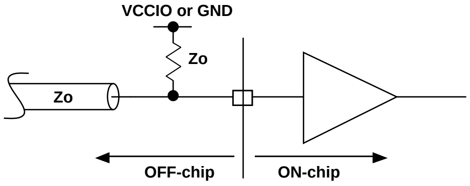
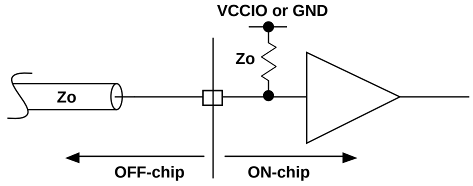
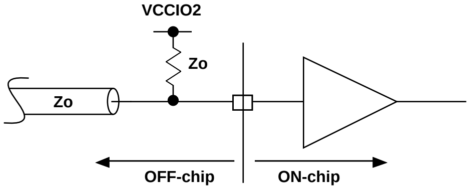
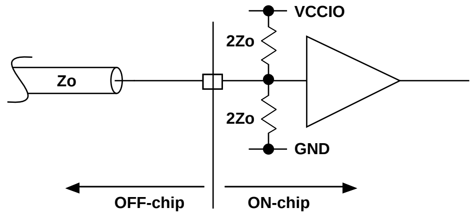
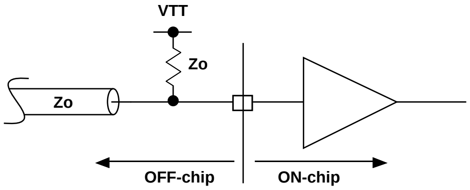
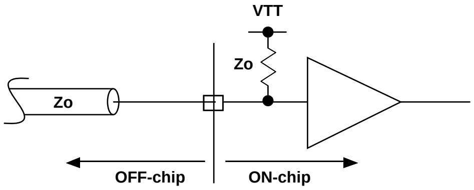
A programmable PCI clamp is available on the top and bottom banks of the device. The PCI clamp can be turned “ON” or “OFF” on each pin independently. The PCI clamp is used when implementing a 3.3V PCI interface. The

Single Ended Inputs: The SC devices support a number of different termination schemes for single ended inputs:

- Parallel to V_{CCIO} or GND
- Parallel to $V_{CCIO}/2$
- Parallel to V_{TT}

Figure 2-28 shows the single ended input schemes that are supported. The nominal values of the termination resistors are shown in Table 2-9.

Figure 2-28. Input Termination Schemes

Termination Type	Discrete Off-Chip Solution	Lattice On-Chip Solution
Parallel termination to to V_{CCIO}, or parallel to GND receiving end		
Parallel termination to $V_{CCIO}/2$ receiving end		
Parallel termination to V_{TT} at receiving end		

In many situations designers can chose whether to use Thevenin or parallel to V_{TT} termination. The Thevenin approach has the benefit of not requiring a termination voltage to be applied to the device. The parallel to V_{TT} approach consumes less power.

VTT Termination Resources

Each I/O bank, except bank 1, has a number of V_{TT} pins that must be connected if V_{TT} is used. Note V_{TT} pins can sink or source current and the power supply they are connected to must be able to handle the relatively high currents associated with the termination circuits. Note: V_{TT} is not available in all package styles.

On-chip parallel termination to V_{TT} is supported at the receiving end only. On-chip parallel output termination to V_{TT} is not supported.

The V_{TT} internal bus is also connected to the internal V_{CMT} node. Thus in one bank designers can implement either V_{TT} termination or V_{CMT} termination for differential inputs.

DDRII/RLDRAMII Termination Support

The DDR II memory and RLDRAMII (in Bidirection Data mode) standards require that the on-chip termination to V_{TT} be turned on when a pin is an input and off when the pin is an output. The LatticeSC devices contain the required circuitry to support this behavior. For additional detail refer to technical information at the end of the data sheet.

VDDAX25 needs to be connected independent of the use of the SERDES. This supply is used to control the SERDES CML I/O regardless of the SERDES being used in the design.

Supported Source Synchronous Interfaces

The LatticeSC devices contain a variety of hardware, such as delay elements, DDR registers and PLLs, to simplify the implementation of Source Synchronous interfaces. Table 2-11 lists Source Synchronous and DDR/QDR standards supported in the LatticeSC. For additional detail refer to technical information at the end of the data sheet.

Table 2-11. Source Synchronous Standards Table[1]

Source Synchronous Standard	Clocking	Speeds (MHz)	Data Rate (Mbps)
RapidIO	DDR	500	1000
SPI4.2 (POS-PHY4)/NPSI	DDR	500	1000
SFI4/XSBI	DDR SDR	334 667	667
XGMII	DDR	156.25	312
CSIX	SDR	250	250
QDRII/QDRII+ memory interface	DDR	300	600
DDR memory interface	DDR	240	480
DDRII memory interface	DDR	333	667
RLDRAM memory interface	DDR	400	800

1. Memory width is dependent on the system design and limited by the number of I/Os in the device.

flexiPCS™ (Physical Coding Sublayer Block)

flexiPCS Functionality

The LatticeSC family combines a high-performance FPGA fabric, high-performance I/Os and large embedded RAM in a single industry leading architecture. LatticeSC devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES for high-speed, full-duplex serial data transfers at data rates up to 3.8 Gbps. The PCS logic in each channel can be configured to support an array of popular data protocols including SONET (STS-12/STS-12c, STS-48/STS-48c, and TFI-5 support of 10 Gbps or above), Gigabit Ethernet (compliant to the IEEE 1000BASE-X specification), 1.02 or 2.04 Gbps Fibre Channel, PCI-Express, and Serial RapidIO. In addition, the protocol based logic can be fully or partially bypassed in a number of configurations to allow users flexibility in designing their own high-speed data interface.

Protocols requiring data rates above 3.8 Gbps can be accommodated by dedicating either one pair or all four channels in one flexiPCS quad block to one data link. One quad can support full-duplex serial data transfers at data rates up to 15.2 Gbps. A single flexiPCS quad can be configured to support 10Gb Ethernet (with a fully compliant XAUI interface), 10Gb Fibre Channel, and x4 PCI-Express and 4x RapidIO.

The flexiPCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic which can also be geared to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Each SERDES pin can be DC coupled independently and can allow for both high-speed and low-speed operation down to DC rates on the same SERDES pin, as required by some Serial Digital Video applications.

The ispLEVER design tools from Lattice support all modes of the flexiPCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow a user to define their own operation. With ispLEVER, the user can define the mode for each quad in a design. Nine modes are currently supported by the ispLEVER design flow:

Power Supply Ramp Rates

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
t_{RAMP}	Power supply ramp rates for all power supplies	Over process, voltage, temperature	3.45	—	—	mV/µs
			—	—	75	ms

1. See the Power-up and Power-Down requirements section for more details on power sequencing.
2. From 0.5V to minimum operating voltage.

Hot Socketing Specifications[1]

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Programmable and dedicated Input or I/O leakage current[2, 3, 4, 5, 6]	$0 <= V_{IN} <= V_{IH}$ (MAX)	—	—	±1500	µA
I_{HDIN}	SERDES average input current when device powered down and inputs driven[7]		—	—	4	mA

1. See Hot Socket power up/down information in Chapter 2 of this document.
2. Assumes monotonic rise/fall rates for all power supplies.
3. Sensitive to power supply sequencing as described in hot socketing section.
4. Assumes power supplies are between 0 and maximum recommended operations conditions.
5. IDK is additive to I_{PU}, I_{PD} or I_{BH}.
6. Represents DC conditions. For the first 20ns after hot insertion, current specification is 8 mA.
7. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed VDDOB of 1.575V, 8b/10b data and internal AC coupling.

DC Electrical Characteristics[5]

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.[3]	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low leakage	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7\ V_{CCIO}$	-30	—	-210	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\leq V_{IN} \leq V_{IH}$ (MAX)	30	—	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	210	µA
I_{BHLH}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	-210	µA
I_{CL}	PCI Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$	—	—	mA
I_{CH}	PCI High Clamp Current	$V_{CC} + 4 > V_{IN} \geq V_{CC} + 1$	$25 + (V_{IN} - V_{CC} -1)/0.015$	—	—	mA
V_{BHT}	Bus Hold trip Points	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{CCIP2} = 1.2V, V_{CCAUX} = 2.5, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C3[2]	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{CCIP2} = 1.2V, V_{CCAUX} = 2.5, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. I_{PU}, I_{PD}, I_{BHLS} and I_{BHHS} have minimum values of 15 or -15µA if V_{CCIO} is set to 1.2V nominal.
4. This table does not apply to SERDES pins.
5. For programmable I/Os.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

MLVDS

The LatticeSC devices support the MLVDS standard. This industry standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. MLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-1 is one possible solution for bi-directional multi-point differential signals.

Figure 3-1. MLVDS Multi-Point Output Example

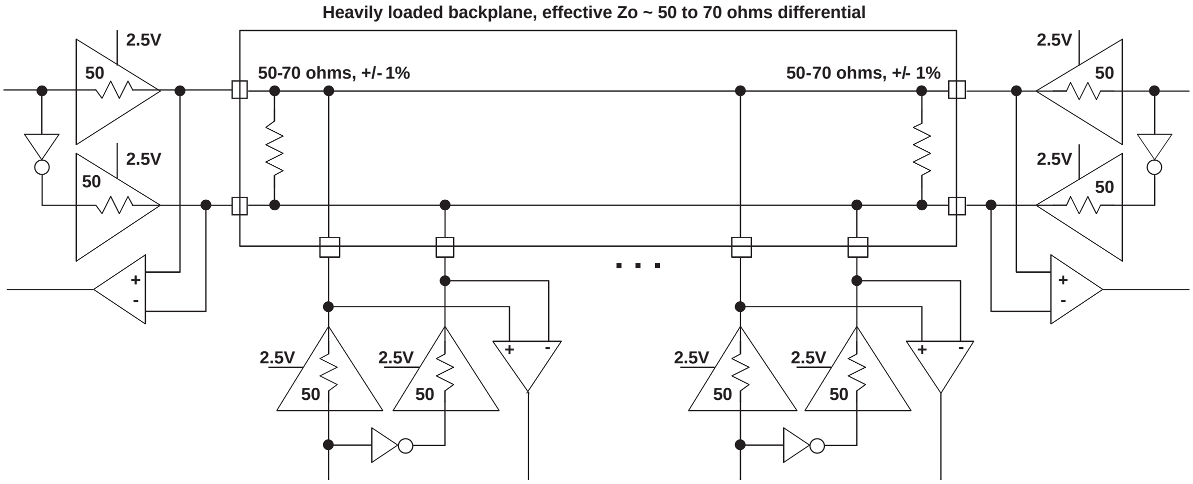


Table 3-1. MLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 50	Zo = 70	
Z_{OUT}	Output impedance	50	50	ohm
R_{TLEFT}	Left end termination	50	70	ohm
R_{TRIGHT}	Right end termination	50	70	ohm
V_{OH}	Output high voltage	1.50	1.575	V
V_{OL}	Output low voltage	1.00	0.925	V
V_{OD}	Output differential voltage	0.50	0.65	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	20.0	18.5	mA

1. For input buffer, see LVDS table.

Figure 3-8. Read Mode with Input and Output Registers

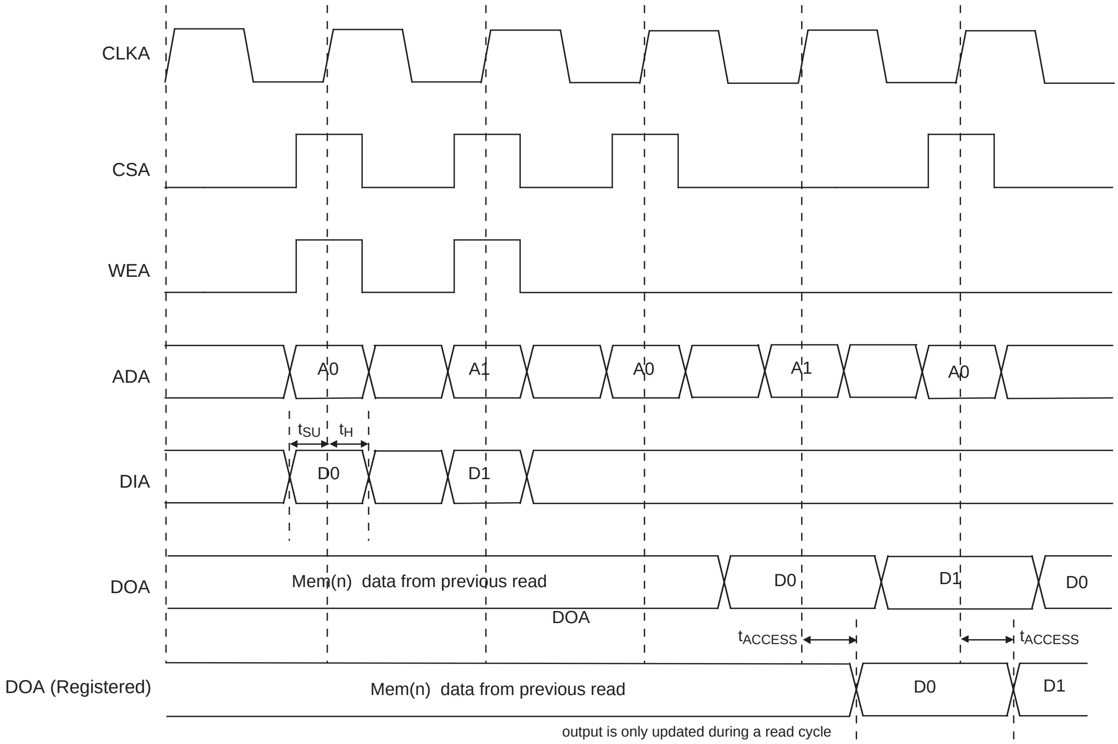
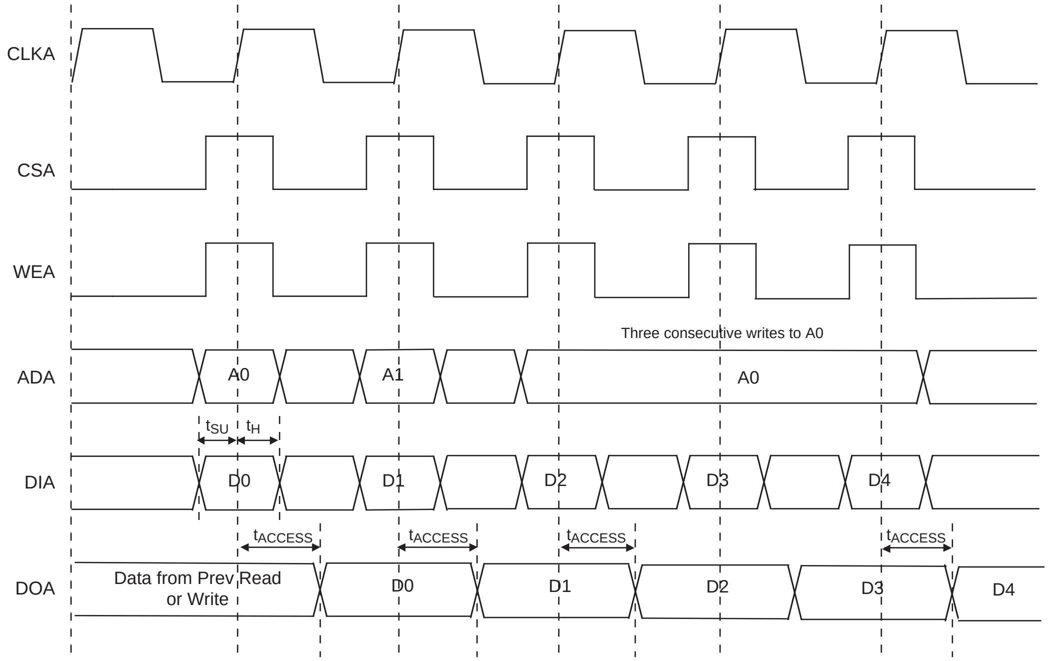


Figure 3-9. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

	LFSC/M15		
Ball Number	Ball Function	VCCIO Bank	Dual Function
M4	PL43B	6	
P1	PL45A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
R1	PL45B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
R2	XRES	-	
P3	TEMP	6	
R3	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
N4	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
T3	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
T2	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
N5	PB5D	5	VREF1_5
P5	PB8A	5	
R5	PB8B	5	
T4	PB9A	5	
T5	PB9B	5	
R6	PB12A	5	PCLKT5_3
T6	PB12B	5	PCLKC5_3
L5	PB13C	5	
P6	PB15A	5	PCLKT5_0
T7	PB15B	5	PCLKC5_0
M7	PB15D	5	VREF2_5
R8	PB16A	5	PCLKT5_1
T8	PB16B	5	PCLKC5_1
N7	PB17A	5	PCLKT5_2
N8	PB17B	5	PCLKC5_2
R9	PB20A	5	
T9	PB20B	5	
M8	PB21A	5	
M9	PB21B	5	
P8	PB24A	5	
P9	PB24B	5	
T10	PB28A	4	
R11	PB28B	4	
N9	PB31A	4	
N10	PB31B	4	
T11	PB32A	4	
R12	PB32B	4	
P11	PB35A	4	PCLKT4_2
M10	PB35B	4	PCLKC4_2
T12	PB36A	4	PCLKT4_1
P12	PB36B	4	PCLKC4_1
T13	PB37A	4	PCLKT4_0
T14	PB37B	4	PCLKC4_0
R15	PB37C	4	VREF2_4

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y9	VCCIO6	-		VCCIO6	-	
J7	VCCIO7	-		VCCIO7	-	
J8	VCCIO7	-		VCCIO7	-	
K7	VCCIO7	-		VCCIO7	-	
K8	VCCIO7	-		VCCIO7	-	
L8	VCCIO7	-		VCCIO7	-	
L9	VCCIO7	-		VCCIO7	-	
M9	VCCIO7	-		VCCIO7	-	
N9	VCCIO7	-		VCCIO7	-	
P9	VCCIO7	-		VCCIO7	-	
R9	VCCIO7	-		VCCIO7	-	
A1	GND	-		GND	-	
A30	GND	-		GND	-	
AA15	GND	-		GND	-	
AA16	GND	-		GND	-	
AK1	GND	-		GND	-	
AK30	GND	-		GND	-	
K15	GND	-		GND	-	
K16	GND	-		GND	-	
L11	GND	-		GND	-	
L12	GND	-		GND	-	
L13	GND	-		GND	-	
L14	GND	-		GND	-	
L15	GND	-		GND	-	
L16	GND	-		GND	-	
L17	GND	-		GND	-	
L18	GND	-		GND	-	
L19	GND	-		GND	-	
L20	GND	-		GND	-	
M11	GND	-		GND	-	
M12	GND	-		GND	-	
M13	GND	-		GND	-	
M14	GND	-		GND	-	
M15	GND	-		GND	-	
M16	GND	-		GND	-	
M17	GND	-		GND	-	
M18	GND	-		GND	-	
M19	GND	-		GND	-	
M20	GND	-		GND	-	
N11	GND	-		GND	-	
N12	GND	-		GND	-	
N13	GND	-		GND	-	
N14	GND	-		GND	-	
N15	GND	-		GND	-	
N16	GND	-		GND	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D7	B_VDDIB0_R	-		B_VDDIB0_R	-	
E10	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
F10	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
K10	VCC12	-		VCC12	-	
A11	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D10	B_VDDOB0_R	-		B_VDDOB0_R	-	
B11	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D11	B_VDDOB1_R	-		B_VDDOB1_R	-	
B12	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L10	VCC12	-		VCC12	-	
A12	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
F11	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
E11	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
G11	VCC12	-		VCC12	-	
D8	B_VDDIB1_R	-		B_VDDIB1_R	-	
G12	VCC12	-		VCC12	-	
D9	B_VDDIB2_R	-		B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-		VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-		B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-		B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-		VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-		VCC12	-	
E9	B_VDDIB3_R	-		B_VDDIB3_R	-	
L13	VCC12	-		VCC12	-	
J11	B_REFCLKN_R	-		B_REFCLKN_R	-	
H11	B_REFCLKP_R	-		B_REFCLKP_R	-	
M15	PT61D	1	HDC/SI	PT77D	1	HDC/SI
M16	PT61C	1	LDCN/SCS	PT77C	1	LDCN/SCS
F14	PT59B	1	D8/MPI_DATA8	PT77B	1	D8/MPI_DATA8
G14	PT59A	1	CS1/MPI_CS1	PT77A	1	CS1/MPI_CS1
L15	PT58D	1	D9/MPI_DATA9	PT75D	1	D9/MPI_DATA9
L14	PT58C	1	D10/MPI_DATA10	PT75C	1	D10/MPI_DATA10
D14	PT57B	1	CS0N/MPI_CS0N	PT75B	1	CS0N/MPI_CS0N
E14	PT57A	1	RDN/MPI_STRB_N	PT75A	1	RDN/MPI_STRB_N
L16	PT55D	1	WRN/MPI_WR_N	PT74D	1	WRN/MPI_WR_N
K16	PT55C	1	D7/MPI_DATA7	PT74C	1	D7/MPI_DATA7
G15	PT55B	1	D6/MPI_DATA6	PT74B	1	D6/MPI_DATA6

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

	LFSC/M40			LFSC/M80		
Ball Number	**Ball Function**	**VCCIO Bank**	**Dual Function**	**Ball Function**	**VCCIO Bank**	**Dual Function**
W13	VCCAUX	-		VCCAUX	-	
W22	VCCAUX	-		VCCAUX	-	
Y21	GND	-		GND	-	
Y25	GND	-		GND	-	
C18	VCCIO1	-		VCCIO1	-	
D17	VCCIO1	-		VCCIO1	-	
F16	VCCIO1	-		VCCIO1	-	
G19	VCCIO1	-		VCCIO1	-	
J20	VCCIO1	-		VCCIO1	-	
K12	VCCIO1	-		VCCIO1	-	
K15	VCCIO1	-		VCCIO1	-	
L23	VCCIO1	-		VCCIO1	-	
Y9	GND	-		GND	-	
J9	VCCIO1	-		VCCIO1	-	
E3	VCCIO2	-		VCCIO2	-	
G6	VCCIO2	-		VCCIO2	-	
H4	VCCIO2	-		VCCIO2	-	
K7	VCCIO2	-		VCCIO2	-	
L3	VCCIO2	-		VCCIO2	-	
M11	VCCIO2	-		VCCIO2	-	
N6	VCCIO2	-		VCCIO2	-	
P4	VCCIO2	-		VCCIO2	-	
R9	VCCIO2	-		VCCIO2	-	
AA3	VCCIO3	-		VCCIO3	-	
AB7	VCCIO3	-		VCCIO3	-	
AC10	VCCIO3	-		VCCIO3	-	
AD4	VCCIO3	-		VCCIO3	-	
AE6	VCCIO3	-		VCCIO3	-	
AG3	VCCIO3	-		VCCIO3	-	
AK4	VCCIO3	-		VCCIO3	-	
T7	VCCIO3	-		VCCIO3	-	
U3	VCCIO3	-		VCCIO3	-	
V4	VCCIO3	-		VCCIO3	-	
W6	VCCIO3	-		VCCIO3	-	
Y10	VCCIO3	-		VCCIO3	-	
AD12	VCCIO4	-		VCCIO4	-	
AF15	VCCIO4	-		VCCIO4	-	
AF9	VCCIO4	-		VCCIO4	-	
AH10	VCCIO4	-		VCCIO4	-	
AH16	VCCIO4	-		VCCIO4	-	
AJ13	VCCIO4	-		VCCIO4	-	
AJ7	VCCIO4	-		VCCIO4	-	
AL14	VCCIO4	-		VCCIO4	-	
AL8	VCCIO4	-		VCCIO4	-	
AM11	VCCIO4	-		VCCIO4	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

	LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function
N27	PL47C	7	
P27	PL47D	7	
K33	PL49A	7	
L33	PL49B	7	
M30	PL49C	7	
N30	PL49D	7	
M31	PL51A	7	
N31	PL51B	7	
P24	PL51C	7	
R24	PL51D	7	
M33	PL56A	7	
N33	PL56B	7	
U25	PL56C	7	
T25	PL56D	7	
L34	PL57A	7	
M34	PL57B	7	
P29	PL57C	7	
R29	PL57D	7	
N34	PL60A	7	
P34	PL60B	7	
R27	PL60C	7	
T27	PL60D	7	
R32	PL61A	7	PCLKT7_1
R31	PL61B	7	PCLKC7_1
U24	PL61C	7	PCLKT7_3
T24	PL61D	7	PCLKC7_3
P33	PL62A	7	PCLKT7_0
R33	PL62B	7	PCLKC7_0
T26	PL62C	7	PCLKT7_2
U26	PL62D	7	PCLKC7_2
T32	PL64A	6	PCLKT6_0
T31	PL64B	6	PCLKC6_0
U29	PL64C	6	PCLKT6_1
V29	PL64D	6	PCLKC6_1
T30	PL65A	6	
U30	PL65B	6	
U27	PL65C	6	PCLKT6_3
V27	PL65D	6	PCLKC6_3
R34	PL66A	6	
T34	PL66B	6	
U28	PL66C	6	PCLKT6_2
V28	PL66D	6	PCLKC6_2
V30	PL69A	6	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP27	PB26A	5	
AP26	PB26B	5	
AK25	PB26C	5	
AK24	PB26D	5	
AN25	PB29A	5	
AN24	PB29B	5	
AE22	PB29C	5	
AE21	PB29D	5	
AM26	PB31A	5	
AM25	PB31B	5	
AF22	PB31C	5	
AF21	PB31D	5	
AN23	PB47A	5	
AN22	PB47B	5	
AP23	PB57A	5	
AP22	PB57B	5	
AG21	PB57C	5	
AG20	PB57D	5	
AP25	PB50A	5	PCLKT5_3
AP24	PB50B	5	PCLKC5_3
AD21	PB50C	5	PCLKT5_4
AD20	PB50D	5	PCLKC5_4
AL23	PB51A	5	PCLKT5_5
AL22	PB51B	5	PCLKC5_5
AH24	PB51C	5	
AH23	PB51D	5	
AM23	PB53A	5	PCLKT5_0
AM22	PB53B	5	PCLKC5_0
AJ24	PB53C	5	
AJ23	PB53D	5	VREF2_5
AN21	PB54A	5	PCLKT5_1
AN20	PB54B	5	PCLKC5_1
AE19	PB54C	5	PCLKT5_6
AD19	PB54D	5	PCLKC5_6
AK21	PB55A	5	PCLKT5_2
AK20	PB55B	5	PCLKC5_2
AK23	PB55C	5	PCLKT5_7
AK22	PB55D	5	PCLKC5_7
AL20	PB58A	5	
AL19	PB58B	5	
AG19	PB58C	5	
AF19	PB58D	5	
AP21	PB61A	5	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
L5	PR38B	2	
K5	PR38A	2	
G2	PR34B	2	
F2	PR34A	2	
F1	PR30B	2	
E1	PR30A	2	
A2	GND	-	
A33	GND	-	
AA15	GND	-	
AA20	GND	-	
AA32	GND	-	
AA4	GND	-	
AB28	GND	-	
AB6	GND	-	
AC11	GND	-	
AC18	GND	-	
AC25	GND	-	
AD23	GND	-	
AD3	GND	-	
AD31	GND	-	
AE12	GND	-	
AE15	GND	-	
AE29	GND	-	
AE7	GND	-	
AE9	GND	-	
AF20	GND	-	
AF26	GND	-	
AG32	GND	-	
AG4	GND	-	
AH13	GND	-	
AH19	GND	-	
AH25	GND	-	
AH7	GND	-	
AJ10	GND	-	
AJ16	GND	-	
AJ22	GND	-	
AJ28	GND	-	
AK3	GND	-	
AK31	GND	-	
AL11	GND	-	
AL17	GND	-	
AL21	GND	-	
AL27	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
V8	PR41C	2		PR55C	2	
T4	PR41B	2		PR55B	2	
U4	PR41A	2		PR55A	2	
V9	PR39D	2		PR53D	2	
U9	PR39C	2		PR53C	2	
V6	PR39B	2		PR53B	2	
U6	PR39A	2		PR53A	2	
AA12	PR38D	2		PR52D	2	
Y12	PR38C	2		PR52C	2	
P1	PR38B	2		PR52B	2	
N1	PR38A	2		PR52A	2	
T7	PR37D	2		PR51D	2	
R7	PR37C	2		PR51C	2	
T5	PR37B	2		PR51B	2	
R5	PR37A	2		PR51A	2	
U10	PR35D	2		PR49D	2	
V10	PR35C	2		PR49C	2	
P2	PR35B	2		PR49B	2	
N2	PR35A	2		PR49A	2	
T8	PR34D	2		PR48D	2	
R8	PR34C	2		PR48C	2	
N3	PR34B	2		PR48B	2	
P3	PR34A	2		PR48A	2	
M6	PR33D	2		PR47D	2	
M7	PR33C	2		PR47C	2	
T6	PR33B	2		PR47B	2	
R6	PR33A	2		PR47A	2	
V11	PR31D	2		PR45D	2	
U11	PR31C	2		PR45C	2	
M1	PR31B	2		PR45B	2	
L1	PR31A	2		PR45A	2	
Y14	PR30D	2		PR44D	2	
W14	PR30C	2		PR44C	2	
M2	PR30B	2		PR44B	2	
L2	PR30A	2		PR44A	2	
T9	PR29D	2	DIFFR_2	PR43D	2	DIFFR_2
R9	PR29C	2	VREF1_2	PR43C	2	VREF1_2
P4	PR29B	2		PR43B	2	
N4	PR29A	2		PR43A	2	
N7	PR26D	2		PR40D	2	
N8	PR26C	2		PR40C	2	
P5	PR26B	2		PR40B	2	
N5	PR26A	2		PR40A	2	
K7	PR25D	2		PR38D	2	
J7	PR25C	2		PR38C	2	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FC1152C[1]	-6	Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FC1152C[1]	-5	Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FC1704C[1]	-6	Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FC1704C[1]	-5	Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.